
IEEE 802.3 Call For Interest 100 Gb/s Lambda Optical PHYs

Consensus Presentation

Objective for this Meeting

- To measure the interest in starting a study group to address:
 - 100 Gb/s per lane Optical PHYs for 100 GbE & 400 GbE
- We don't need to
 - Fully explore the problem
 - Debate strengths and weaknesses of solutions
 - Choose any one solution
 - Create PAR or five criteria
 - Create a standard or specification
- Anyone in the room may speak / vote
- RESPECT... give it, get it

Agenda

- Market Drivers
- Technical Feasibility
- Why Now?
- Q&A Panel
- Straw Polls

Presenters and Panelists

- TBD
-
-
-

Ethernet has a successful track record of reusing and leveraging technology in order to enable new cost-optimized solutions for broad market adoption. Recently, both the IEEE 802.3bs and IEEE 802.3cd Ethernet projects defined optical interfaces based on 100 Gb/s PAM4 per lane optics for 500m reaches on single-mode fiber. This technology enables a lower component count implementation that can lead towards a lower cost solution.

The successful industry adoption of 100 Gb/s is resulting in higher volumes and continuing cost pressures on optical interfaces and the hyper-scale data centers, being aggressive adopters of cost-effective solutions, are looking to enable the next generation of lower cost solutions for 400 Gb/s Ethernet interfaces.

At this time, no IEEE 802.3 Ethernet specifications exist for greater than 500m reaches on single-mode fiber using this advanced technology. This Call For Interest is a request for the formation of a Study Group to explore the potential market requirements and feasibility of extending 100 Gb/s PAM4 per lane optical technology to longer 100 Gb/s and 400 Gb/s Ethernet reaches.

Overview: Motivation

Significant industry interest and progress has been made towards extending the existing IEEE 802.3 Optical PHYs using 100 Gb/s per lane optical technology to longer reaches.

This proposed study group would look to develop 2 km and 10km SMF PHYs for both 100 GbE and 400 GbE

The motivation is to leverage technology to address the ongoing cost pressures on optical interconnects for a set of known and identified markets including:

- Web-scale data centers
- Service Provider
- Enterprise data centers

Today's Point-to-Point SMF Ethernet

	Lanes	500m	2km	10km	20km	40km	Up to 80km	
1000BASE-	1		LX	LX10 / LH		EX	ZX	
10GBASE-	1			LR		ER	ZR	
25GBASE-	1			LR		ER		
40GBASE-	4	PSM4		LR4		ER4		
	1			FR				
50GBASE-	1		FR	LR				
100GBASE-	10		10X10					
	4	PSM4	CWDM4 / CLR4	LR4 / WDM4-10	WDM4-20	ER4 / WDM4-40		
	1	DR					ZR	
200GBASE-	4		FR4	LR4		ER4		
400GBASE-	8		FR8	LR8				
	4	DR4					ER8	ZR
	1							

Black Text

Red Text

Blue Text

IEEE Standard

In Standardization

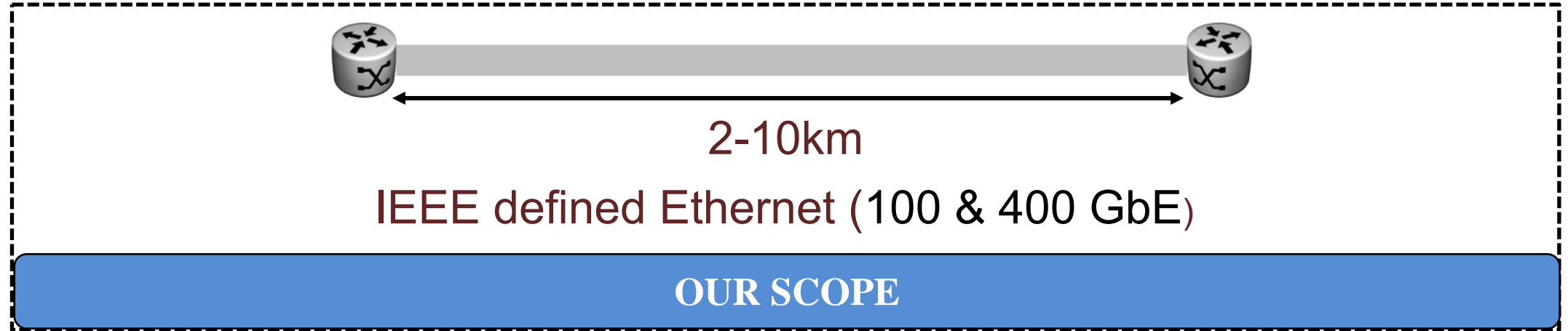
Non-IEEE standard but complies to IEEE electrical interfaces



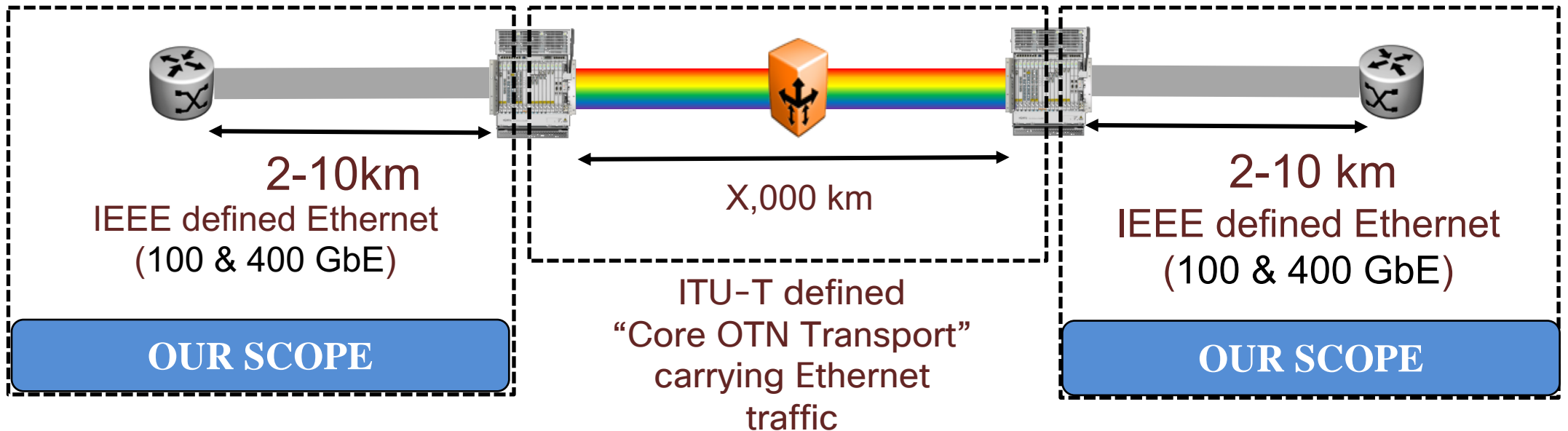
Focus of this CFI

What Are We Talking About?

Scenario #1



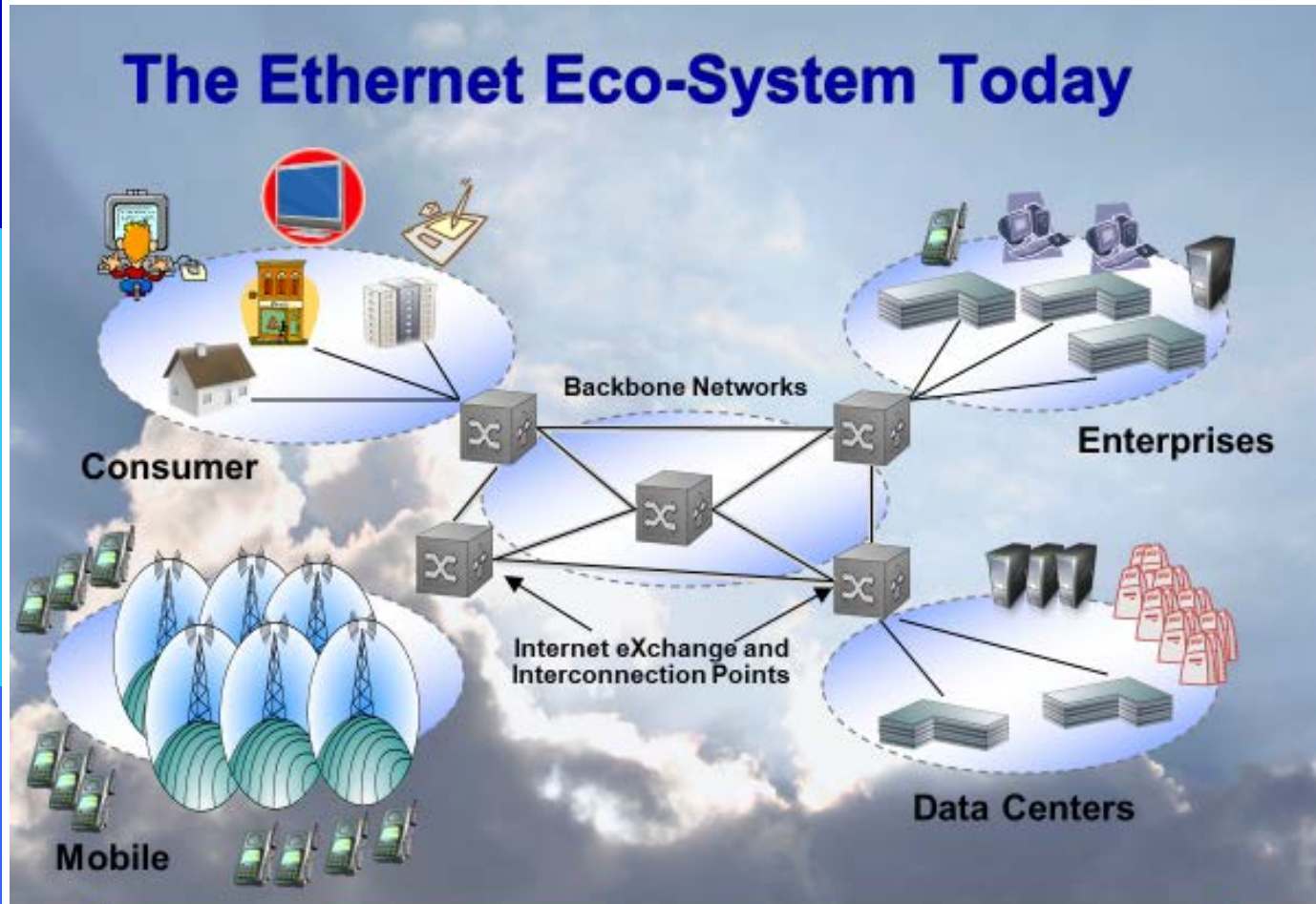
Scenario #2



Market Drivers:

longer reach (up to 10km) 100 Gb/s
per lane optical technology

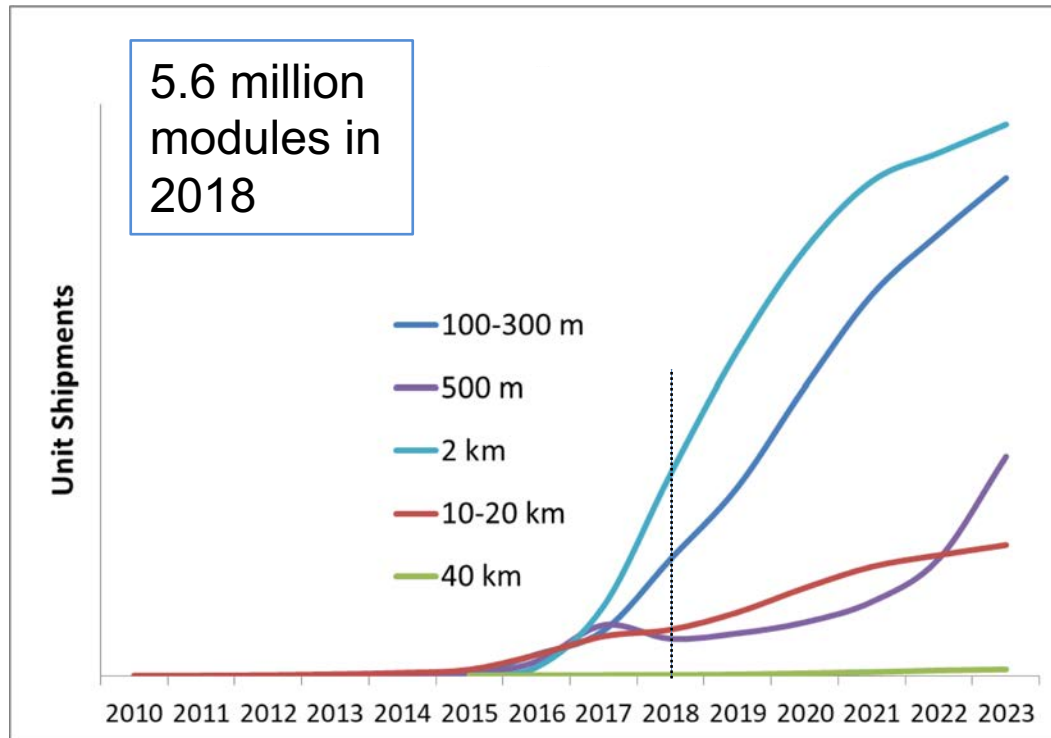
2 & 10km optics dominate throughout SMF ecosystem



- Equipment interconnect within buildings
 - Web-scale Data Center
 - Service Provider Data Center and Point-of-presence
 - Enterprise Data Center
- Intra-building interconnects in campus environment (up to 10km)
- Forecast market size (all formats) of TBD Million ports per year in 202x
- This CFI's goal is to add next generation optical technology into that ecosystem

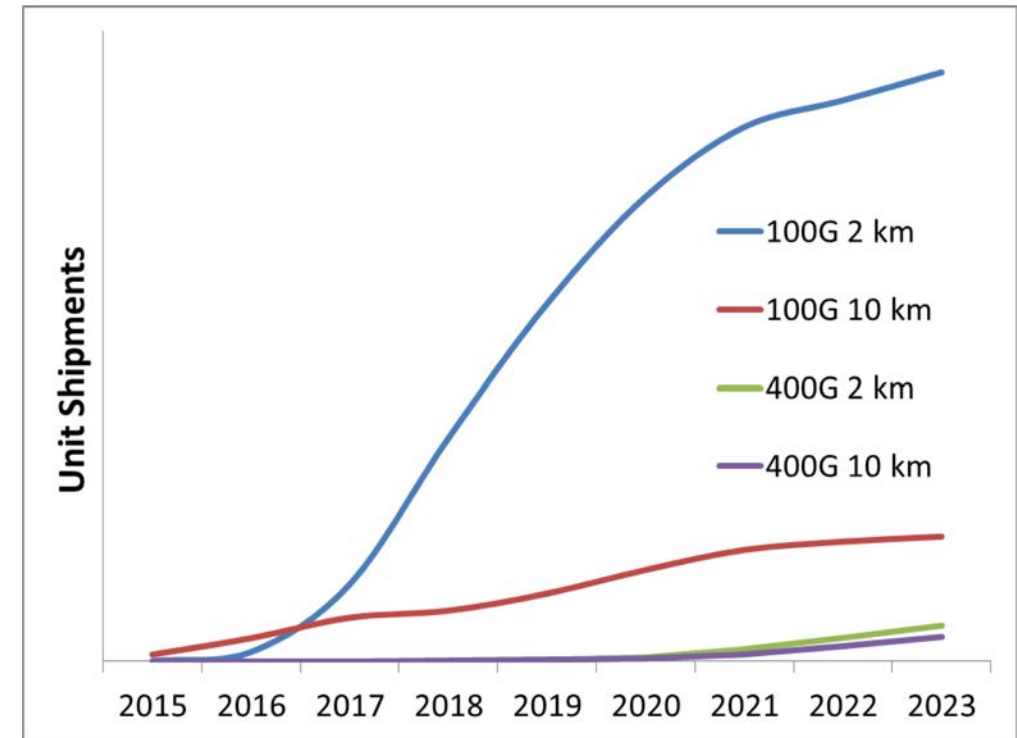
Market Forecast slides

100 GbE Optics by reach



Courtesy Dale Murray, Light Counting

100 GbE & 400 GbE 2 & 10 km SMF Optics



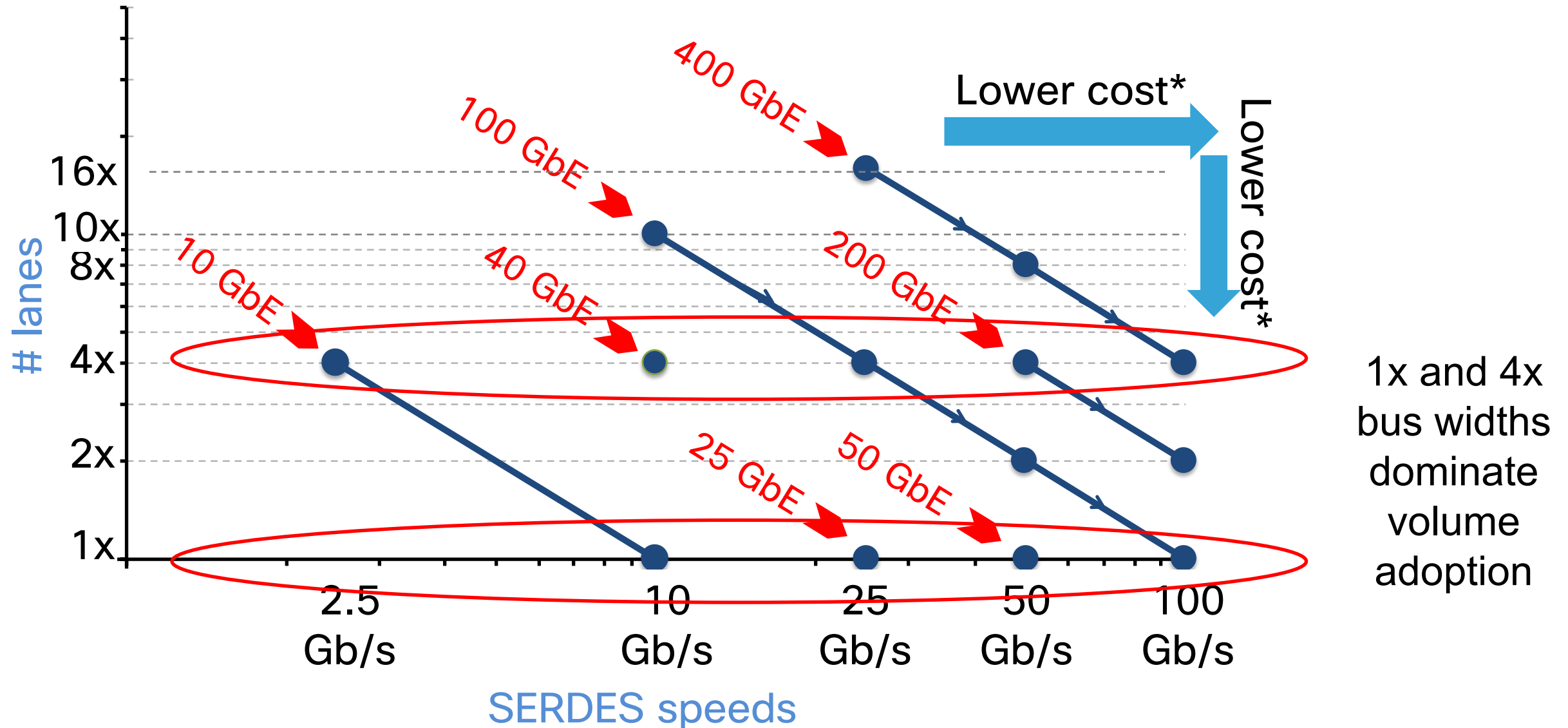
Courtesy Dale Murray, Light Counting

- 100 GbE Optics market still in strong growth phase
- 400 GbE at start of its ramp but expected to be fast

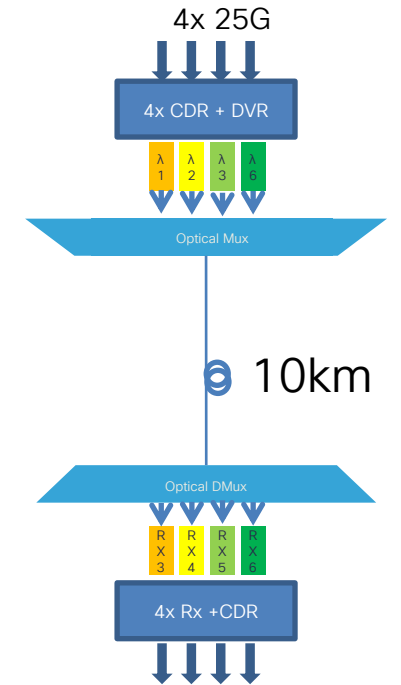
} Both market conditions benefit from cost reductions

* At the right time

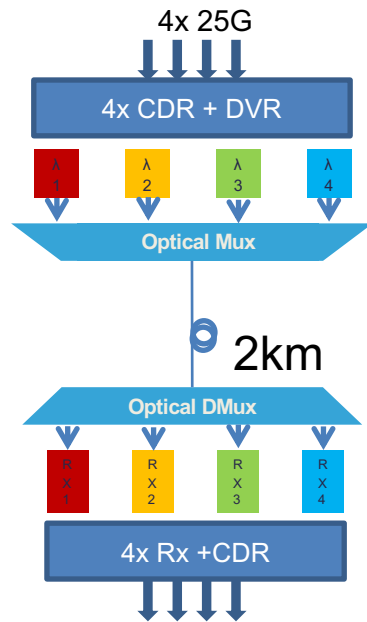
Ethernet's consistent trend – Narrower/Faster



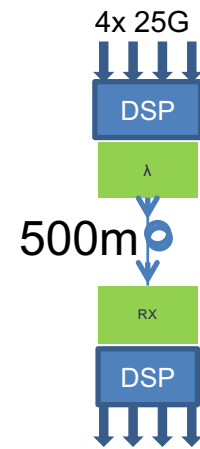
Reduced complexity leads to lower cost



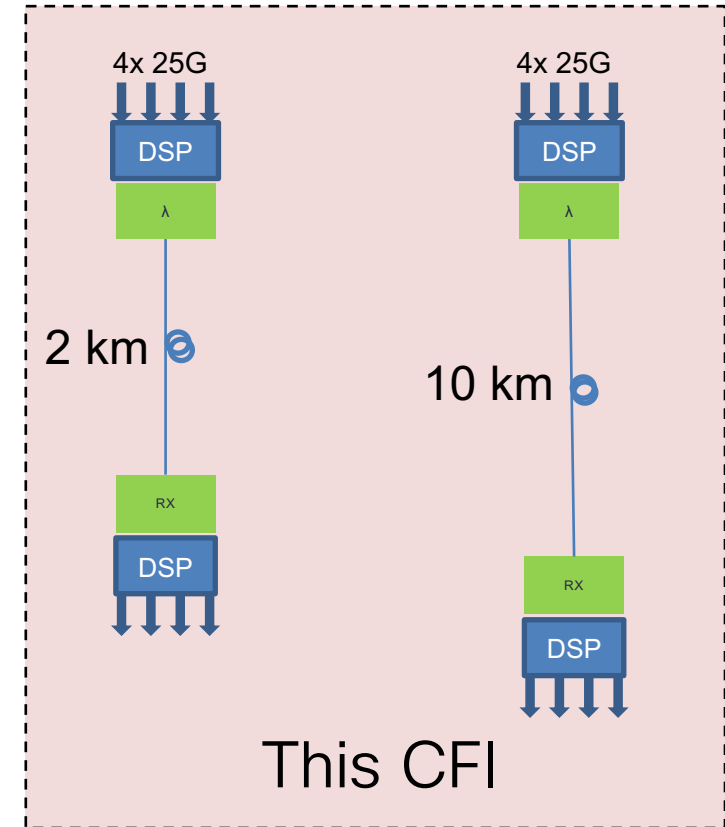
100GBASE-LR4



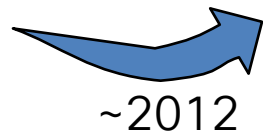
100G-CWDM4



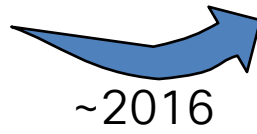
100GBASE-DR



This CFI



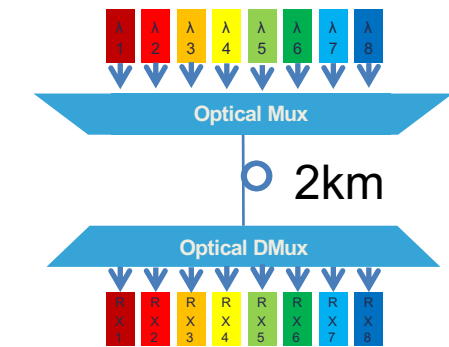
~2012



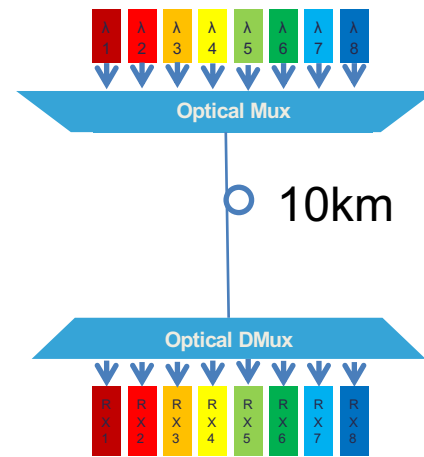
~2016

4x lane reduction

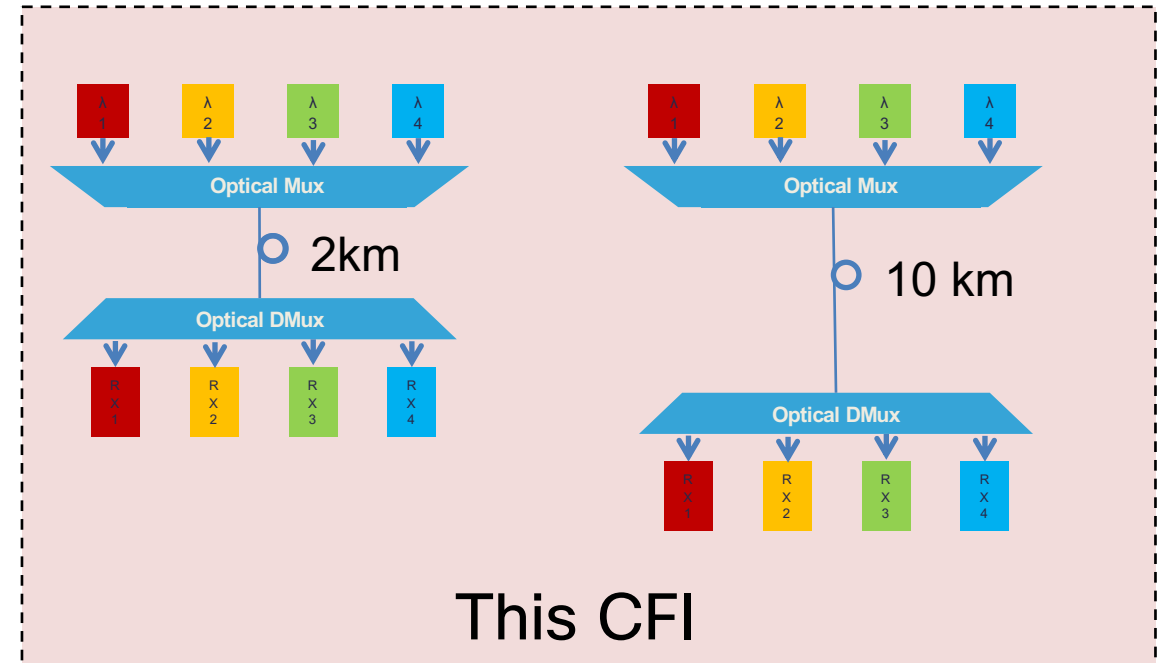
400 GbE Duplex SMF Optics – potential complexity reduction



400GBASE-FR8



400GBASE-LR8

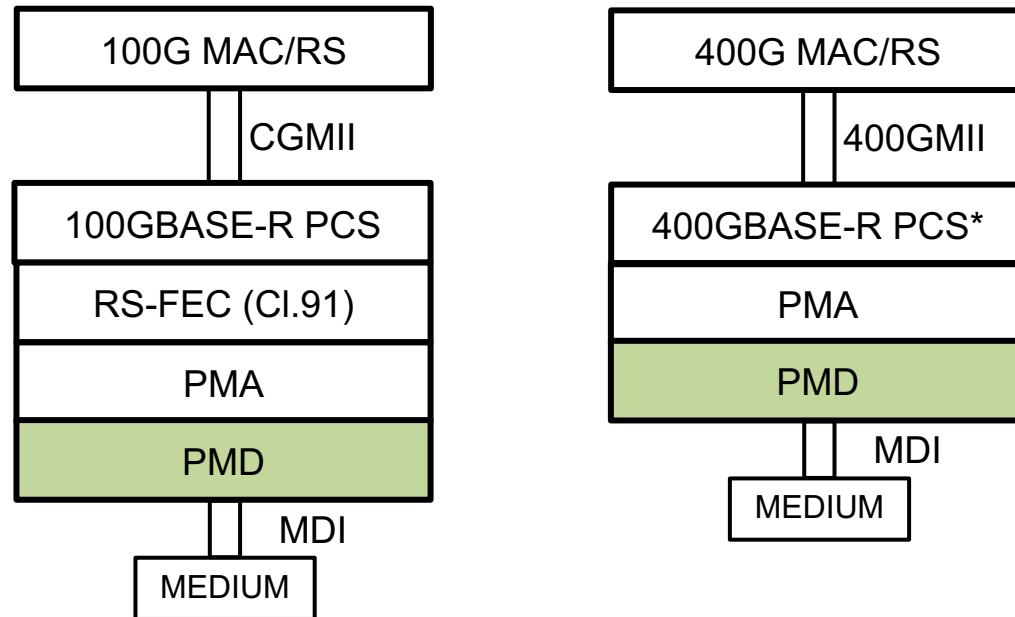


2x lane reduction

Moving from 8 lanes to 4 lanes further enables relaxation on wavelength grid to be considered

Technical Feasibility

IEEE 802.3 Architectural view



- No architectural changes based on anticipated work and scope of project if approved
- New PMDs to be defined
- No compatibility issues with existing host designs

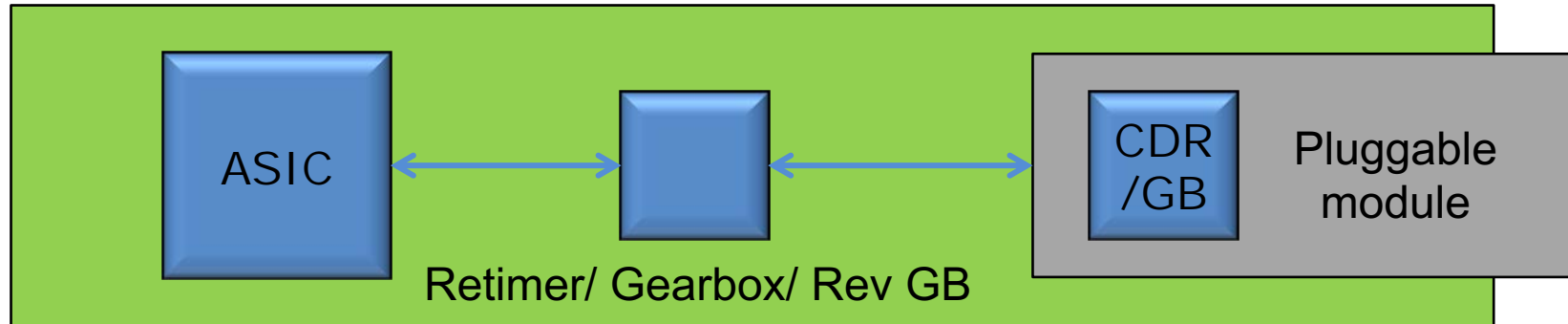
 new

* FEC is part of the PCS sublayer

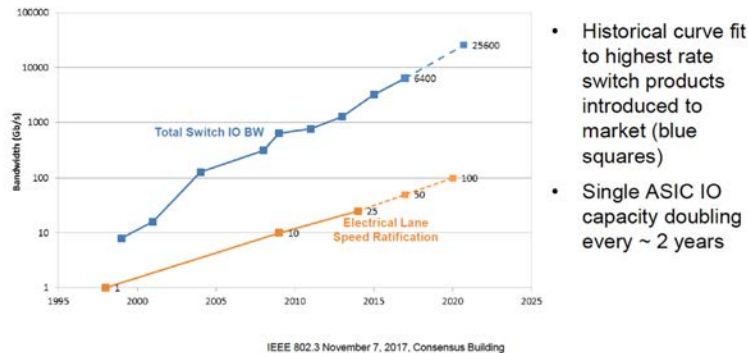
Industry Progress on 100 Gb/s per lane technology

- 400GBASE-DR4 Completed Dec 2017
- 100GBASE-DR Submitted to RevCom – Oct 2018
- Ethernet Alliance awards “Holy Cup” to first public demonstration of 100 Gb/s per lambda in QSFP28 @ ECOC 2018
 - <https://twitter.com/EthernetAllianc/status/1044678676799905793>
- Multiple public demonstrations of 100 Gb/s per lane technology
 - 100 GbE – 500m, 2km, 10km
 - 400 GbE – 500m, 2km
- See examples on next slides

Matching ASIC IO to Module IO



Historical Perspective Shows What's Coming



IEEE P802.3ck's CFI:
http://www.ieee802.org/3/cfi/1117_3/CFI_03_1117.pdf

ASIC IO speed increasing.

When:

- ASIC IO speed = Module IO speed
 - Retimers on as-needed basis per port
- ASIC IO speed > Module IO speed
 - Reverse Gearbox mandatory on all ports

Extending the reach

Link budgets that would extend beyond the current 500m specifications needs to deal with:

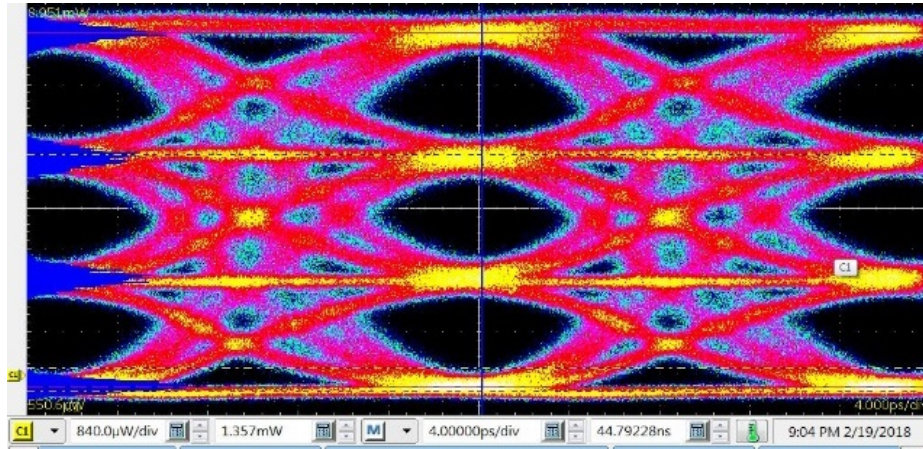
- Extra fiber loss
- Extra wavelength mux/demux loss (400G 2 & 10km only)
- Extra dispersion penalty

Options to address include:

- Increased launch power
- Increased receiver sensitivity (including PIN or APD)
- Wavelength grid (CWDM vs. LWDM)

Technical feasibility - Transmitters

TDECQ = 1.26 dB

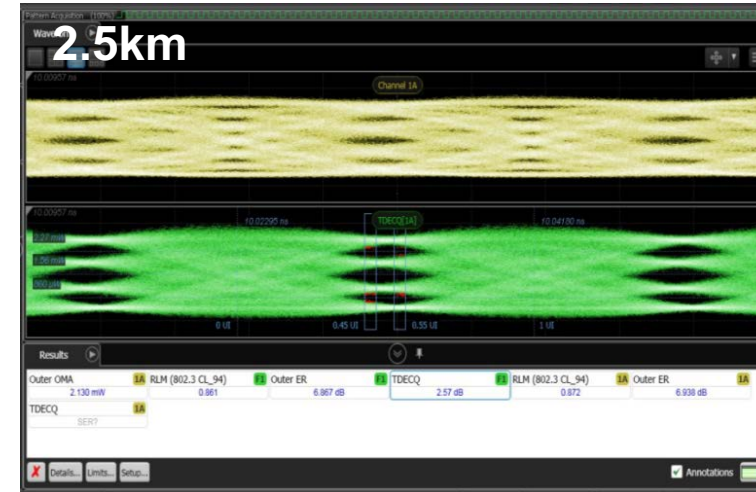


53 GBaud PAM4 (106 Gb/s)

IEEE Pattern PRBS13Q See - mazzini_3cd_01a_0518

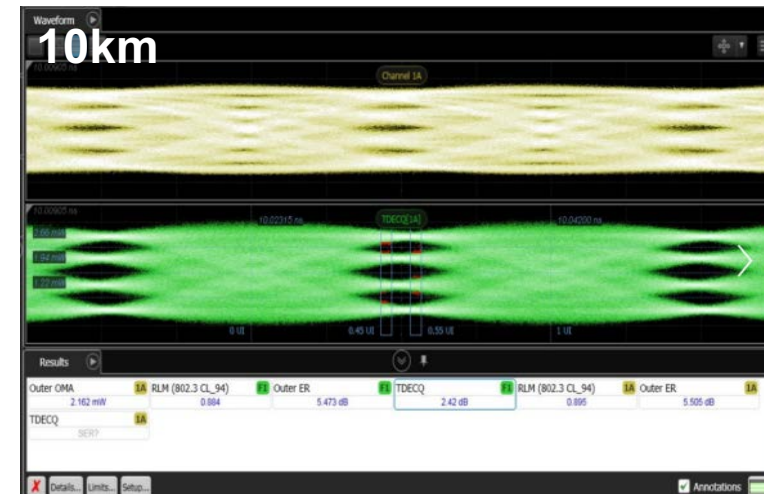
Various transmitters capable of 100 Gb/s PAM4 have been demonstrated or presented

Under construction...



2.5km
Penalty =
0.22dB

ER=5.5dB, TDECQ= 2.64dB



10km
Penalty =
0.21dB

ER=6.9dB, TDECQ= 2.78dB

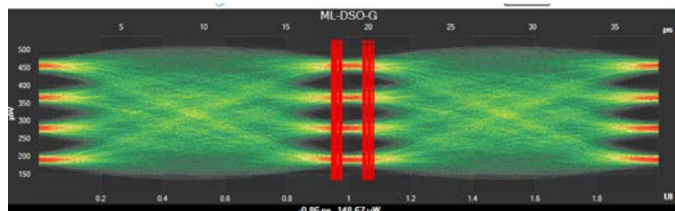
Courtesy Broadcom

Technical feasibility - Receivers

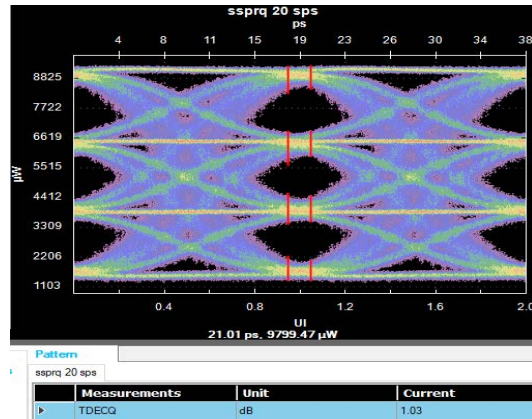
Under construction...

Technical feasibility – Test & Measurement

Advanced TDECQ Test & Measurement equipment available



Courtesy Multilane



Under construction...



Why Now?

Why Now?

- Technical developments underway already to extend 100 Gb/s per lane technology to longer reaches
- Current IEEE Ethernet solutions not fully aligned with end user demand,
 - especially Web-scale Data Centers looking for solutions based on 100 Gb/s per lane technology
- Technical feasibility demonstrations happening
- Standardization in IEEE 802.3 brings industry convergence and extends Ethernet's solution breadth
- Target markets are:
 - Moving into high volume and therefore cost sensitive (e.g. 100 GbE)
 - Initiating early adoption and cost reduction will accelerate (e.g. 400 GbE)

Straw Polls

Straw Poll 1: Call-For-Interest

- Should a Study Group be formed to consider extending 100 Gb/s PAM4 per lane optical technology to longer 100 Gb/s and 400 Gb/s Ethernet reaches up to 10km?

Y: N: A:

Room Count:

Participation

- I would participate in the “100G Lambda*” Study Group in IEEE 802.3.

Tally:

- My company would support participation in the “100G Lambda*” Study Group in IEEE 802.3.

Tally:

* Extending 100 Gb/s PAM4 per lane optical technology to longer 100 Gb/s and 400 Gb/s Ethernet reaches