IEEE 802.3 Timestamp liaison letter Ad Hoc
30th July 2015

David Law
dlaw@hp.com
Agenda

• IEEE-SA patent policy
• Review of ITU-T SG15 letter
• Review of July plenary discussion
• Next steps
Instructions for the WG Chair

The IEEE-SA strongly recommends that at each WG meeting the chair or a designee:

• Show slides #1 through #4 of this presentation

• Advise the WG attendees that:
  • The IEEE’s patent policy is described in Clause 6 of the IEEE-SA Standards Board Bylaws;
  • Early identification of patent claims which may be essential for the use of standards under development is strongly encouraged;
  • There may be Essential Patent Claims of which the IEEE is not aware. Additionally, neither the IEEE, the WG, nor the WG chair can ensure the accuracy or completeness of any assurance or whether any such assurance is, in fact, of a Patent Claim that is essential for the use of the standard under development.

• Instruct the WG Secretary to record in the minutes of the relevant WG meeting:
  • That the foregoing information was provided and that slides 1 through 4 (and this slide 0, if applicable) were shown;
  • That the chair or designee provided an opportunity for participants to identify patent claim(s)/patent application claim(s) and/or the holder of patent claim(s)/patent application claim(s) of which the participant is personally aware and that may be essential for the use of that standard
  • Any responses that were given, specifically the patent claim(s)/patent application claim(s) and/or the holder of the patent claim(s)/patent application claim(s) that were identified (if any) and by whom.

• The WG Chair shall ensure that a request is made to any identified holders of potential essential patent claim(s) to complete and submit a Letter of Assurance.
• It is recommended that the WG chair review the guidance in IEEE-SA Standards Board Operations Manual 6.3.5 and in FAQs 14 and 15 on inclusion of potential Essential Patent Claims by incorporation or by reference.

Note: WG includes Working Groups, Task Groups, and other standards-developing committees with a PAR approved by the IEEE-SA Standards Board.

(Optional to be shown)
Participants, Patents, and Duty to Inform

All participants in this meeting have certain obligations under the IEEE-SA Patent Policy.

- Participants [Note: Quoted text excerpted from IEEE-SA Standards Board Bylaws subclause 6.2]:
  
  - “Shall inform the IEEE (or cause the IEEE to be informed)” of the identity of each “holder of any potential Essential Patent Claims of which they are personally aware” if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents
  
  - “Should inform the IEEE (or cause the IEEE to be informed)” of the identity of “any other holders of potential Essential Patent Claims” (that is, third parties that are not affiliated with the participant, with the participant’s employer, or with anyone else that the participant is from or otherwise represents)
  
  - The above does not apply if the patent claim is already the subject of an Accepted Letter of Assurance that applies to the proposed standard(s) under consideration by this group
  
  - Early identification of holders of potential Essential Patent Claims is strongly encouraged
  
  - No duty to perform a patent search
Patent Related Links

All participants should be familiar with their obligations under the IEEE-SA Policies & Procedures for standards development.

Patent Policy is stated in these sources:

IEEE-SA Standards Boards Bylaws
http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6

IEEE-SA Standards Board Operations Manual

Material about the patent policy is available at
http://standards.ieee.org/about/sasb/patcom/materials.html

If you have questions, contact the IEEE-SA Standards Board Patent Committee Administrator at patcom@ieee.org or visit
http://standards.ieee.org/about/sasb/patcom/index.html

This slide set is available at
https://development.standards.ieee.org/myproject/Public/mytools/mob/slideset.ppt
Call for Potentially Essential Patents

- If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance:
  - Either speak up now or
  - Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible or
  - Cause an LOA to be submitted
Other Guidelines for IEEE WG Meetings

- All IEEE-SA standards meetings shall be conducted in compliance with all applicable laws, including antitrust and competition laws.
  - Don’t discuss the interpretation, validity, or essentiality of patents/patent claims.
  - Don’t discuss specific license rates, terms, or conditions.
    - Relative costs, including licensing costs of essential patent claims, of different technical approaches may be discussed in standards development meetings.
      - Technical considerations remain primary focus
  - Don’t discuss or engage in the fixing of product prices, allocation of customers, or division of sales markets.
  - Don’t discuss the status or substance of ongoing or threatened litigation.
  - Don’t be silent if inappropriate topics are discussed … do formally object.

See IEEE-SA Standards Board Operations Manual, clause 5.3.10 and “Promoting Competition and Innovation: What You Need to Know about the IEEE Standards Association's Antitrust and Competition Policy” for more details.
Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces
IEEE Std 802.3-2012

Figure 90-3—Data delay measurement

<table>
<thead>
<tr>
<th>Specification Range</th>
<th>Description</th>
<th>Standardization Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1801 through 1.1804</td>
<td>TimeSync PMA/PMD transmit path data delay</td>
<td>45.2.1.105</td>
</tr>
<tr>
<td>1.1805 through 1.1808</td>
<td>TimeSync PMA/PMD receive path data delay</td>
<td>45.2.1.106</td>
</tr>
</tbody>
</table>
Data delay diagram
Path delay registers

• Transmit and Receive path data delay registers
  – Maximum and Minimum for each MMD
    • Total of four values: TX min, TX max, RX min, RX max
  – Sum MMDs together to obtain xMII to MDI delay
  – Maximum and Minimum difference due to path delay variability
    • For example due to crossing clock boundaries

• Any variability impacts clock accuracy
  – Implementer free to reduce to minimum possible
    • To support high accuracy clock application
  – Registers are valid when the link is established
    • Can remove link start to link start variations such as FIFO depths
Data delay diagram
Multi-lane data delay diagram

- TX
- Media
- RX

- xMII
- MDI
- MDI
- xMII

- TX
- Media
- RX Deskew
- RX Path

PHY
RX min
RX max
Path delay registers

• Receive path delay defined in terms of MDI
  – Multi-lane PHYs may have different media lane delays
• Suggest arrival time on slowest lane be used
  – Elasticity buffer compensates for different media delays
Multi-lane data delay diagram

TX

Media

RX

xMII  MDI  MDI  xMII

TX  Media  RX  RX

TX  Media  RX Deskew  RX Path

PHY  RX min  RX max
Multi-lane data delay diagram

TX

Media

RX

xMII

MDI

MDI

PHY
RX min
RX max

RX

xMII

TX

Media

RX Deskew

RX Path