XAUI Breakouts
IEEE802.3ae Jitter Adhoc Meeting
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Sponsered by 10Gbe Alliance

Anthony Sanders
COM ANS SYS

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Contents

1 Introduction

The following document is a summary of the XAUI issues covered in the 2 day adhoc in Austin Texas.
The main focus of the adhoc meeting was jitter related issues, with the main body of the group dealing with the 10G PMD Jitter issues. However, the morning of each day also entailed two breakoff XAUI Jitter meetings. The first on Thursday, being chaired by Shelto Van Dorn (NSerial) started discussion on the current status of the XAUI Jitter specification, and pinned down the current proposal for extending the second corner frequency of the jitter tolerance mask. The second on Friday, being chaired by Anthony Sanders (Infineon), consisted of an implementors sanity check, which took a step back to assess if all phenomina relevant to a XAUI channel interfaces have been thought through, if all these phenomina were covered in some way by the specification, and if the numbers in the specification were based on reasonable assumptions.
The following sections are a combined summary of all issues dealt with over the 2 days are are not in chronological order, as many issues were revisited and refinned.

2 Organisational Issues

The current PMD Serial Reflector shall be renamed to Jitter, and shall be used for all PMD Serial Issues and XAUI issues, including Channel Compliance.

3 XAUI Test Patterns

Use of FC defined patterns would seems to be a logical step for compliance testing. Please refer to 10.8 for some further details.

- SSO D21.5 101010 Simulatious Switching
- FC CRPAT 8b10b good random data
- K25.5 +- has low and high frequency components
- K28.7 +- 5x0, 5x1 good for random jitter, due to elimate of DJ
- FC CTPAT, spectral peak plus jump

It is currently not anticipated, how codes shall be introduced into the XAUI channel, and how BER shall be measured. Possible methods for measurement can be reference from the current FC specifications, however, exact implementation shall be left open.

4 XAUI Jitter tolerance

Very low frequency jitter or wander below the f_c/25000 should not be an issue for the XAUI receive CDR theoritically, however the effect on FIFO sizing could be relevant. Based on this it is proposed that the low frequency part of the Jitter Tolerance be extented down to between 10kHz and 45kHz; the final frequency being based on the results cited [1].

It is currently the opinion that for the calculation of the FIFO, Jumbo frames should be used, although they are not officially supported within the current definition of the 802.3ae. In addition the calculation for the FIFO size could be assumed to be on the encoded or decoded data and is a matter of implementation. It should not be forgotten in the calculation of the FIFO size the requirements of the WIS, which will be the most dominating factor in a UniPhy implementation.

The low frequency jitter as defined by the current FC sinusoidal jitter specification is to take of the effects of for example poor switching power supplies, and it can be seen that the 20dB increase in low frequency jitter from the f_c/1667 down to f_c/25000 is a direct calculated from a hyperthetical 100ppm tolerance clock.

Please refer to section 10.3 for further details regarding jitter tolerance.

5 XAUI Upper Jitter Tolerance Corner Frequency

There are currently a number of proposal from Agilent and Broadcom concerning moving the current f_c/1667 corner frequency for the jitter tolerance to 2..3 times it's current value.

The proposal from Agilent consists of simply shifting the entire 20dB slope right along the frequency axis, and limiting then the maximum jitter amplitude at 1.5UI down to the current f_c/25000.

The proposal from Broadcom involves some increasing of the slope of the jitter tolerance, which must be discussed in some more detail.

It was heard how pushing the corner frequency out would ease the loop filter design for the CMU, especially in respect to high integration solutions, because of the decrease in intergrated capacitor size. However, counter arguments pointed out how only a single CMU would most likely be present on any XAUI design, incompatibility to other current standards e.g InfiniBand would put too much pressure on SerDes designers and how the PSSR could be degraded.

If was also pointed out that by pushing the corner frequency of the transmit CMU out, although this could be compensated by also pushing the corner frequency of the CDR out; this would lead to more difficulties in controlling jitter peaking of the CDR. Although jitter peaking is not an issue concerning jitter transfer as clock looping is not anticipated as being an acceptable option, the possibility for spectral content on the transmit side being then amplified by the CDR and leading to reduced set and hold times was voiced as a concern. This concern was also voiced by Ali Ghiasi on behalf of Newport.

The final straw poll showed that any attempt to try and move the corner frequency out would not be supported in a ballot.

6 XAUI Transmit Jitter

Due to the current fears of large amounts of high frequency jitter being present in the receive signal, there was a proposal from Ali Ghiasi to reduce receive DJ to 0.39UI from 0.415UI, to allow more room for RJ.

It should be noted that the current v2.0 draft contains typos concerning X1, and X2, and X1 should read 0.175UI, and X2 0.415UI.

[2] defines on the transmit data eye, an X2 equal to (X1+0.19UI), however, this 0.19UI should be reassed as to its relevance in this specification. Given this definition of X2 this would then give an X2 of 0.365UI as opposed to the current 0.415UI, which is currently considered as not allowing for enough jitter in the channel.

These questions of DJ and RJ in the channel will have to remain open until the final channel compliance investigation is finally closed.

7 XAUI Jitter Transfer

It is not necessary to include jitter transfer specification to allow for the implementation of loop back clocks on the XAUI side. After the receive jitter tolerance is extended down to a lower frequency, this in combination with the filtered transmit jitter should be sufficient to maintain a control on jitter accumalation. [1].

8 XAUI Clocking Sources

It is definately the opinion of all implementors and also customers that the XAUI interface shall require a very clean, low spectral content clock for reference on the XAUI transmit side. And that this clock will almost definately not be a cheap crystal. Many bad experiences have been made by chip integrators concerning fully integrated clock sources or attempts to save money by use of cheap clocking sources.

9 XAUI Sanity Check

The following bullet points are an attempt to summarise all possible phenomina that could effect the compliance, operability and interopability of a XAUI link. It should be the goal of the final specification, to make sure that any phenomina are somehow taken into account but not necessaryly directly. e.g PSD of a CMU VCO is not directly specified but is covered in the definition of RJ for the transmit data eye given a high pass filter with corner frequency of f_c/1667.
Each subsection is a loose grouping of the sub-points.

9.1 Clocking

9.1.1 Quality of transmit clock source

- Clock source PSD
- Clock offsets (Temperature, Power supply)
- EME Issues (Modulation of clocking source)

9.1.2 CMU Characteristic

- Inherent PLL Noises (Phase Noise, CP/PD)
- Power supply noise Transfer functions
- Phase transfer function

9.1.3 Receiver CDR Characteristics

- Inherent PLL Noises
- Peaking
- Phase transfer function
- Cheap CMOS Phase Detector could be more sensitive to DCD parts of DJ, and therefore may have to be specified seperately.
- Typical Setup/Hold time
- Possible Loopback of clocks and accumalation of low frequency jitter (does defn of receiver tolerance pin this down). ?? Is this a real practical issue.

9.2 Measurement and Compliance

- How do we test transmitter
- How do we test receiver
- How do we guarentee interopobility between manufactures

[1] This assumption must be verified with the XAUI channel model

9.3 Driver/Receiver

- Driver Mismatch/Non-linearities
- H(w) of package, PCB
- Electrical specification

9.4 Power Supply Noise

- Frequency depedant clock offsets
- Driver common mode noise
- Recieve sensitivty (PSSR, common mode -> Time Jitter)
- Time jitter TxRJ VCO PSSR, RxRJ VCO PSSR
- Trace Coupling on PCB (Note : Measurement of chopper noise using differential probe vs. single probe with ground return is critical)

9.5 SSO

- Pattern on all four channels
- Driver signal dependancy
- Crossing onto PLL
- Given "killer" packets causing PSN, increased RJ and failure.

9.6 Crosstalk

- Contra-directional FEXT / NEXT
- Co-directional FEXT/NEXT
- Pattern Dependancy
- PCB Crosstalk
- On Chip
- From other chips
- Specification must make sure that enough margin is included to cover worst case skew, with "worst case" pattern.
- Connectors can play large role in cross talking issues.

9.7 EMC

- Telephone
- Black and Decker test

9.8 EME (Radiated Emissions)

- PCB design (stripline or microstrip, plus grounding, vias)
- Driver signal strength (amplitude and dv/dt)
- Coding
- Terminations (reflection cooef, differential balance)
- Common mode noise, differential skew

9.9 PCB Design

- 2x6", 2xconnectors, 12" BP
- XAUI driving LDD or BP
- vias
- connectors
- Layer Stackup (aufbau)

- tolerances
- resonance
- other materials
- Multiple Channels
- External Noise Sources (Transmitters, Switching, Supplies)

9.10 Equalisation

- White paper "Compliance at 0" and 20" implies compliance at all points inbetween."
- Programmability
- Forms of recieve equalisation

9.11 FIFO Sizing

- White paper to be written "Standard point to point connection"
- White paper "Concatenated XAUI interfaces"

10 IEEE Specification

The following bullet point section is a summary of the items currently covered by the IEEE802.3ae and items currently proposed with a strong possibility for inclusion.

10.1 Transmitter Compliance (non-equalised system)

- Filter defined
- Transmit Data Eye (10e-12 BER)
- Defined Transmit DJ, RJ
- BERT possible [2]
- TIA possible

10.2 Transmitter Compliance (equalised system)

- Inclusion of compliance channel
- Filter defined [3]
- Receive Data Eye [4]
- Defined Recieve DJ, RJ
- Measured for 0änd 20Ẅhat is 0"
- BERT possible
- TIA possible

10.3 Receiver Compliance

- DJ [5]
- RJ [6]

[2] Measurement techniques are not currently specified by the IEEE802ae, but will be most likely borrowed from current non-released FC specification [2]

[3] It is currently unclear if the inclusion of a high pass filter in combination with TJ, defines the max low frequency jitter within realms of FIFO capability and size

[4] Does this include enough amplitude margin for amplitude induced crosstalk

[5] frequency range as in FC specification must be defn, however for testing this is effected goverened by the test pattern

[6] frequency range must be defn as in FC specification

- SJ(f) Tolerance defined [7]
- BERT or TIA possible [8]

10.4 Electrical Transmit/Reciever Characteristics

- Differential amplitude : Based on investigation for non-equalised system
- Absolute amplitudes : Based on current practise to protect decoupling capacitors
- Output/Input Differential Skew : Pinning down Common mode, and EME
- Output/Input Differential return loss : Good practise value incl. frequency. Is this over specificied (must be based on further analysis)
- Output/Input Common mode return loss : Good practise value incl. frequency
- Edge speeds : Based on good practice for EME and Data Eye Compliance
- AC Coupling clearly defined

10.5 Entire Link

- BER clearly defined. [9]

10.6 Jitter/Loss Budget

- Driver
- PCB Trace
- NEXT/FEXT [10]
- Connectors (assumed to include vias) [11]

10.7 Compliance Channel

- Assumes single channel
- S21 [12]
- ISI
- Group delay
- Impedance plus tolerance
- Additional Random Jitter [13]

10.8 Test Patterns

- Defined to excercise certain phenomina
- SSO D21.5 101010 Simulatious Switching
- FC CRPAT 8b10b good random data
- K25.5 +- has low and high frequency components
- K28.7 +- 5x0, 5x1 good for random jitter, due to elimate of DJ [14]

[7] f_c/1667 defined from 100ppm clock offset and 0.1UI high frequency margin. 0.1UI is defined from SWAG pragmatic values from the industry. It should be noted however that the receiver tolerance should be verified with maximum clock offset, plus the defined jitter tolerance mask (refer [2] pp20 99-151)

[8] Measurement techniques are not currently specified by the IEEE802ae, but will be most likely borrowed from current non-released FC specification. However, for receiver testing no indication of exact access to BIST or recovered clocks shall be specified

[9] Currently XAUI is defined for BER=10e-12. However, it is abiguous as to whether this BER applies to each channel or to all four channels. In addition entire 10Gbe link is defined as 10e-12, which would imply the the XAUI channel link must be better than this.

[10] It is current questionable as to whether this currently defined value is enough

[11] again this value is currently assumed to be very optimistic

[12] Definition of acceptable group delay and S21 in compliance channel can be budgeted to account for via, connectors, etc., however again it is currently questionable as to whether there is enough margin in current methodology for the definition of S21 to allow for additional via and connectors

[13] Currently no RJ is defined, however it is felt that some sort of external EMC factor should be include here, although in the jitter budget specification DJ and TJ are defined, but the TJ for the PCB part is smaller than the DJ

[14] There was some questionability as to the ability to really measure the RJ given this code

- FC CTPAT, spectral peak plus jump
- Additional code should be assesed for their ability to excercise multiple lanes [15]

11 White Papers

Currently Infineon shall write three White Papers that shall be published with the IEEE forum.

11.1 XAUI Compliance Basis

This paper is an overview paper based on the results of the XAUI Jitter Adhoc and XAUI Channel Compliance Adhoc. The paper shall outline the reasoning for the numbers contained with the IEEE802.3 specification for the XAUI link, and will form the basis for any implementor wishes to understand the physical basis for the specification.

11.2 XAUI Equalisation Compliance at 0" and 20" Implies Compliance at All Intermediate Points

Based on the clear need for equalisation of the XAUI link, either on the transmit and, or recieve side. Infineon shall also look towards the ongoing question as to whether spot compliance testing of the XAUI with equalisation at 0" and 20" is sufficient to guarentee compliance at all other points along the link.

11.3 FIFO Sizing for Point to Point XAUI Connection

It is clear that some confusion exists within the IEEE concerning clock offsetting and frequency jitter. To this end, Infineon shall release a short paper explaining the effect of these phenomina on the sizing of a simple FIFO.

References

[1] Anthony Sanders, *The Effect of Clock Tolerance and Jitter on FIFO Sizing*, IFX COM ANS, to be released.

[2] T11.2 Technical Committee, *Fibre Channel - Methodologies for Jitter Specification*, T11.2 Project 1230 Rev 10, June 9 1999

[3] Hanson et al, *Proposed Set Of Three 10 Gigabit Ethernet PMDs and Related Specifications*, hanson_1_0500.pdf, May 23 2000.

[15] Currently no suggestions exist