XGMII Transmit Direction Timing
Clause 46

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Comments

- Transmit direction timing benefits from being non symmetrical
- 1UI=320ps. @40% duty cycle DDR, 1/2 cycle = 256ps.
- Data is sampled at both clock edges
- Timing is easier to meet if setup/hold is skewed toward front half of UI

Source Synchronous Timing

Ttdct: Data, Clock Transition Window; Ttds, Ttdh: setup, hold; 40% Clock Duty Cycle

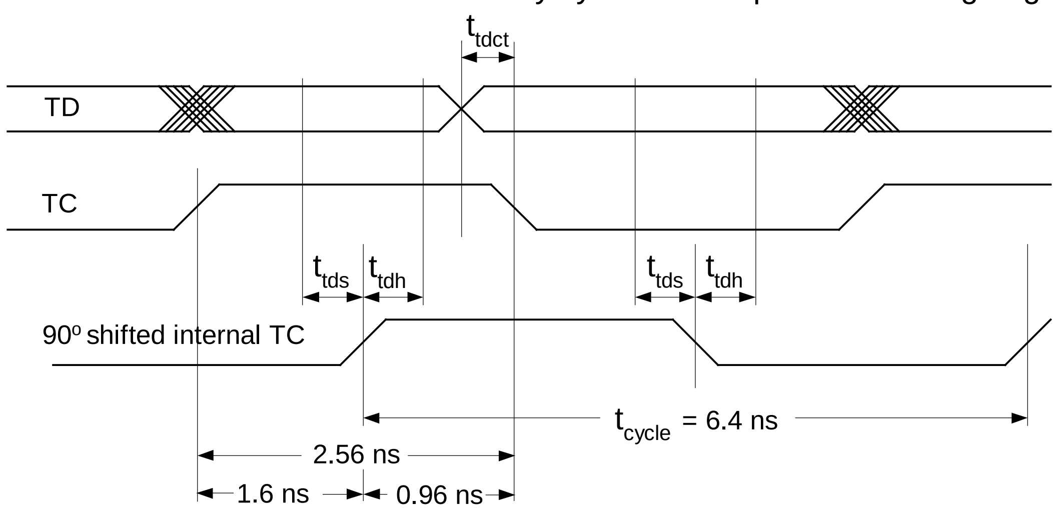
$$Tcycle * (40\%) - Tcycle * (1/4) > Ttdh + Ttdct$$

At 3.125 Gbps, this translates to:

$$960\ ps > Ttdh + Ttdct$$

The next page shows the other corner case that places a limit on Ttds.

TSH = 0 and TC with 40% duty cycle with respect to its rising edge



2.56 ns - 1.60 ns = 0.96 ns > t_{tdh} + t_{tdct}

Source Synchronous Timing

For worse case: TC is 60% duty cycle from its rising edge:

Tcycle * (40%) - Tcycle * (1/4) > Ttds + Ttdct

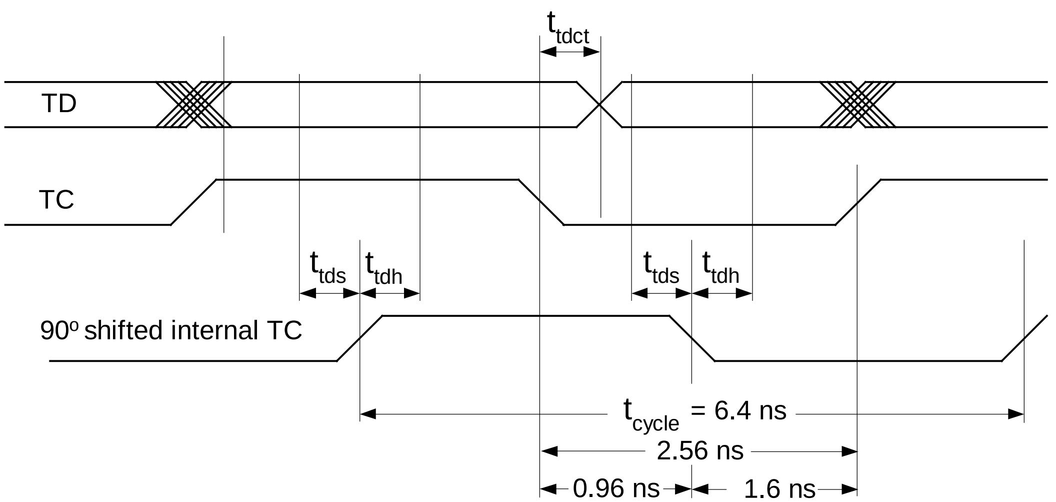
At 3.125 Gbps, this translates to:

960 ps > Ttds + Ttdct

Adding the two pages: 1920 ps > Ttds + Ttdh + 2 * Ttdct

If Ttds + Ttdh = 960 ps at destination, Ttdct < 480 ps (from – to + : 960 ps range)

TSH = 0 and TC with 60% duty cycle with respect to its rising edge



2.56 ns - 1.60 ns = 0.96 ns > t_{tds} + t_{tdct}

Setup, Hold Timing

$$Tcycle * (40\%) > Ttds + Ttdelay(max)$$
$$Tdelay(min) > Ttdh$$

At 3.125 Gbps, this translates to:

$$2560\ ps > Ttds + Ttdelay(max)$$
$$2560\ ps - (Ttds + Ttdh) > Ttdelay(max) - Ttdelay(min)$$

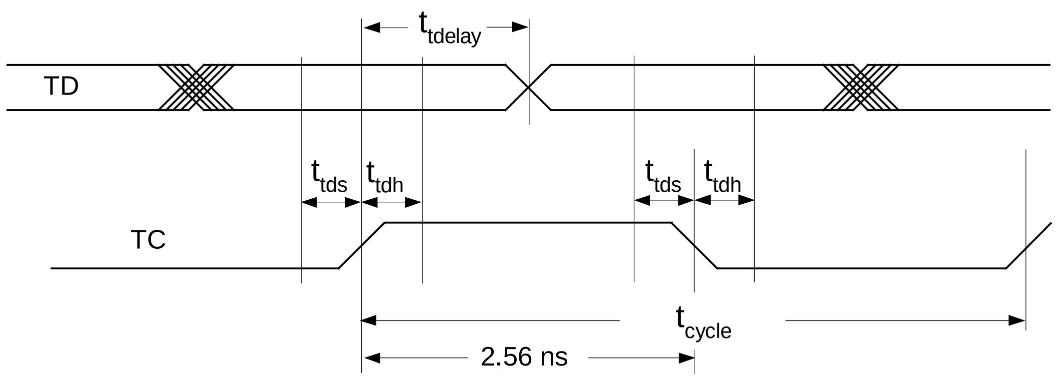
If Ttds + Ttdh = 960 ps at destination

$$1600\ ps > Ttdelay(max) - Ttdelay(min)$$

If Ttdh is 480 ps, Tdelay range is: 480 – 2080 ps at destination (at driver: 960 – 1600)
If Ttdh is 160 ps, Tdelay range is: 160 – 1760 ps at destination (at driver: 640 – 1280)

The first case gives a Tdelay(max) / Tdelay(min) ratio of 1.67, the second: 2.00

TSH = 1 and TC with 40% duty cycle with respect to its rising edge



$$2.56\ ns > 3 * t_{tdelay} + t_{tds}$$
$$t_{tdelay} > t_{tdh}$$

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CONCLUSION:

For XGMII Transmit Direction Timing

- Setup and Hold Timing is Better than Source Synchronous
- Asymmetry in Setup and Hold more flexible for the ASIC/FPGA
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	Recommend		Old	
	Driver	Receiver	Driver	Receiver
Tsetup	1280ps	800ps	960	480
Thold	640ps	160ps	960	480