IEEE P802.3ae
10 Gigabit Ethernet Task Force

XGMII Update

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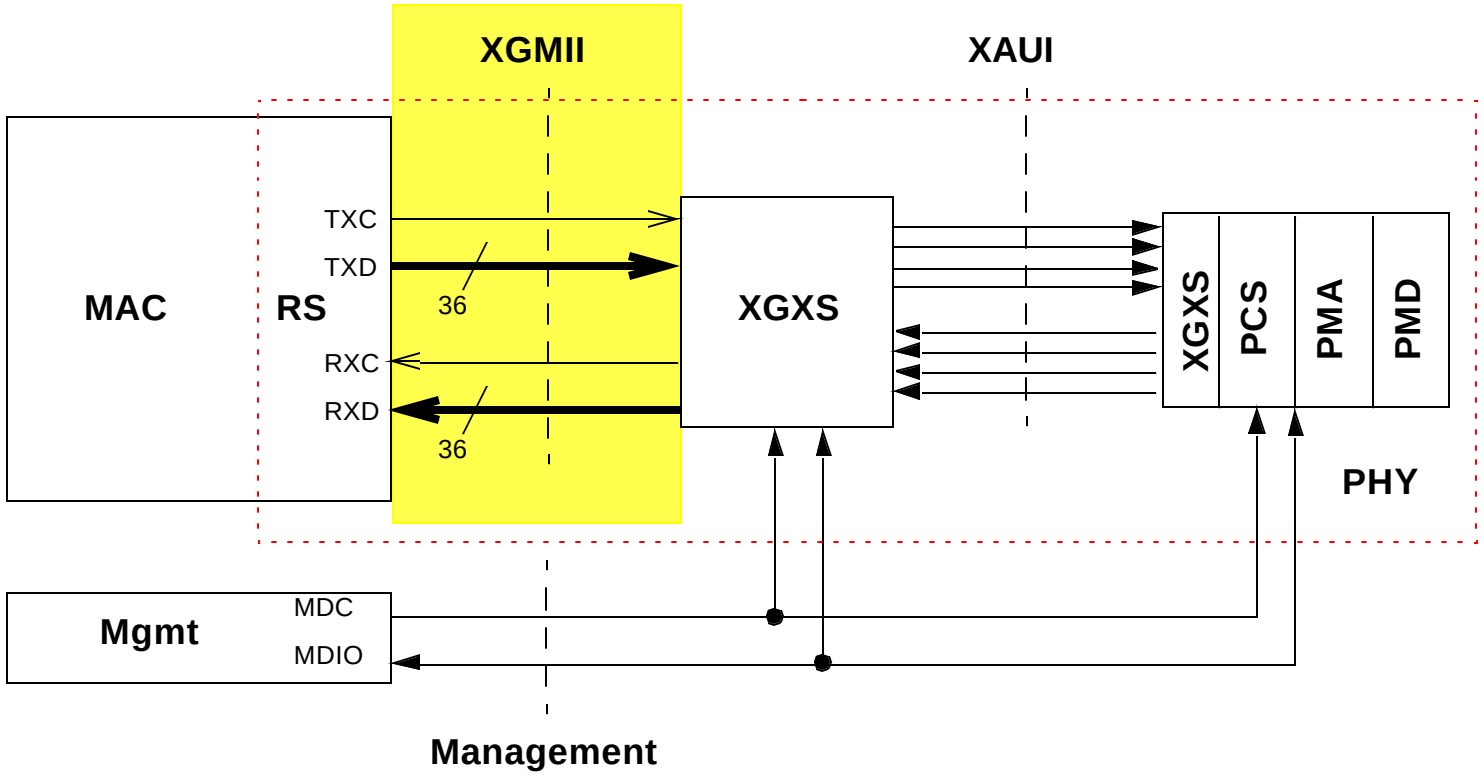
Goals and Assumptions

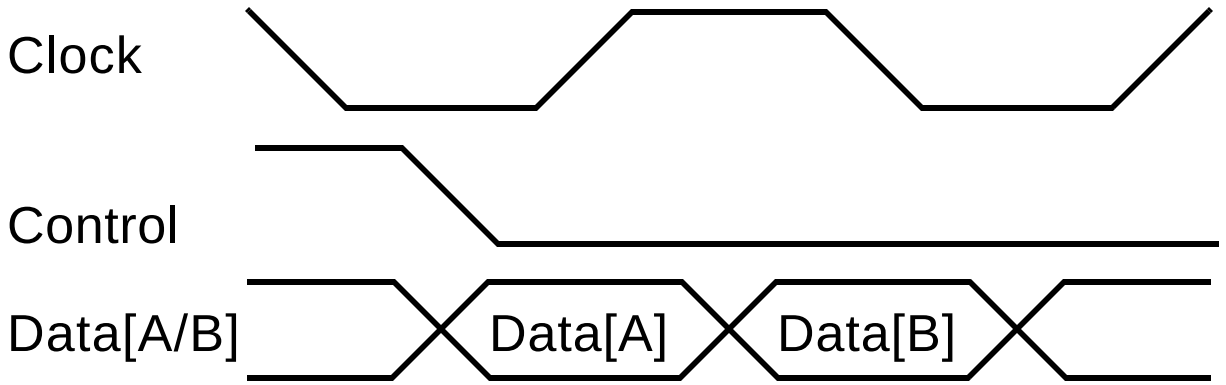
- Allow multiple PHY variations
- Provide a convenient partition for implementers
- Provide a standard interface between MAC and PHY
- Reference industry standard electrical specifications

Interface Locations



10 Gigabit Media Independent Interface

- 32 data bits, 4 control bits, one clock, for transmit
- 32 data bits, 4 control bits, one clock, for receive
- Dual Data Rate (DDR) signaling, with data and control driven and sampled on both rising edge and falling edge of clock



- 32 bit data paths are divided into four 8 bit “lanes”, with one control bit for each lane

10 Gigabit Media Independent Interface - Coding

- Use embedded delimiters rather than discrete signals
- Control bit (C) is “1” for delimiter and special characters
- Control bit (C) is “0” for normal data characters
- Delimiter and special character set includes:
  - Idle, Start, Terminate, Error
- Delimiters and special characters are distinguished by the value of the 8 bit data lane when the corresponding control bit is “1”
- Data (d) symbols are striped on lane 1, lane 2, lane 3, lane 0, etc.
  - Frames (packets) may be any number of symbols in length subject to minFrameSize and maxFrameSize

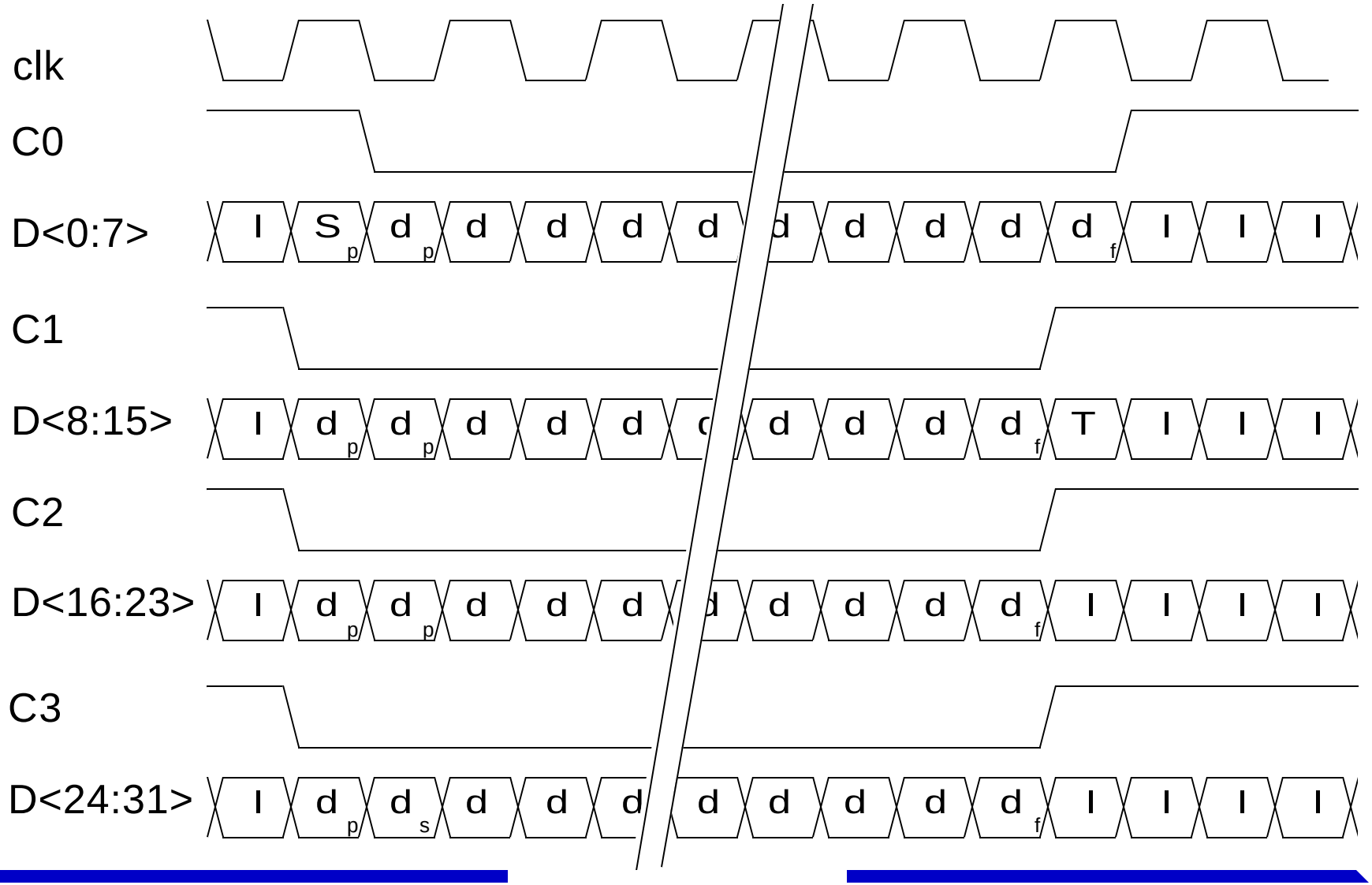
10 Gigabit Media Independent Interface - Coding

- Idle (I) is signaled
  - during the Inter-Packet Gap
  - when there is no data to send
- Start (S) is signaled
  - for one byte duration at the beginning of each packet
  - always on lane 0
- Terminate (T) is signaled
  - for one byte duration at the end of each packet
  - may appear on any lane
- Error (E) is signaled
  - when an error is detected in the received signal
  - when an error needs to be forced into the transmitted signal

10 Gigabit Media Independent Interface - Coding

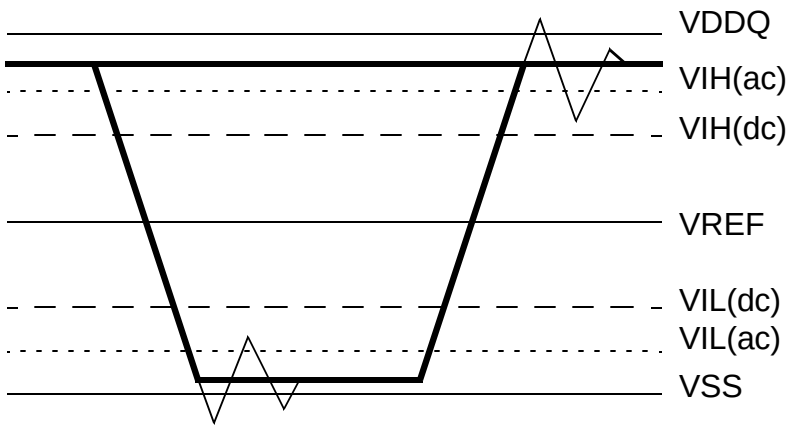
Shorthand	Name	Code Point (Control)	Code Point (Data)
I	Idle	1	0x07
S	Start	1	0xFB
T	Terminate	1	0xFD
E	Error	1	0xFE
d	Data	0	0x00 - 0xFF

10 Gigabit Media Independent Interface - Example



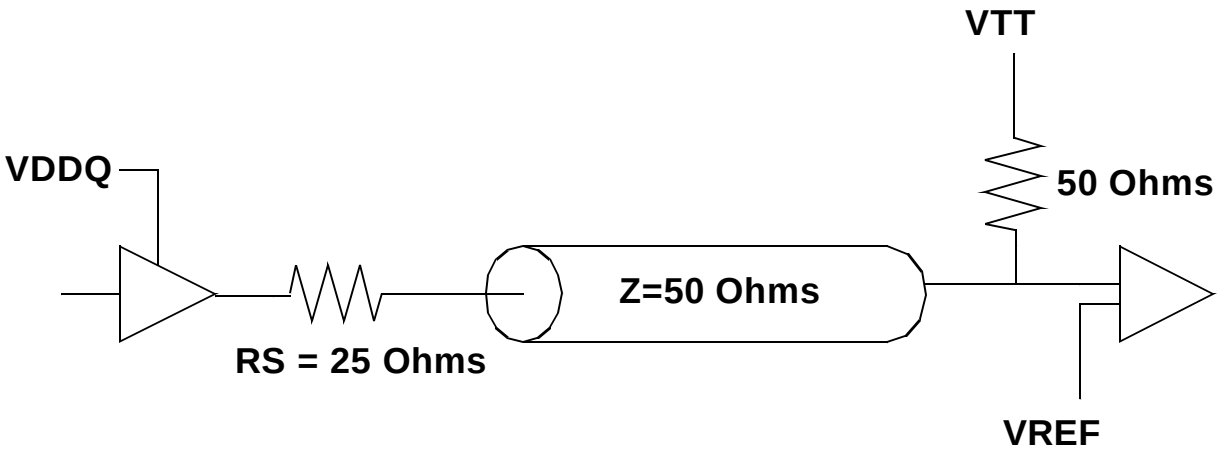
10 Gigabit Media Independent Interface - Electrical Characteristics

- Use Stub Series Terminated Logic for 2.5 Volts
  - SSTL_2
  - EIA/JEDEC Standard EIA/JESD8-9
  - Class I (8 ma) output buffers

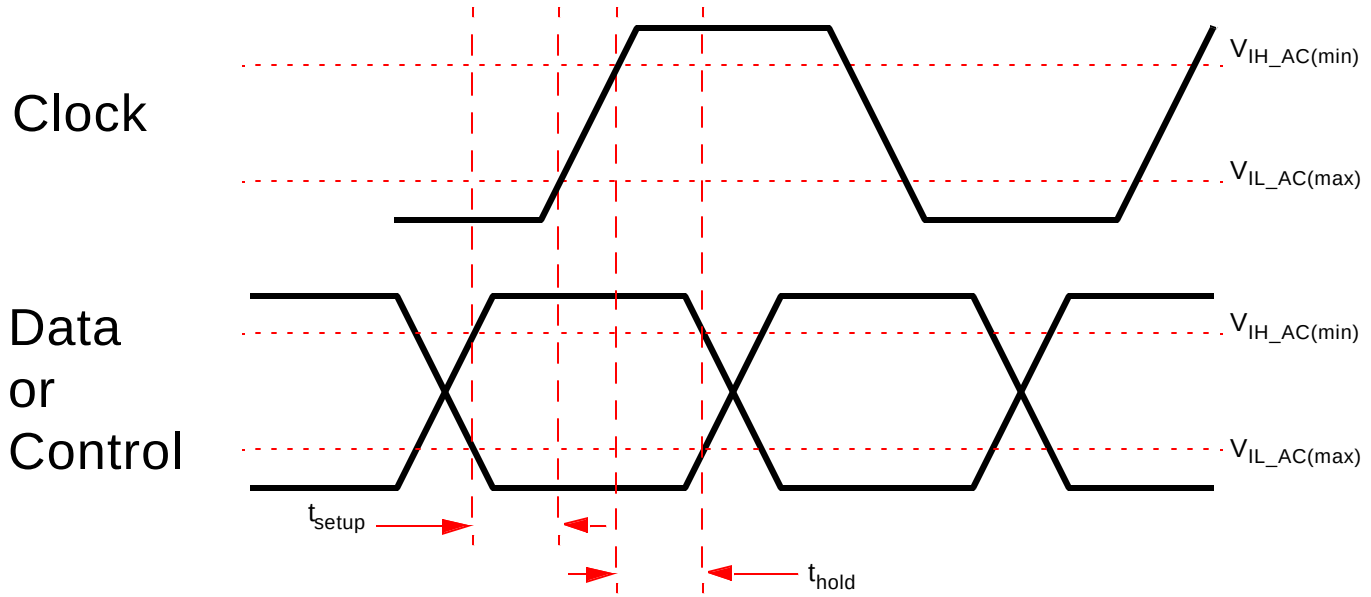


Symbol	Parameter	Min	Typ	Max
VDDQ	Supply Voltage	2.3	2.5	2.7
VREF	Reference Voltage	1.15	1.25	1.35
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04
VIH(dc)	dc input logic high	VREF+0.18		VDDQ+0.3
VIL(dc)	dc input logic low	-0.3		VREF-0.18
VIH((ac)	ac input logic high	VREF+0.35		
VIL(ac)	ac input logic low			VREF-0.35

10 Gigabit Media Independent Interface - Circuit Topology Example



10 Gigabit Media Independent Interface - Timing



Symbol	Driver	Receiver	Units
t_{setup}	960	480	ps
t_{hold}	960	480	ps

Summary

- The XGMII coding proposal is stable
- The EIA/JEDEC SSTL_2 standard can be referenced for the XGMII electrical specification
- The timing proposal presented herein is a starting point for further discussion