50.3.8 WIS Serial Test Patterns

The serial test patterns allow the 10GBASE-W family of PMD devices described by Clause 52 to test for compliance while in a system environment. Two patterns have been defined for testing: a fixed square wave pattern and a framed mixed frequency test pattern. The patterns may be implemented at a bit or frame level and may be used for transmitter testing. The receiver shall have the ability to synchronize to the Mixed Frequency Test Pattern and report bit error rate for the payload back to the user. The receiver is not required to synchronize to and analyze the square wave pattern.

50.3.8.1 Square Wave Test Pattern

The square wave test pattern generated by the WIS block shall be a continuos, repeating pattern of 00FFh. This creates a square wave with a frequency of 622.08 MHz +/- 20ppm.

50.3.8.2 Mixed Frequency Test Pattern

The mixed frequency test pattern is based upon the pattern defined by ITU-T specification O.172 *Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH),* with a CID pattern as described by ITU-T specification G.957 *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy.* The pattern was selected because it re-uses the existing framer combined with a low gate-count PRBS generator and a CID pattern to stress the lock range of the receive CDR circuitry. The CID pattern overwrites the default value for the last nine Z0 bytes in the section overhead since this area is not scrambled during normal operation of the WIS. The CID alternates an a frame by frame basis from all one's (light on) to all zero's (light off). The PRBS generator is a 2^{23}-1 bit generator, as defined by ITU recommendation O.151, which is inserted into the SONET payload envelope (SPE) at the transmitter. The receiver shall extract the SONET overhead as defined in clause 50 and synchronize to the PRBS within the SPE. Once synchronization has occurred, bit errors can be detected and reported. External text equipment shall confirm every bit in the test signal structure (TSS).

The WIS shall function as described by the remainder of Clause 50 with the exception of the CID pattern in the last nine octets of the Z0 byte location, and the use of a PRBS as the data source for the SPE (in place of data from the PCS). The SONET frame is scrambled as defined by this clause when operating in test pattern mode.

50.3.8.2.1 Test Signal Structure

The Test Signal Structure (TSS) is defined to be two SONET frames in length. The CID shall alternate from all zeros in the first frame to all ones in the second frame. The PRBS section shall start at a reset value provided by the MDIO (TBD) in the first byte of the payload. I.e. at the location immediately following fixed stuff in the path overhead of the frame. The PRBS generator shall fill the SONET SPE for the first frame with the output of the PRBS starting at the reset value. The second SPE shall be generated from the PRBS starting from the same reset value with the output of the PRBS inverted. The WIS frames shall include the POH and fixed stuff as defined by Clause 50.

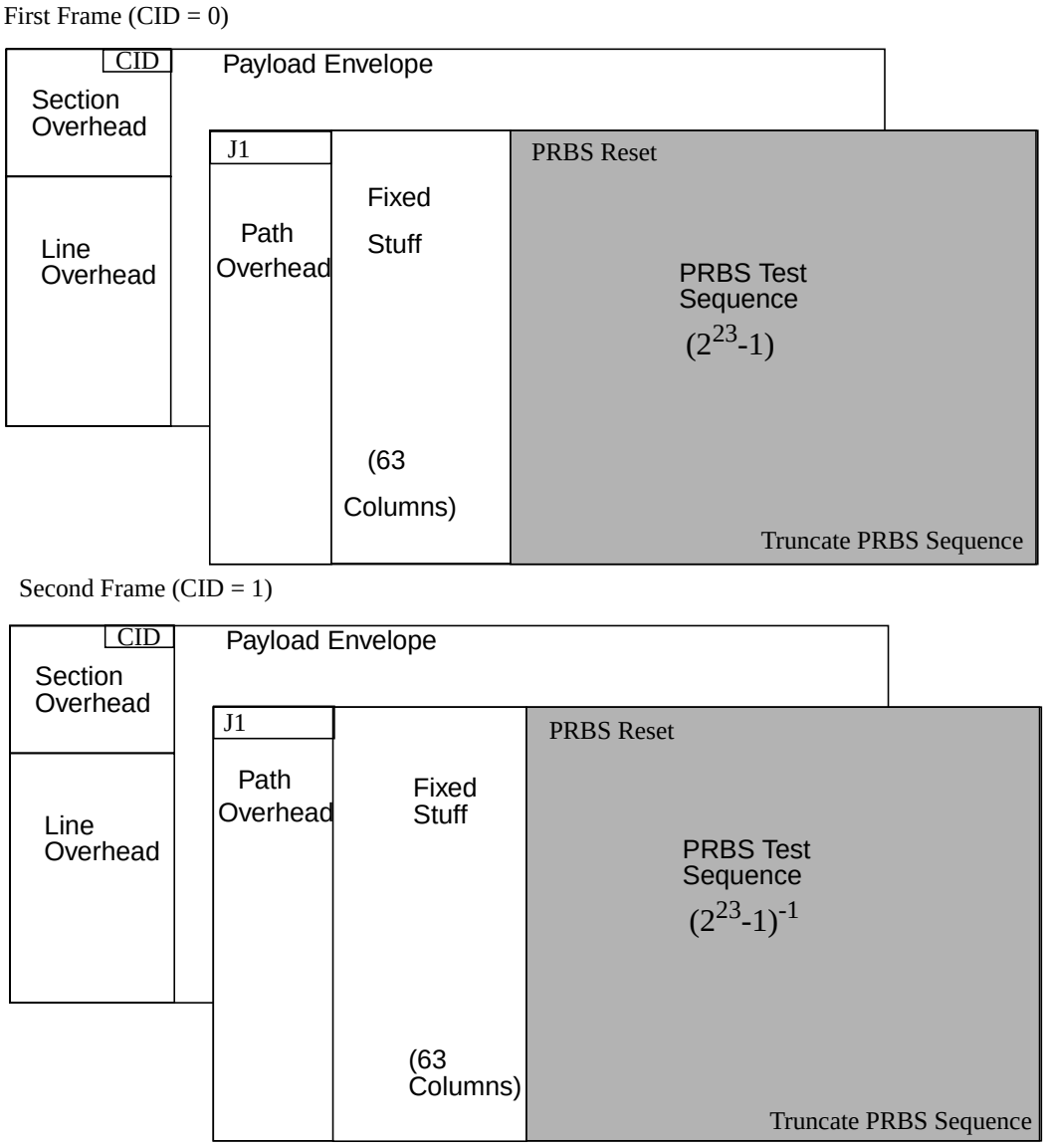
The synchronous mapping of the payload to the start of the SPE as defined in Clause 50.3.2.2 places the J1 byte in the octet immediately following the CID pattern. To improve the efficacy of the CID, the J1 byte should be programmed to a fixed value which, after scrambling, provides optimal stress to the transmitter and receiver. The J1 byte value is provided by the MDIO (TBD). The default value of 0x89 shall be used for the J1 byte.

Editors' Note: *To be removed prior to final publication*
The value for the K1, K2 and G1 bytes must be fixed. This ensures a predictable, repeatable value for every bit in the TSS.

For SONET test equipment and for the WIS receiver, there is no requirement to process the Z0 bytes. The area of interest created by the CID is in the first bits in the SPE following the CID, i.e. the J1 byte. The use of a SONET tester is not recommended under this strategy since PRBS re synchronization is required for every frame. While the BER could be predicted, it is a non-optimal solution.

For bit error rate testers, it is necessary to allocate two full frames of memory (2.5 Mbits) to hold the pattern containing both CID values. Such a tester would provide the capability to monitor the entire frame including the CID pattern.

Figure 1: TSS For 10GBASE-W Signals

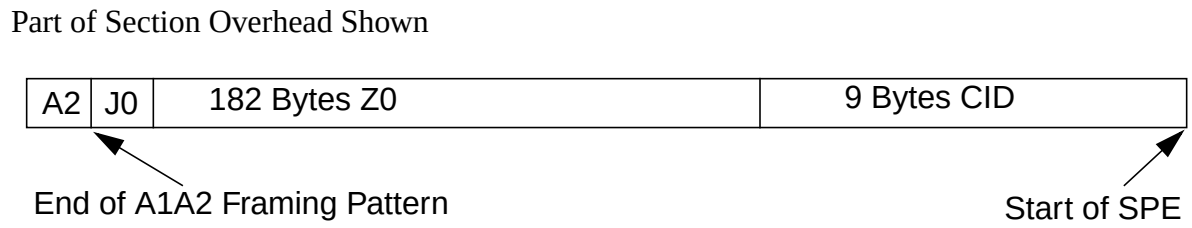


50.3.8.2.2 Continuous Identical Digits (CID)

The CID pattern is derived from G.957. The shortcoming of patterns defined by G.957 is that the pattern is not a regular SONET frame. This has an impact on the WIS block's ability to generate abnormal frame structures. The pattern's abnormal structure also increases the time required to achieve synchronization at the receiver, which has a direct impact on test time. The addition of the CID provides additional stress to the lock range of the CDR in the receiver since there are no bit transitions during this period.

The CID shall be inserted into the Z0 byte location of each SONET frame (since the Z0 byte location is not scrambled). Refer to Figure 1 on page 3 for a view of the CID signal structure.

Figure 2: CID Signal Structure



The 9 bytes of CID shall alternate in consecutive frames. The first frame shall contain 72 bits of all zero's, the second frame shall contain 72 bits of all 1's etc. There is no requirement to test the contents of the Z0 byte in the receiver. If the CID pattern resulted in eye closure at the transmitter, or an error at the receiver, it would be reflected in a bit error detection in the PRBS of the SPE.