

# **Returnloss Measurements and Simulations**

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# Causes

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- **Driver / Receiver:**

- Total capacitance: 1.4pF+
  - Driver / Receiver = 500fF+
  - Pad / ESD = 900fF+

- **Package:**

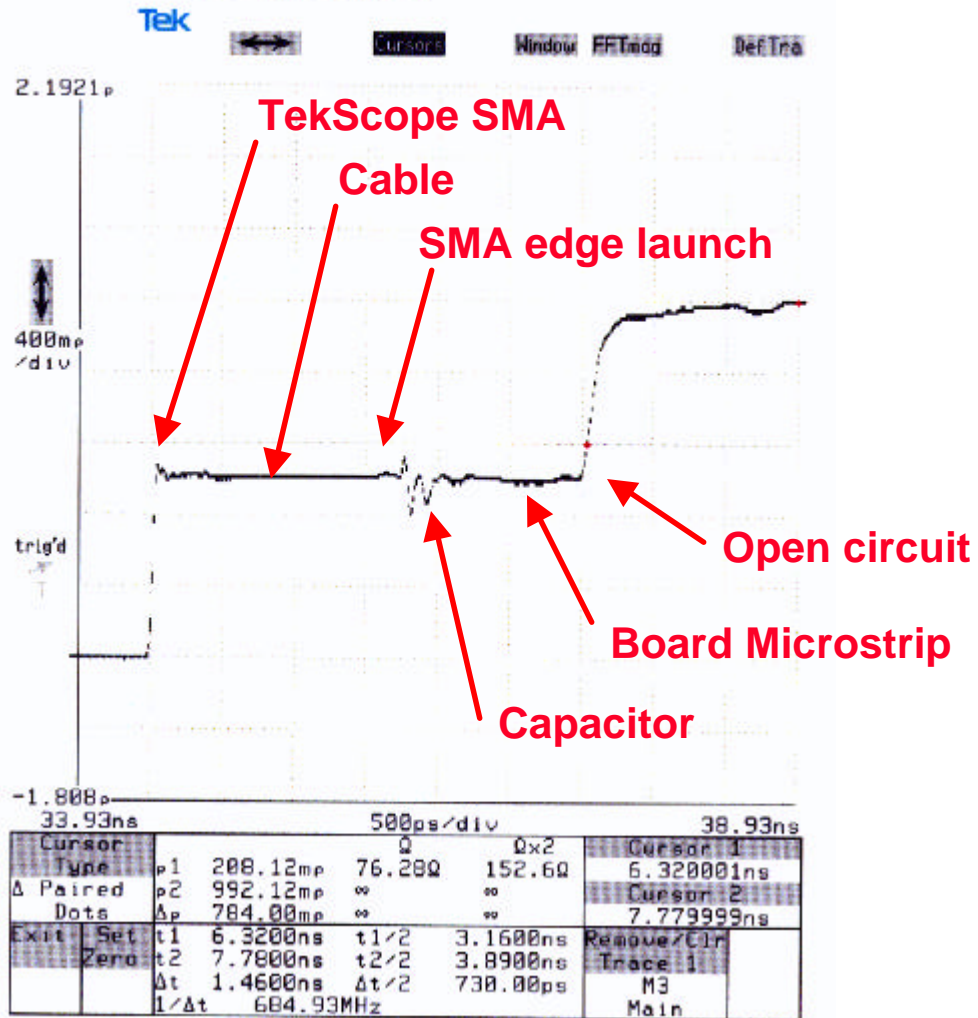
- Package was designed with 100 Ohm differential lines and short bondwires (1mm)
- However, package-only returnloss sims already show <10dB returnloss above 2GHz (assuming ideal 50 Ohm terminations inside/outside package)

- **Board:**

- Board has 50 Ohm traces, but:
- Via underneath BGA ball adds about 1.5pF load reducing impedance
- Socket adds significant load (risetime goes from 100ps to 130ps with socket), but even soldered down part still has problems
- AC decoupling caps cause significant impedance change
- Current board has poor edge launch SMA

# Measurements (time)

11801C DIGITAL SAMPLING OSCILLOSCOPE  
date: 23-MAR-25 time: 18:02:13



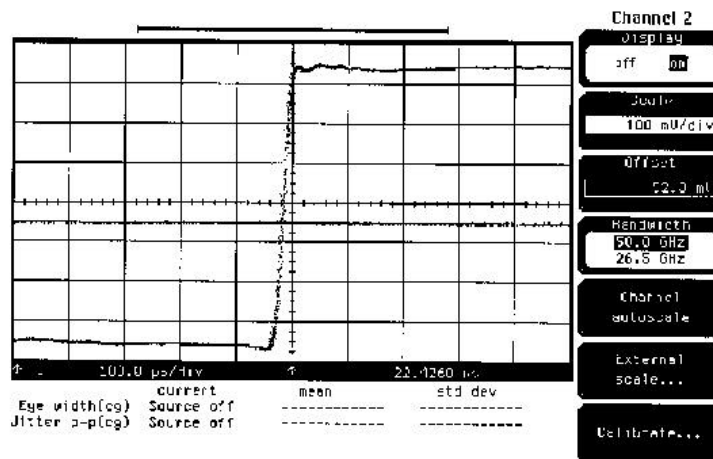
- **TDR – Board only**

- 50ps rise time
- contains: scope SMA, cable, SMA edge launch, decoupling cap and board trace.
- Shows poor SMA edge launch and effect of decoupling capacitor
- 500ps /div

# Measurements (time)

Acquired: 02 JUL 2001 11:16:23.90

Printed: 02 JUL 2001 11:18:23

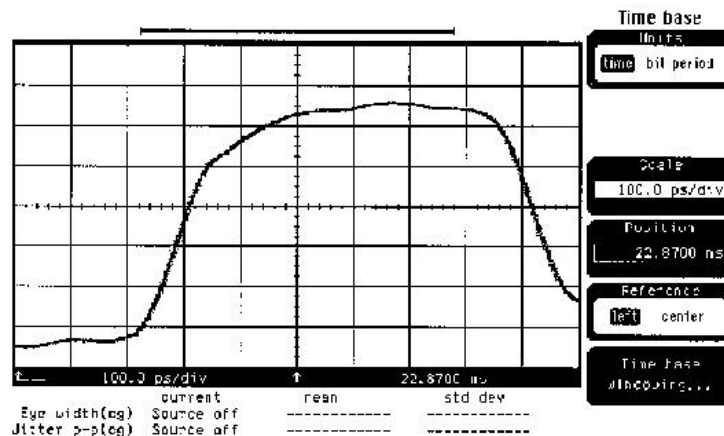


- **TDT – Bare Substrate soldered**

- In through tdp, out through tdn
- 100ps / div plots
- Upper left: input = 20ps rise time
- Bottom left: TDT with bondwire
- Bottom right: TDT with solderdot
- Same reduction in slope

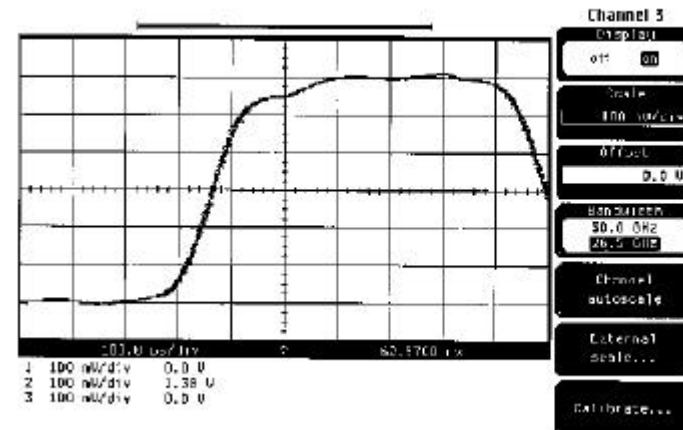
Acquired: 02 JUL 2001 11:16:28.90

Printed: 02 JUL 2001 11:16:28



Acquired: 02 JUL 2001 11:40:27.10

Printed: 02 JUL 2001 11:40:37



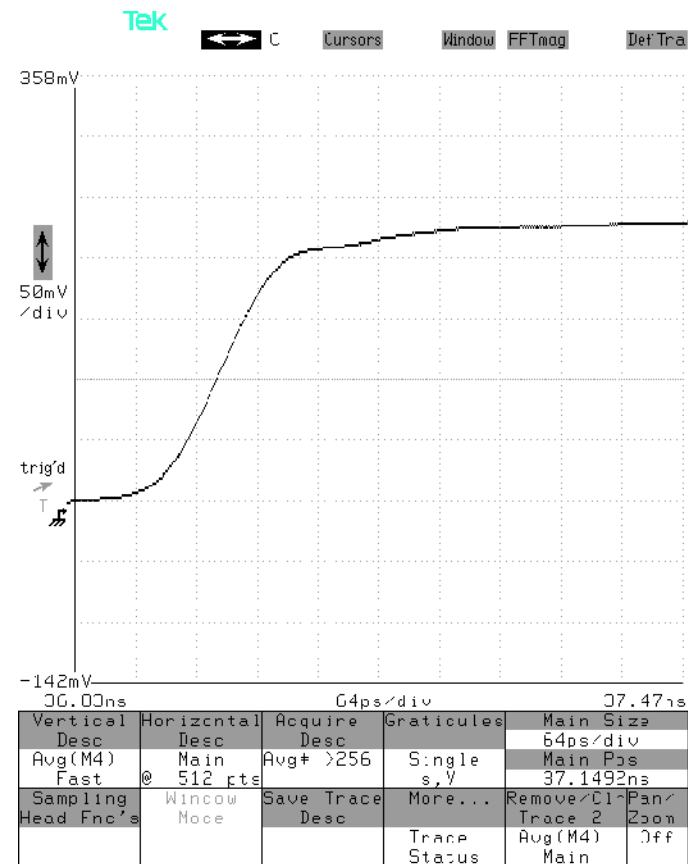
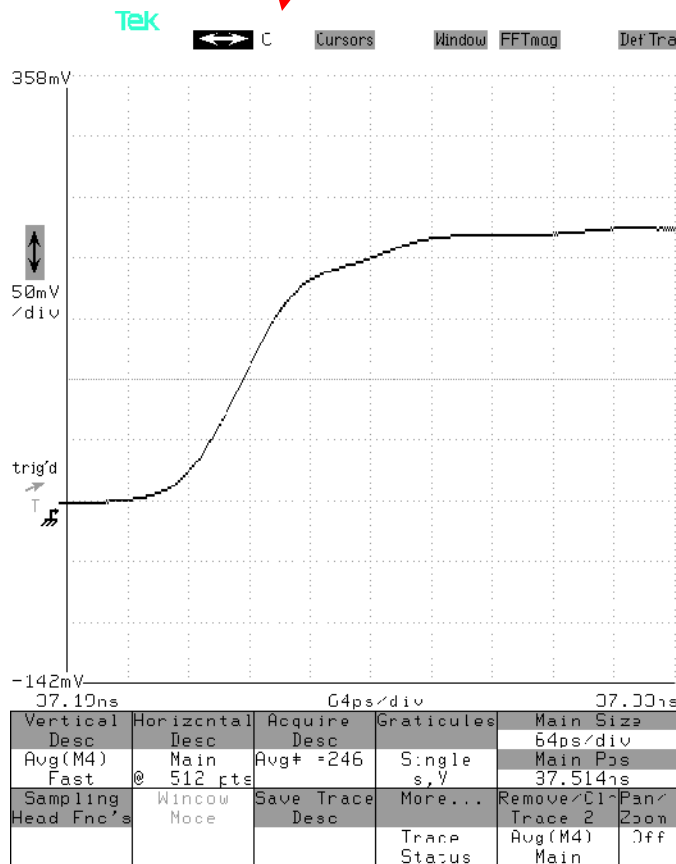
# Measurements (time)

Solderdot short

Bondwire short

- TDT – Bare Substrate soldered

- In through tdp, out through tdn
- 64ps / div plots
- Now with TekScope



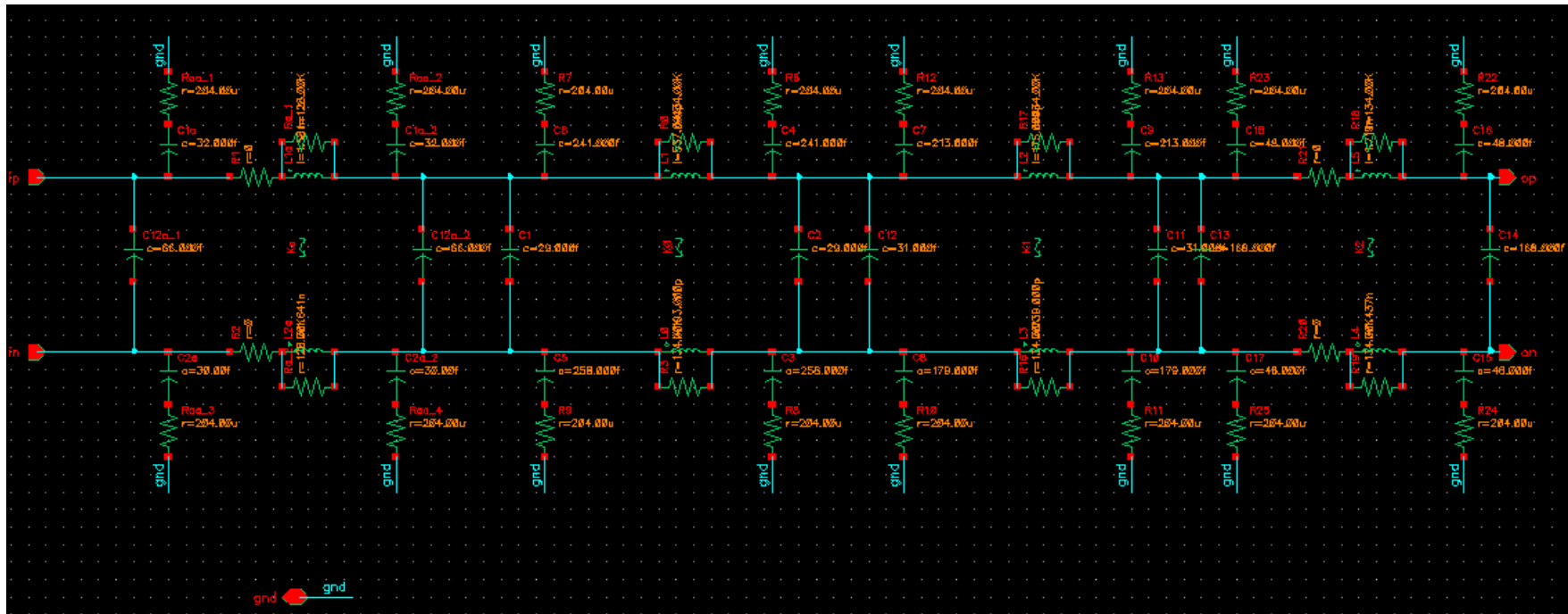
# Simulations

- **Several simulations**

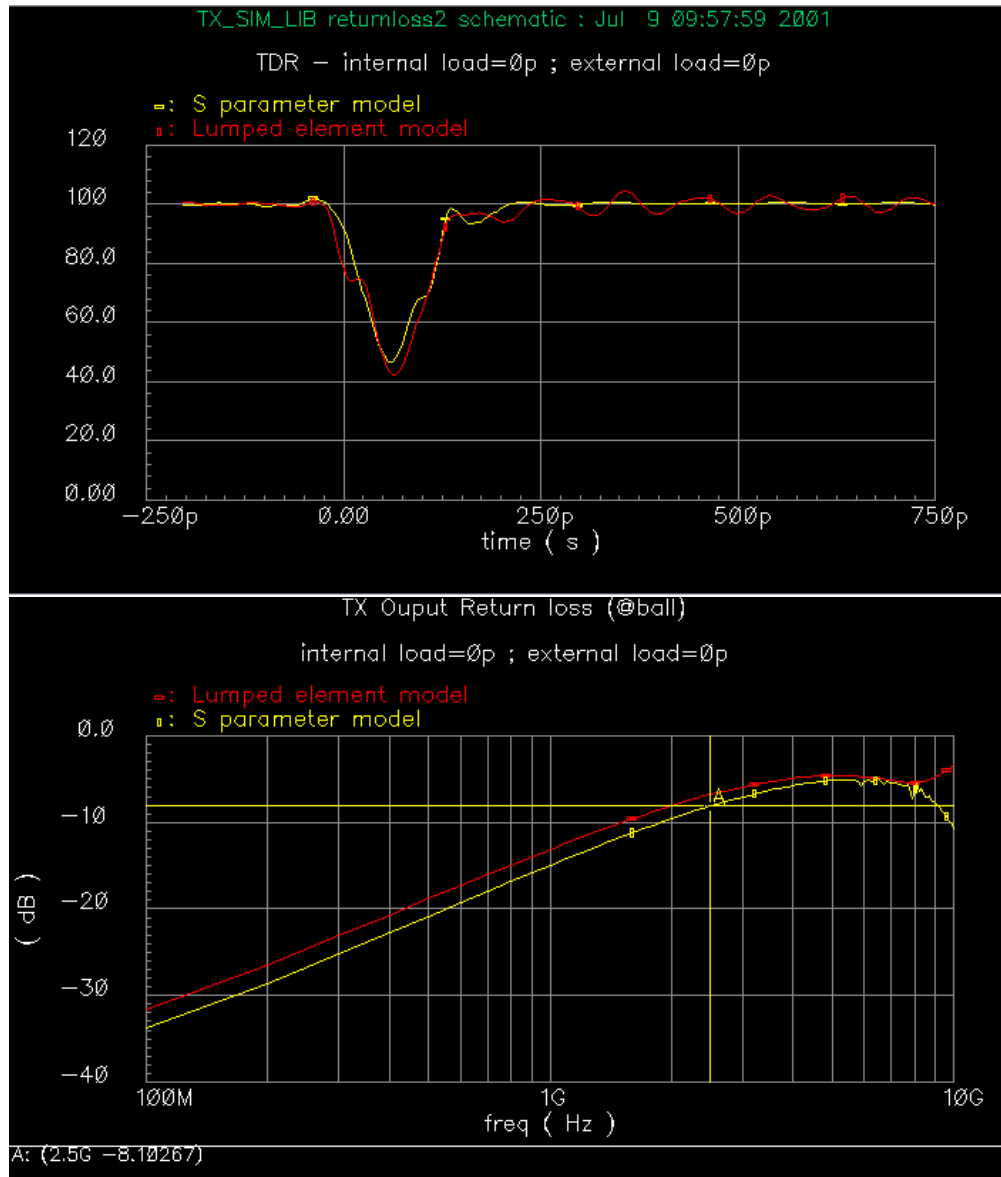
- TDR Simulations
- Returnloss simulations
- Transient (pulse response) simulations

- **Models**

- S parameter model (3D – HFSS)
- Lumped element model (fitted)



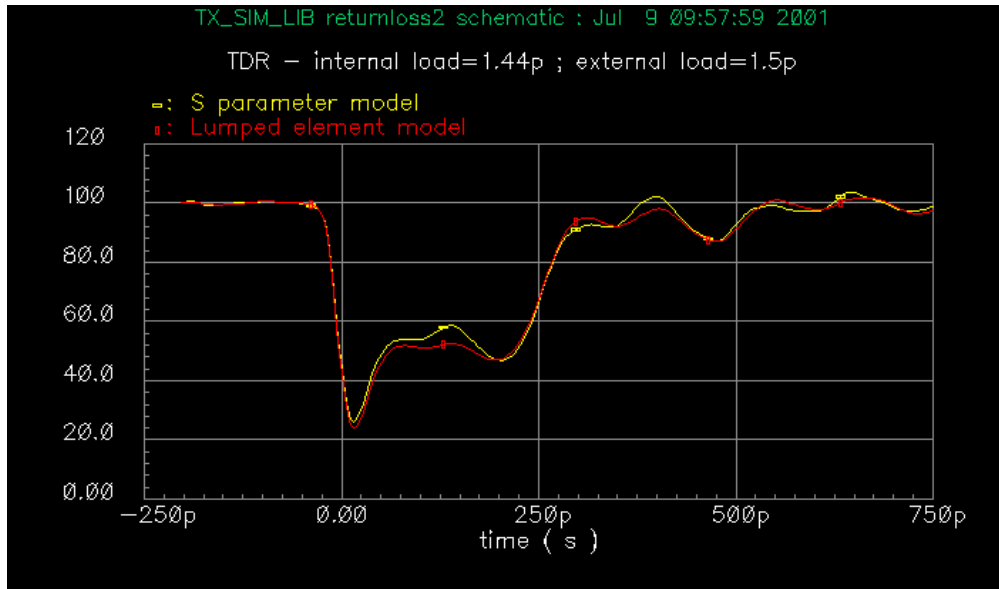
# Simulations (TDR / RL)



- **Package only**

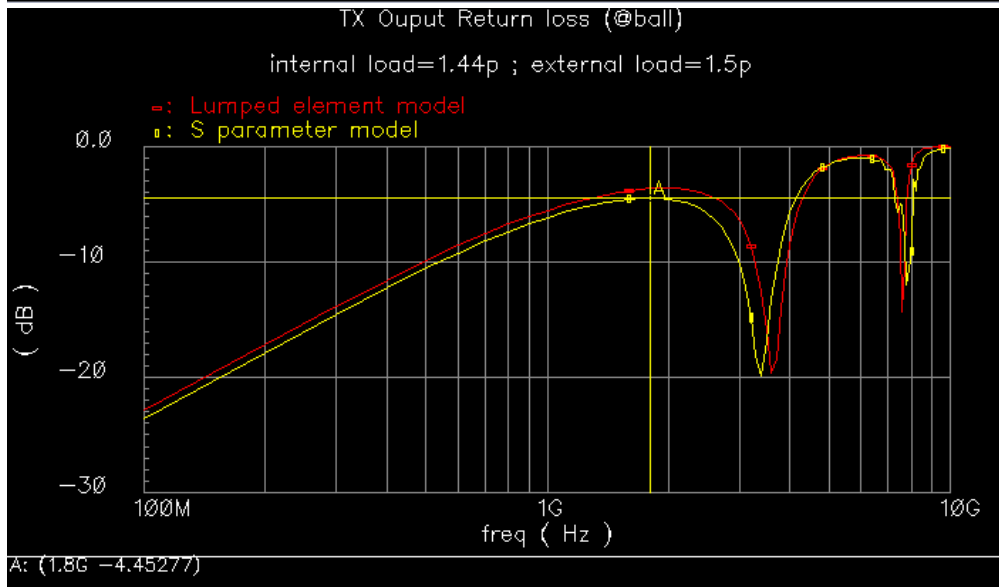
- Always fully differential simulation set-up
- Always proper 100 Ohms source / load terminations
- Internal and external capacitances varied
- Here: no capacitive loads
- Impedance drops below 50 Ohms
- Returnloss @ 2.5GHz = 8.1dB

# Simulations (TDR / RL)



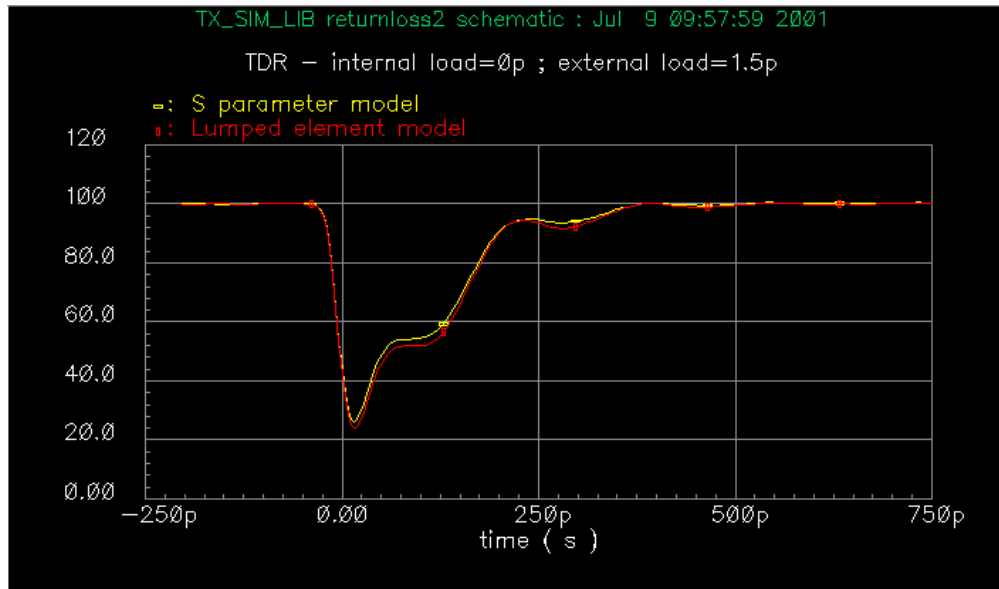
- **Full Capacitive load**

- Internal = Pad + Driver
- External = Via + Trace
- Impedance drops below 30 Ohms
- Returnloss @ 1.8GHz = 4.5dB
- TDR pulse is over 2x wider



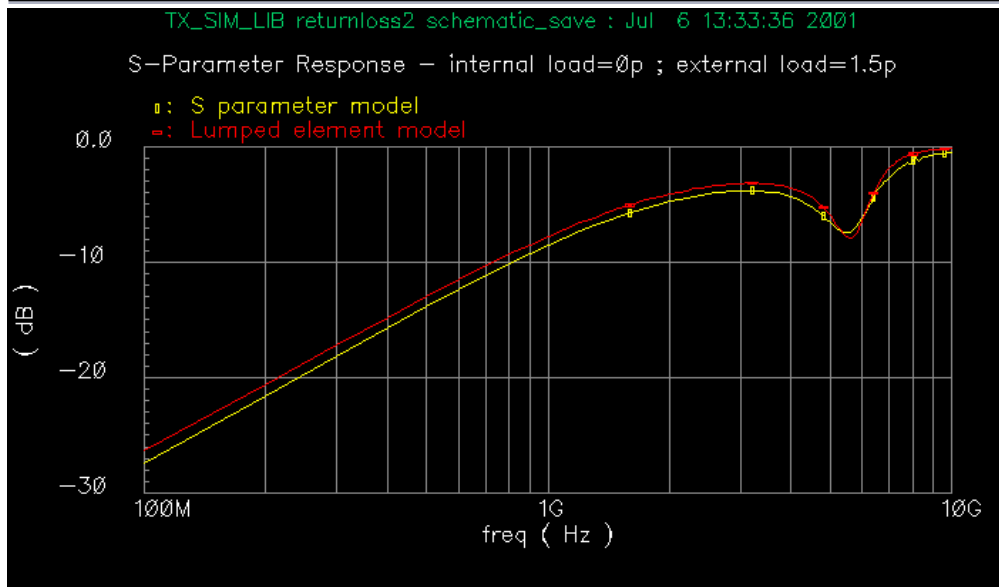


# Simulations (TDR / RL)

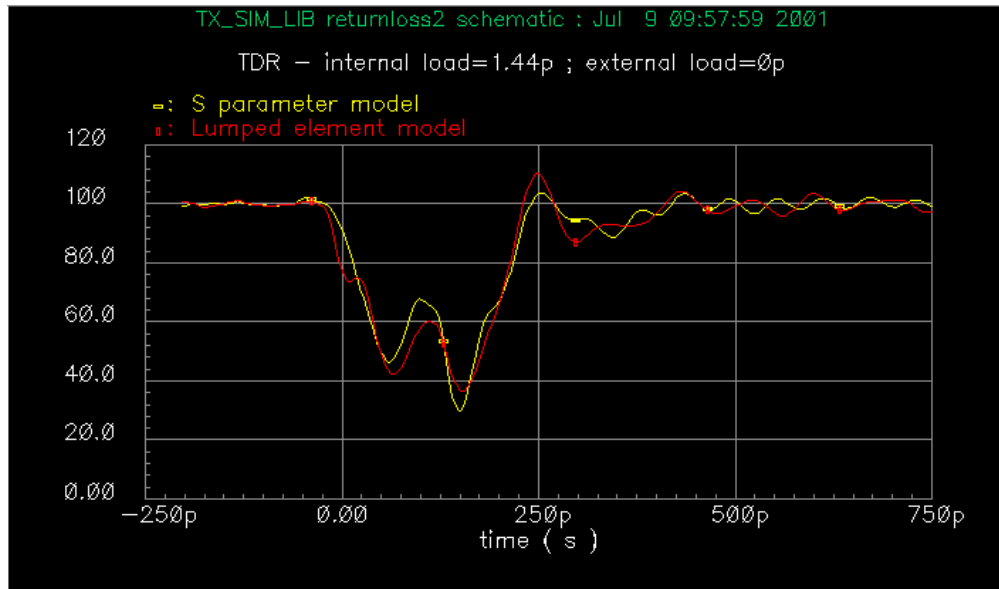


- **External load only**

- Impedance drops below 30 Ohms
- Returnloss @ 2.5GHz = 5dB
- Internal load does not effect returnloss drastically when external load is present, but the TDR pulse is much shorter when no internal capacitance is present

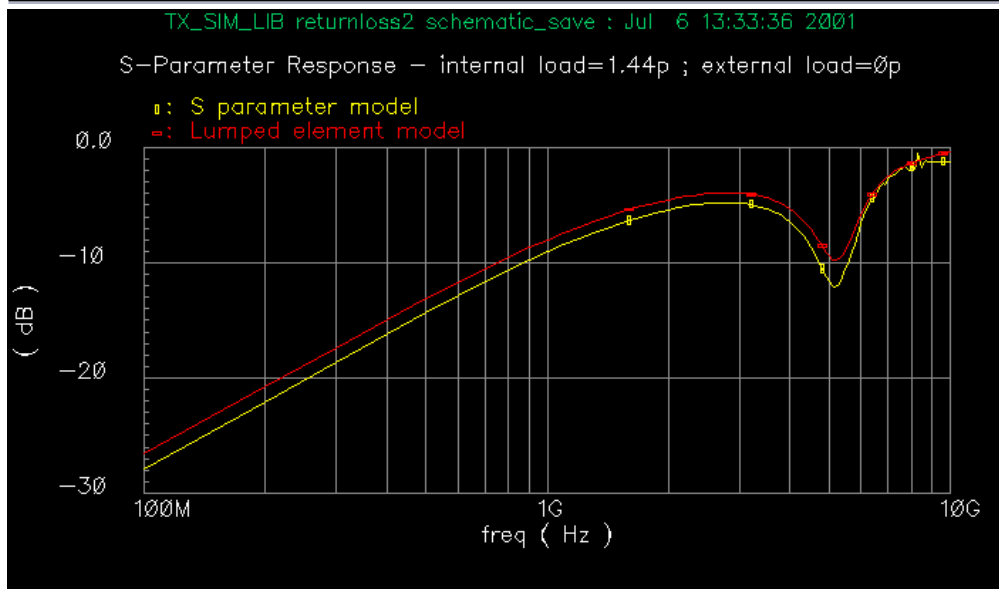


# Simulations (TDR / RL)



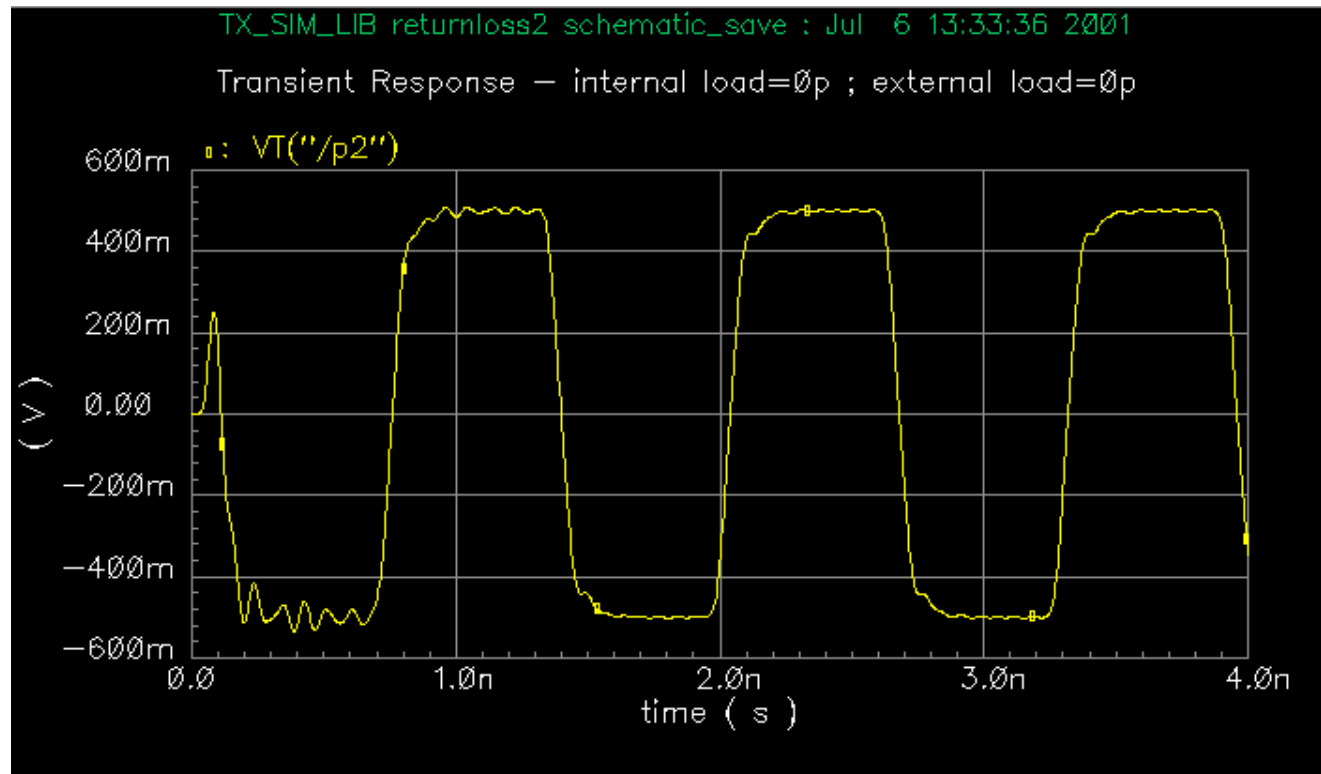
- **Internal load only**

- Impedance drops below 40 Ohms
- Returnloss @ 2.5GHz = 6dB
- Internal load still has significant effect when no external load is present, but TDR has more distinctive 'double' bump



# Simulations (time)

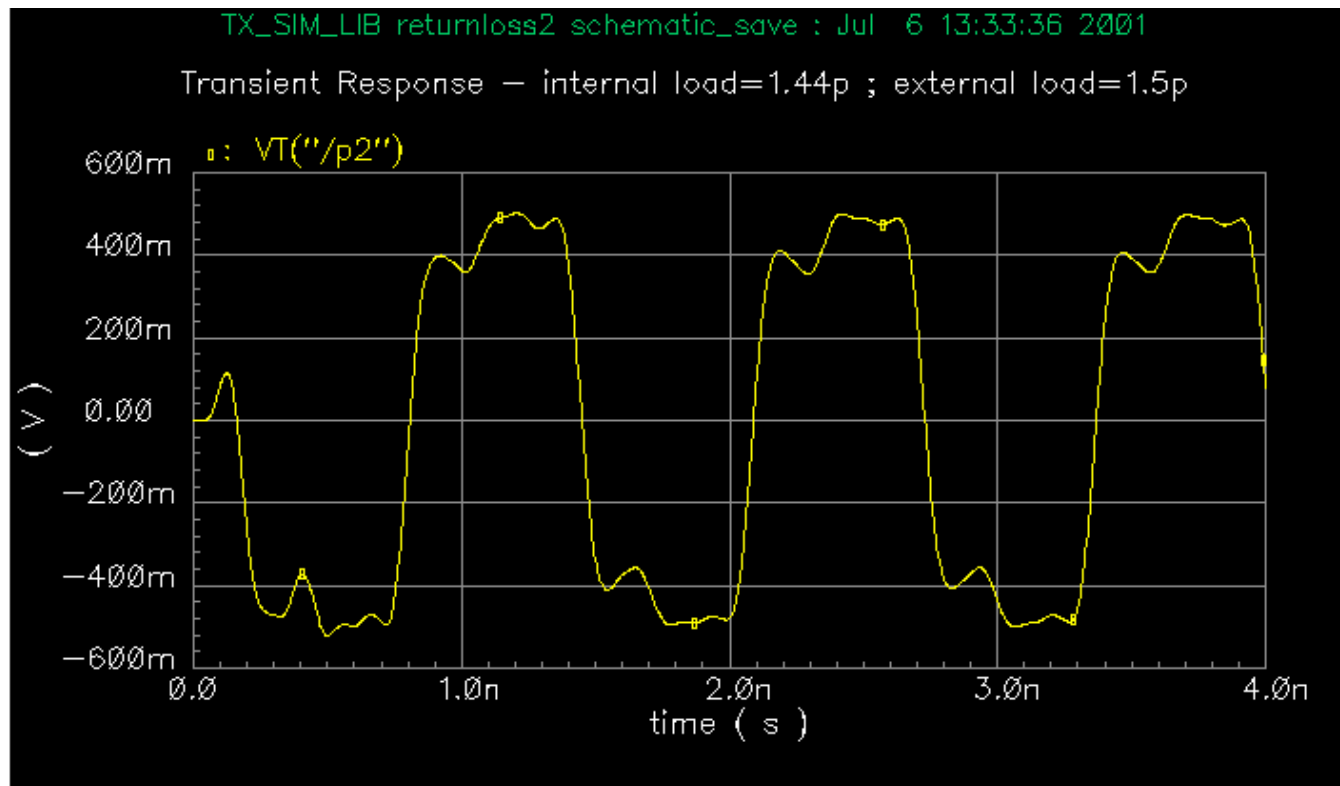
- **Package Only**
  - Output waveform with '111000111' pattern
  - Very small reflection noticeable at the transitions.



# Simulations (time)

- **Full capacitive load**

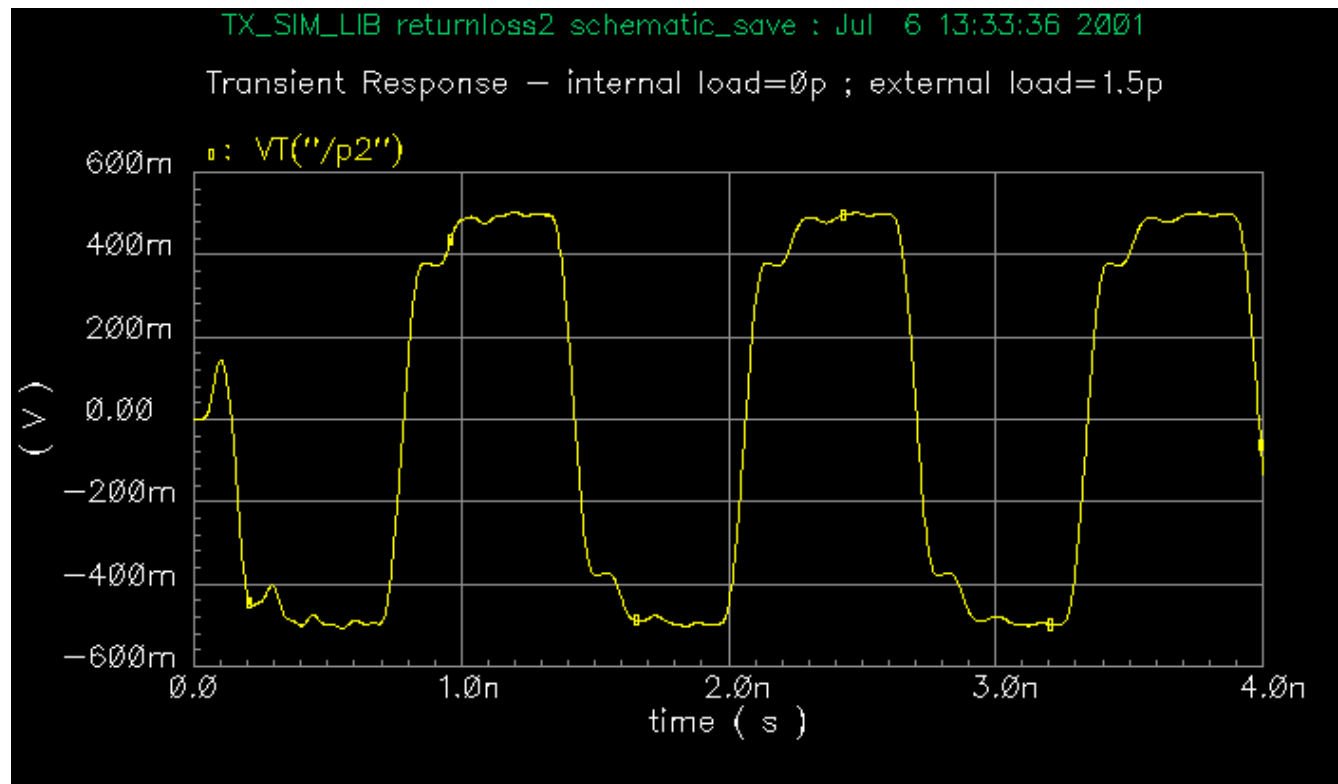
- Output waveform with '111000111' pattern
- Significant reflection (>15%) at every transistion, nearly 1 UI long
- Reflection is more pronounced than in TDR and output measurements



# Simulations (time)

- **External load only**

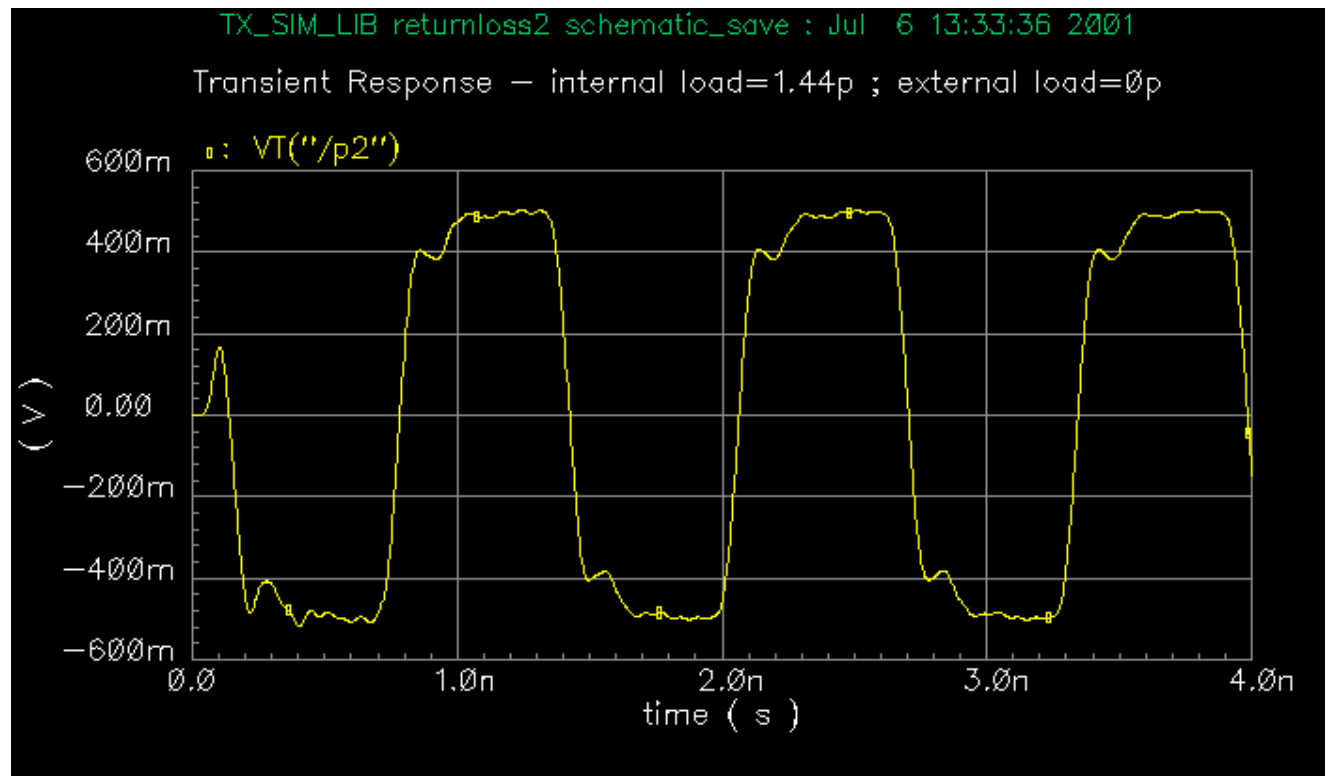
- Still significant reflection ( $>15\%$ ) at every transistion, but shorter than with internal capacitance
- Flat / Step-like reflection resembles output measurements for soldered down part.



# Simulations (time)

- **Internal load only**

- Still significant reflection ( $>15\%$ ) at every transistion, but shorter than with full capacitive load
- Difference between internal and external load not significant



# Simulations (time)

- **Reduced capacitive load**
  - Estimate of capacitive reduction in pad and on board
  - Very little improvement compared to full capacitive load

