Clause 50 and 51 Status

Tom Alexander
Clause 50 Editor

Cl. 50 Comment Resolution Status

- 10 comments on D3.1
  - 1 TR, resolved and signed off
    - Change “jitter test patterns” to “test patterns”
  - 6 technical, all resolved
  - 3 editorial, all resolved
- Relatively minor changes to Clause 50
  - New jitter pattern for pseudo-random mode
    - As per warland_1_0701.pdf
    - Change from D3.1: replace fixed SPE contents with PRBS, restarted every 2 WIS frames
  - Minor editorial changes

Cl. 51 Comment Resolution Status

- 10 comments on D3.1
  - 3 TRs, resolved and signed off
  - 5 technical, all resolved
  - 2 editorial, all resolved
- Few technical changes to Clause 51
  - Voltage levels for auxiliary signals on XSBI changed
  - Long discussion on +/- 20ppm clock tolerance
    - Informative note added clarifying the change from 100 ppm to 20 ppm
  - Discussion of bit ordering on XSBI

Change to XSBI signals – Cl. 51

- Changed PMA_SI and Sync_Err voltage family to EIA/JESD8-B as per comment
  - Originally set at LVCMOS
  - Comment that this doesn't match the industry standard (SFI-4)
  - EIA/JESD8-B: "Interface Standards for Nominal 3V / 3.3V Supply Digital ICs"
    - Compatible with both LVCMOS and LVTTL (LVCMOS and LVTTL are both referenced within this specification)