Low Voltage Signaling for Higher Performance and Lower Cost

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Abstract

- **10 Gigabit Ethernet switch may have several hundreds I/O associated with XGMII ⇒ EMI.**
  - Reduce Amplitude, power of 2 improvement.
  - Impedance control driver and 50 Ω TL .
- **Reduce Power Dissipation**
  - Reduce Amplitude.
- **Terminated Logic for XGMII**
  - SSTL ~ 1.25 V swing
  - HSTL ~ 0.75 V swing .

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Why Reduce the Signal Amplitude

- XGMII with 74 I/O operating at 1250 mV of swing will generate significant EMI and SSN.
- Reducing the signal swing reduces EMI and SSN.
- Significant amount of money is spend on EMI Means: real metal enclosure and etc.
- Lower PD typical SSTL2 ~25mW and ~15mW for HSTL.
- Lower slow rate ⇒faster bit rate.
- Compatible with advance CMOS sub 0.15 um logic family.

Background on HSTL

- **HSTL ⇒ High Speed Transceiver Logic EIA/JESD 8-6.**
- **A 1.5 V output buffer supply voltage based.**
- **Developed for flexibility, compatibility with most IC process and voltage independent.**
- **Typical swing is about 750 mV.**
- **It has 4 classes:**
  - Symmetrical parallel terminated loads, VTT=1/2VDDQ.
  - Class II Externally source series term., VTT=NA.
  - Class III Asymmetrically || terminated load, VTT= VDDQ.
  - Class IV Symmetrical Double || terminated, VTT=VDDQ.
- **It can also be made differential.**

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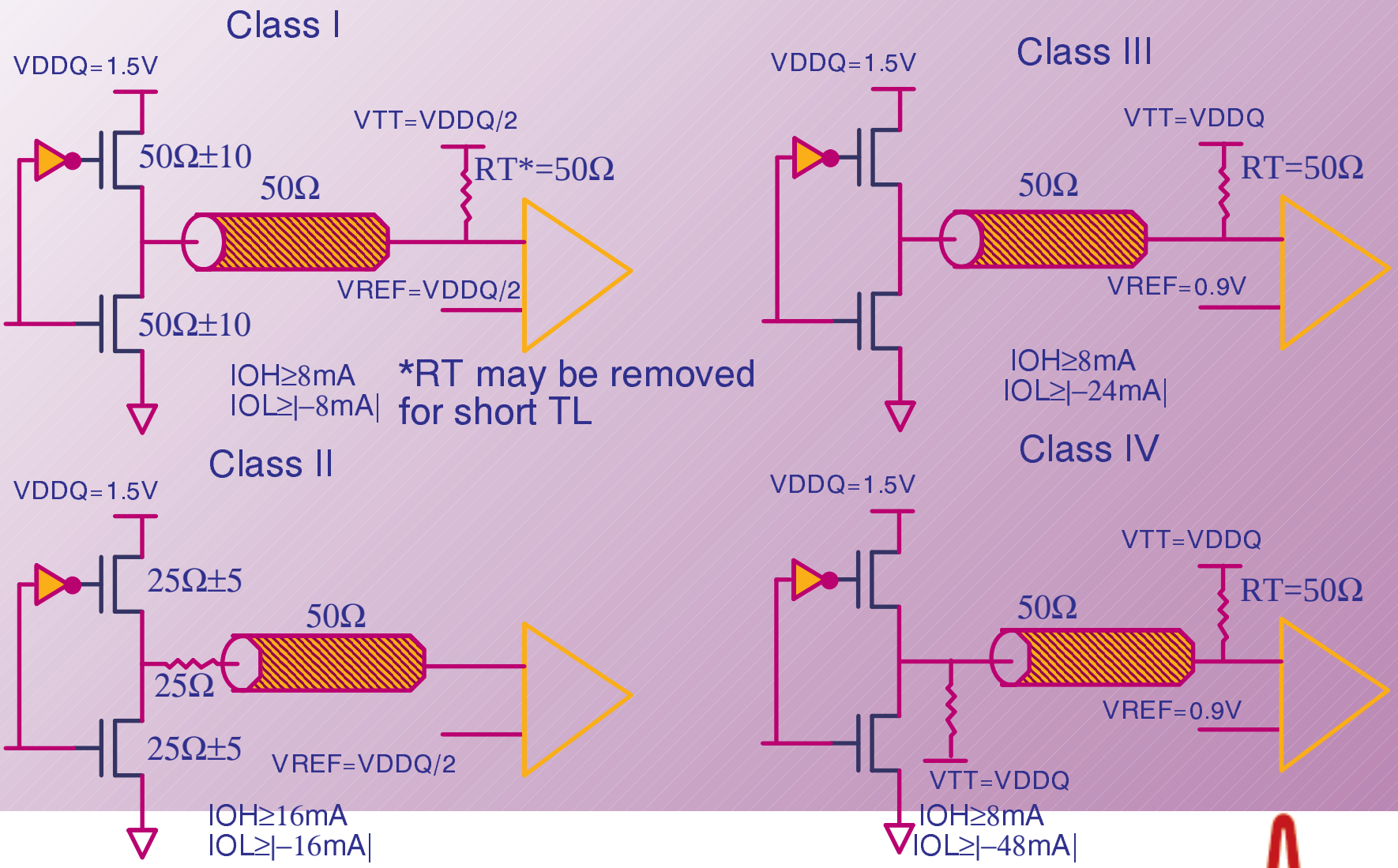
Schematics of HSTL Classes



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Recommendation

- We adapt HSTL Class I with optional load termination for XGMII and control signals.
- Optional load termination may be require for drivers with poor impedance control or long >6" PCB traces.
- HSTL Class I will reduce power by about 40% compare to existing SSTL2.
- HSTL Class I will be compatible with future generation of CMOS as MDIO controls will have long life.
- HSTL with 0.75 V swing is even suited to operate the XGMII at 624 Mb/s with careful design.

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