Clause 46 Issues

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November 8, 2000

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- XGMII Electrical
- XGMII data stream sequences
  - Delimiter robustness
  - Starting sequence options
  - Generation of DATA_COMPLETE
  - Generation of DATA_NOT_VALID
- Delay specifications

Logic type/level

- There is no standard for HSTL at 1.8 volts
- TF only left other parameters TBD
- XGMII electrical application
  - Near term chip-to-chip
  - I/O available in FPGA and quick turn ASIC
  - Should be a standard I/O, not custom
- Class I, 1.5 volt HSTL added under editor's note

Electrical Work items

- XGMII Electrical Interface Options
  - Develop 1.8v specifications
  - Reference Class I, 1.5v HSTL & select options
  - Revert to SSTL per 802.3ae/D1.0
- Tasks
  - Logic parameters
  - Termination
  - Timing

Motion

- Move to select 1.5v HSTL for the XGMII electrical specification per EIA/JESD8-6.
- M: Pannell, S: Dineen
- Y:27, N: 0, A:10

Motion

- Move to accept HSTL Class I per EIA/JESD8-6, Aug 1995.
- M: Lynch, S: Dineen
- Y: 37, N: 0, A: 2

XGMII Sequence

- Delimeter robustness
  - Leave it to the PCS?
  - Add checking to XGMII?
    - Idle, Start; Terminate, Idle
- Preamble options
  - Optionally reject frame if:
    - Start not aligned to Lane 0
    - Preamble length
    - Preamble contents
    - SFD not aligned to Lane 3

MAC Service Interface

- XGMII doesn't have RX_DV equilivent
- DATA_NOT_VALID on:
  - Control character
  - Control character not Error
  - Terminate or Idle
  - Something else?

Delay Specification

- The current specification is imprecise
  - Previous specifications were to signals like CRS
  - Primary purpose for MAC control frames (e.g., Pause)
  - Allocation and specification to MAC control sublayer