WIS Fault Isolation

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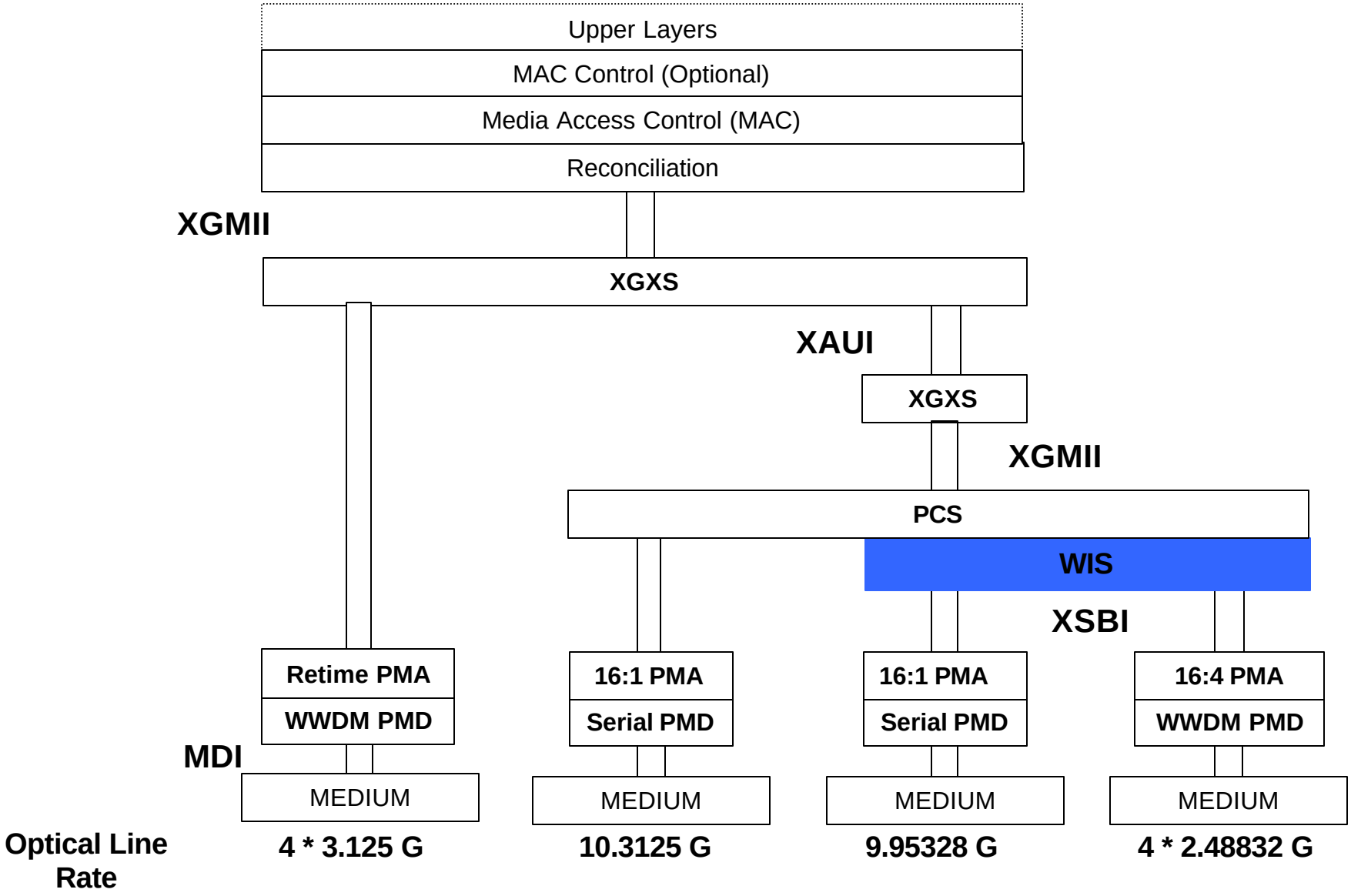
Tampa

David Martin, Norival Figueira, Paul Bottorff.....	Nortel Networks
Gary Nicholl.....	Cisco Systems
Howard Frazier.....	DomiNet Systems
Roy Bynum.....	WorldCom
Pankaj Kumar.....	Intel/Level One
Fred Weniger.....	Vitesse
Nan Chen.....	Force10 Networks
Nader Vijeh.....	Lantern Communications
Tom Alexander, Stuart Robinson, Gary Bourque, Richard Cam.....	PMC-Sierra
Prosun Chatterjee, Vinitha Suresh.....	Paxonet Communications

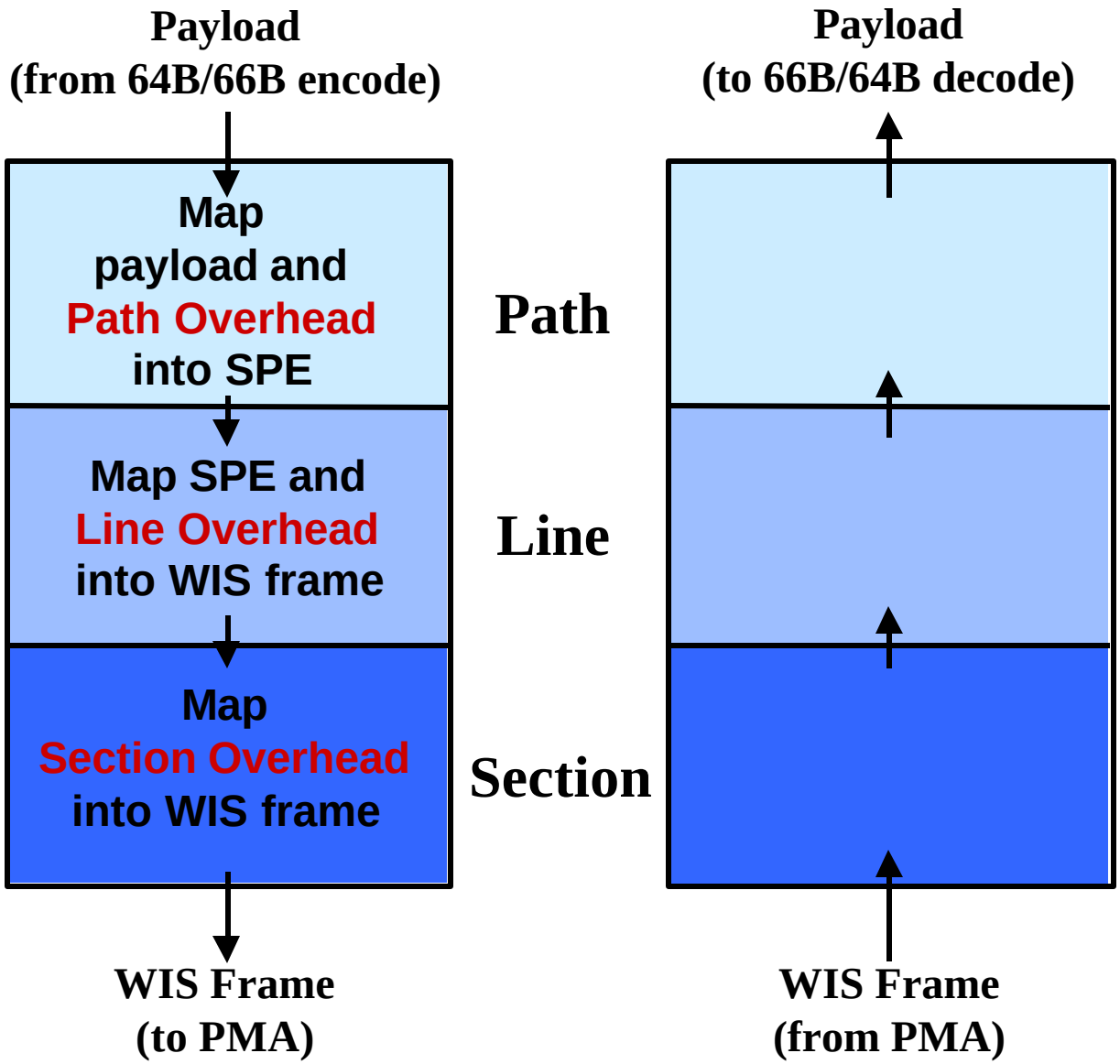
Fault Isolation

- **Two presentations at the May/Ottawa interim discussed the value in having some additional WIS overhead processing to facilitate 10GE WAN PHY fault isolation:**
  - http://grouper.ieee.org/groups/802/3/ae/public/may00/bynum_1_0500.pdf
  - http://grouper.ieee.org/groups/802/3/ae/public/may00/nicholl_1_0500.pdf
- **This presentation addresses those requests.**

WIS Location



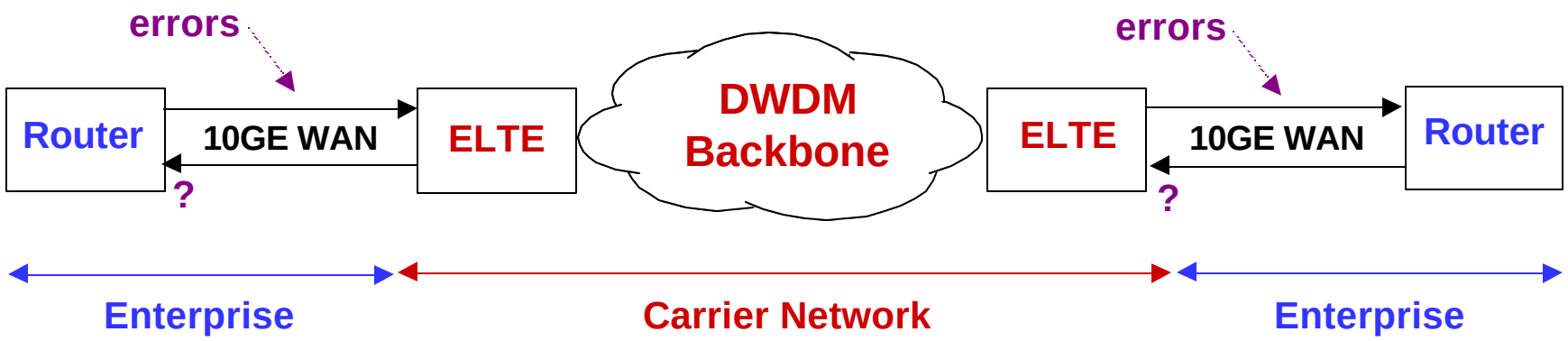
WIS Overhead Layers



From - http://grouper.ieee.org/groups/802/3/ae/public/jul00/figueira_1_0700.pdf

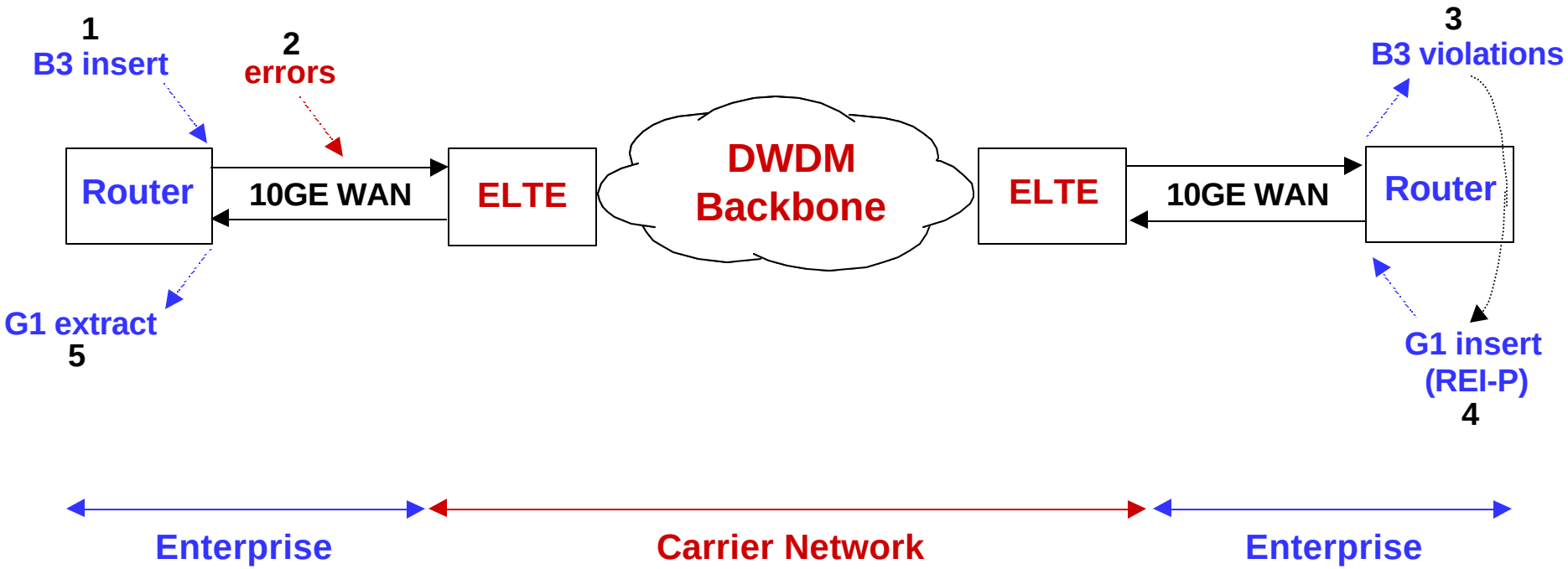
Single-Ended Maintenance: Soft Failure

- **Ability to determine a *degradation* of the transmit link from Enterprise or Carrier end.**



ELTE = Ethernet Line Terminating Equipment

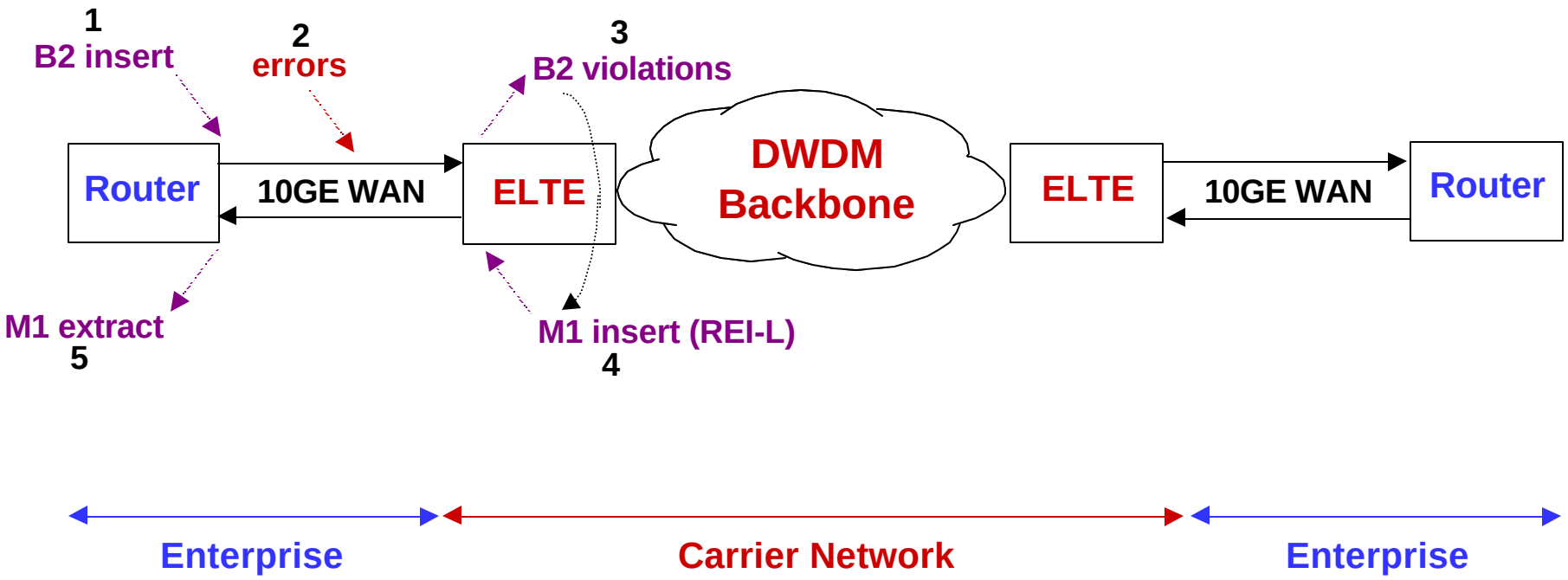
Example - Path layer view only (D1.0)



- **B3 violations are fed back in G1, but lefthand router cannot determine where the errors occurred.**

REI-P = Remote Error Indication-Path Layer

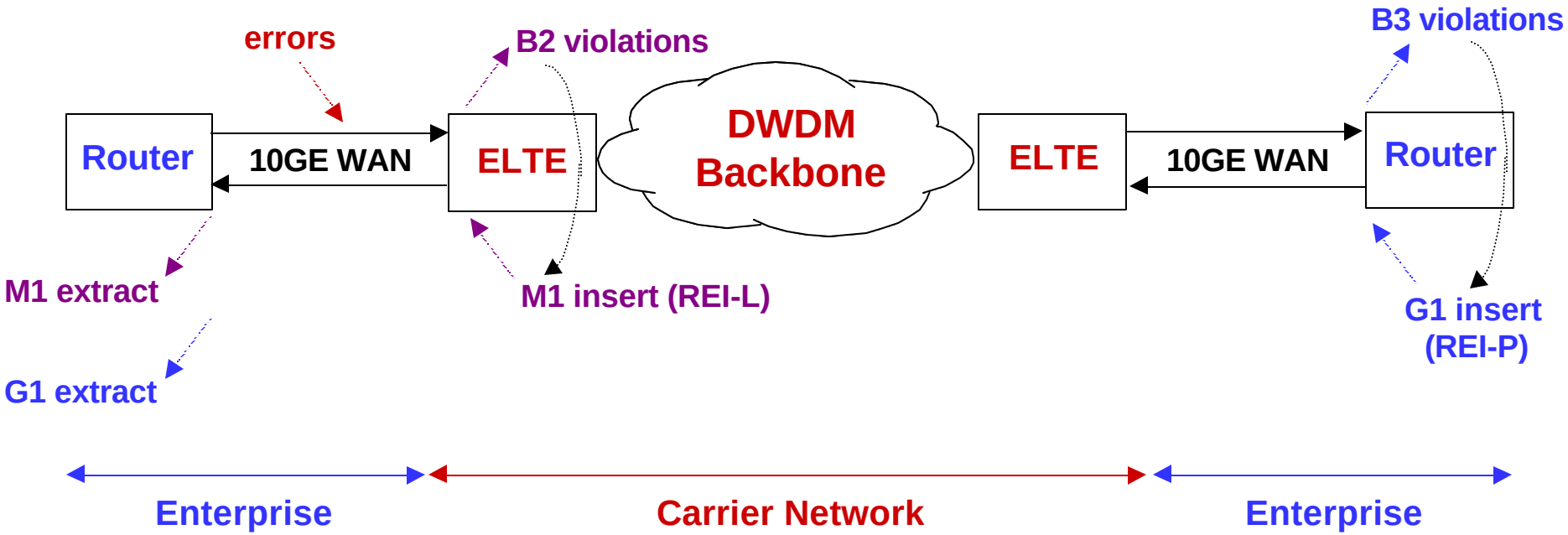
Example - Line layer view only



- **B2 violations are fed back in M1, so lefthand router can determine whether errors occurred in its outgoing link, but not the overall path.**

REI-L = Remote Error Indication-Line Layer

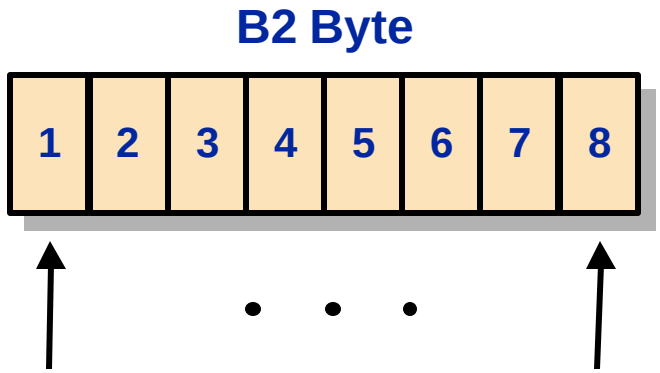
Example – Both line & path layer views



- **By comparing M1 & G1 values, lefthand router can determine whether errors occurred on its outgoing link or beyond.**

REI-L = Remote Error Indication-Line Layer
REI-P = Remote Error Indication-Path Layer

B2 (Line BIP-8) Definition



Even parity calculated over
all bit 1s from entire STS-1 frame
excluding section overhead

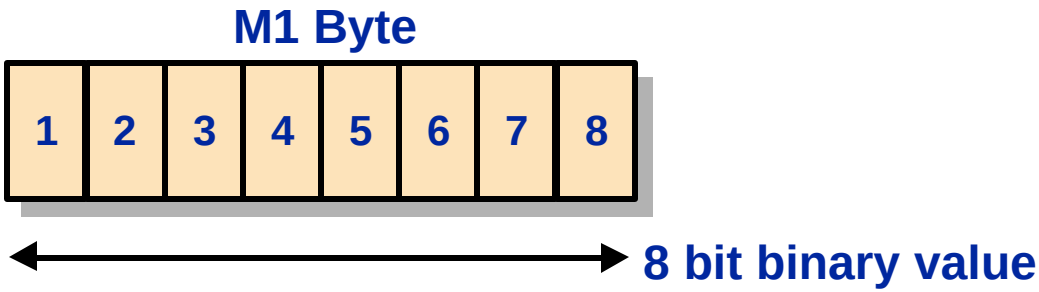
Even parity calculated over
all bit 8s from entire STS-1 frame
excluding section overhead

There are 192 B2 Bytes in the WIS frame, one in each STS-1

- In the transmit direction the WIS calculates & inserts the B2s
- In the receive direction the WIS calculates Line BIP-8s & compares with the extracted B2 values, discrepancies are B2 code violations

BIP-8 = Bit Interleaved Parity-8 bits wide

M1 (REI-L) Definition

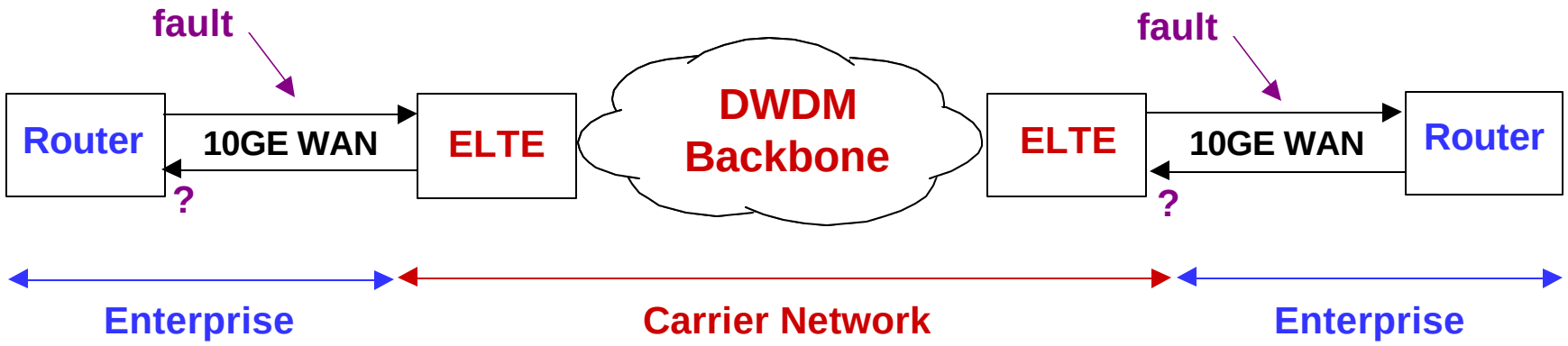


- In the transmit direction the WIS inserts the summed B2 violation count (truncated to 255) from its partner receiver into the outgoing M1 timeslot
- In the receive direction the WIS simply extracts the M1 value

REI-L = Remote Error Indication-Line Layer

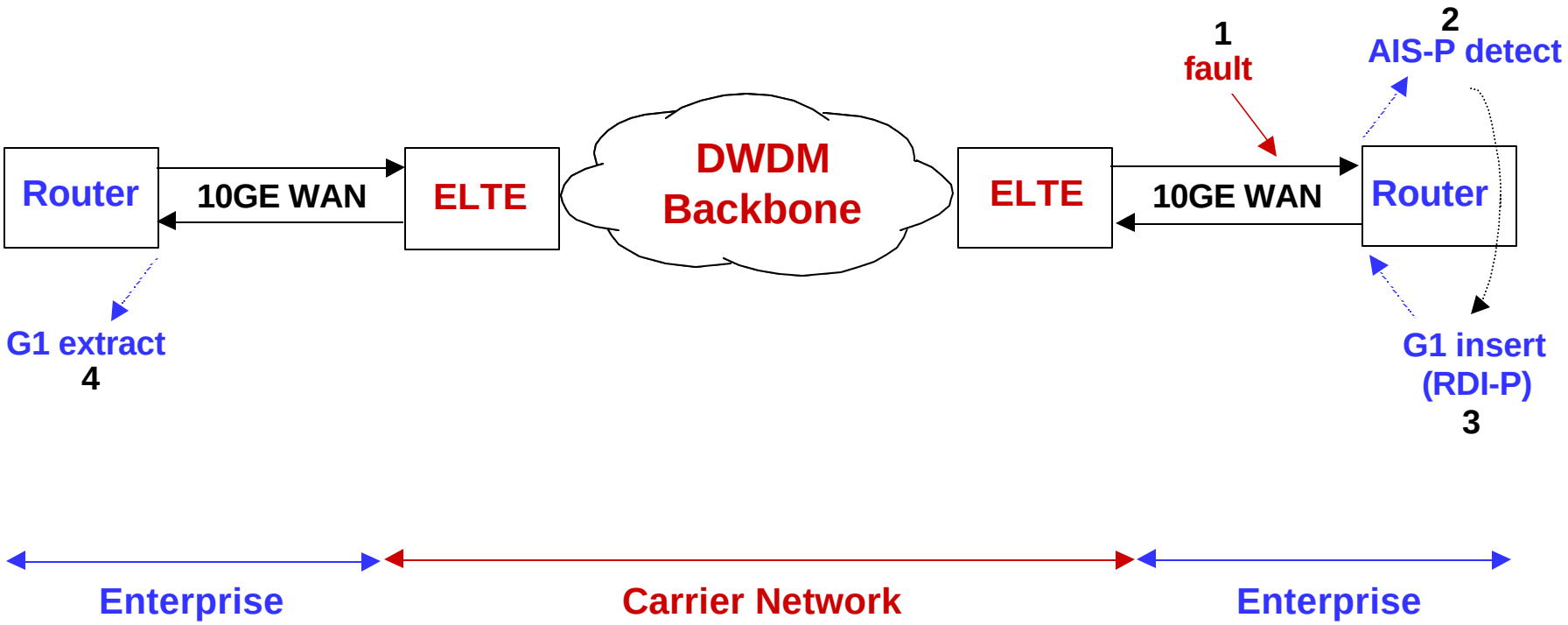
Single-Ended Maintenance: Hard Failure

- **Ability to determine a *failure* of the transmit link from Enterprise or Carrier end.**



ELTE = Ethernet Line Terminating Equipment

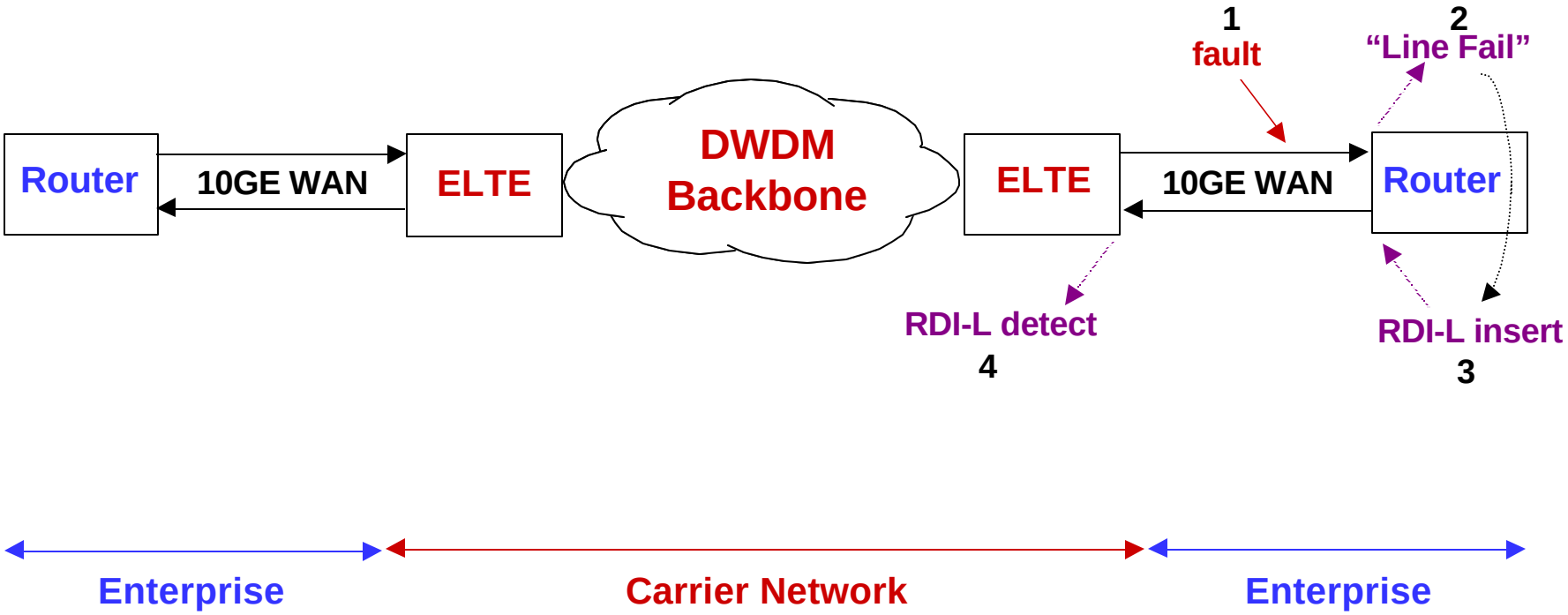
Example - Path layer view only (D1.0)



- **RDI-P is fed back in G1, but lefthand router cannot determine where the fault occurred.**

AIS-P = Alarm Indication Signal-Path layer
RDI-P = Remote Defect Indication-Path layer

Example - Line layer view only

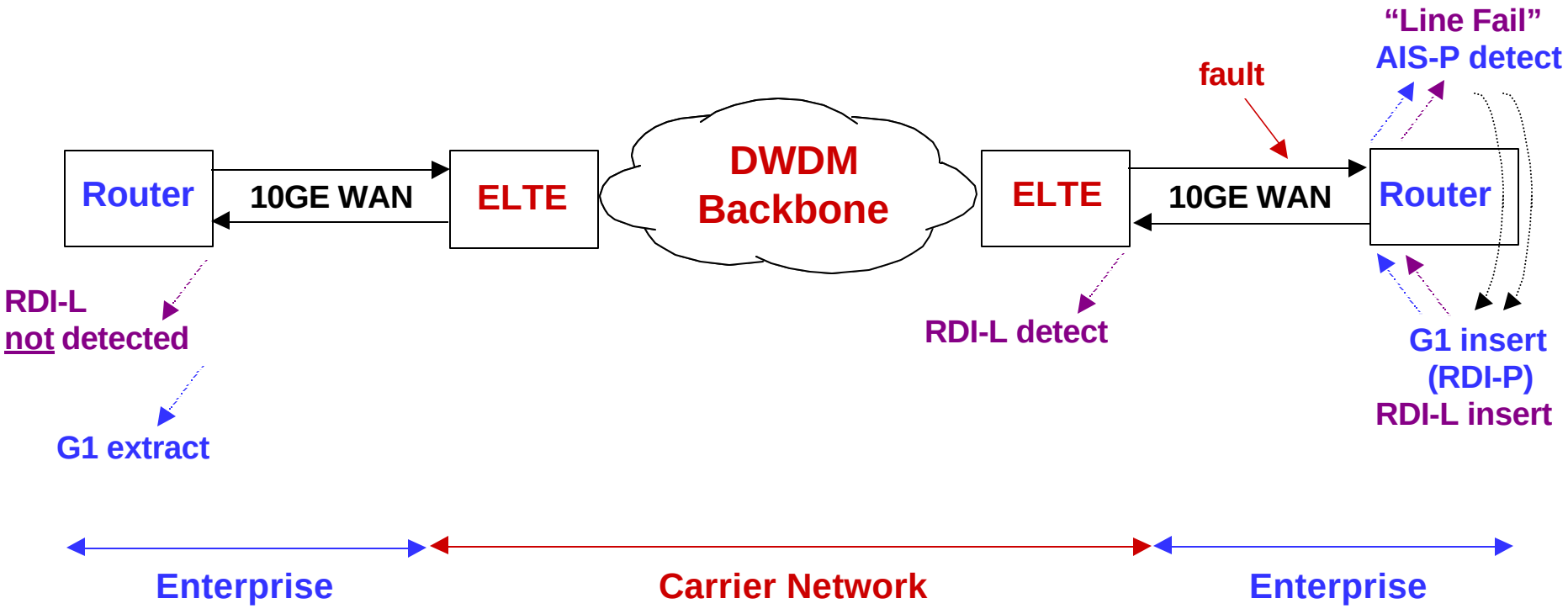


- **Lefthand router unaware that a failure occurred downstream.**

Line Fail = LOS + LOF + AIS-L
LOS = Loss Of Signal
LOF = Loss Of Frame
AIS-L = Alarm Indication Signal-Line layer

RDI-L = Remote Defect Indication-Line layer

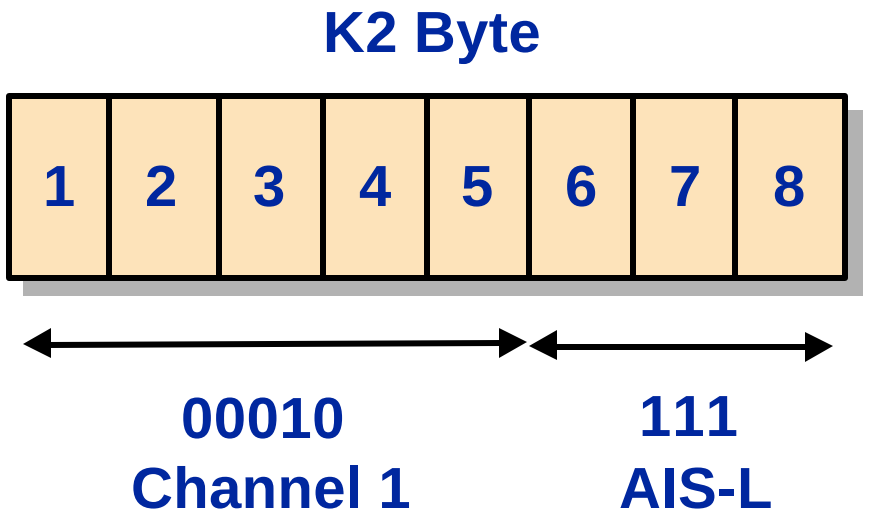
Example – Both line & path layer views



- **By comparing RDI-L state & G1 , lefthand router can determine whether a fault occurred on its outgoing link or beyond.**

RDI-L = Remote Defect Indication-Line layer
AIS-P = Alarm Indication Signal-Path layer
RDI-P = Remote Defect Indication-Path layer

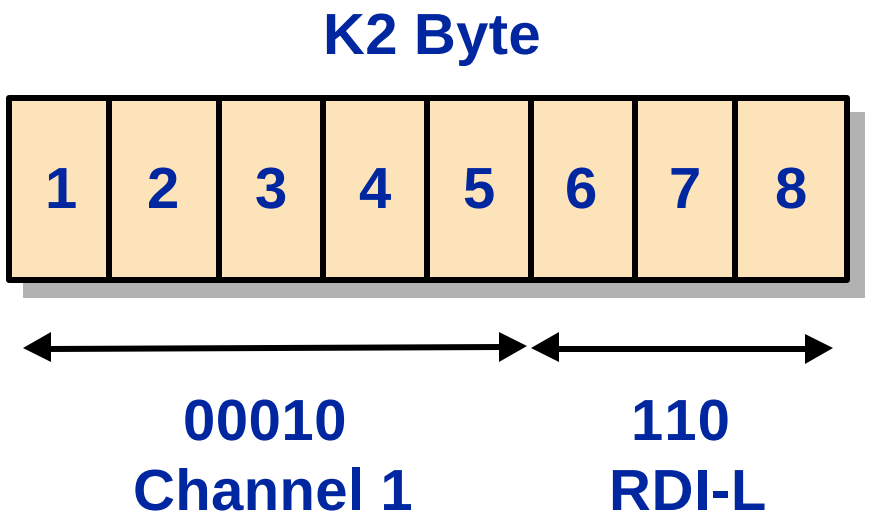
AIS-L Definition



- WIS normally generates K2 = 00010000
- The setting of bits 6-8 = 111 would occur in the Carrier's network at a Regen
- WIS only needs to detect AIS-L as a trigger to generate RDI-L

RDI-L = Remote Defect Indication-Line layer
AIS-L = Alarm Indication Signal-Line layer

RDI-L Definition

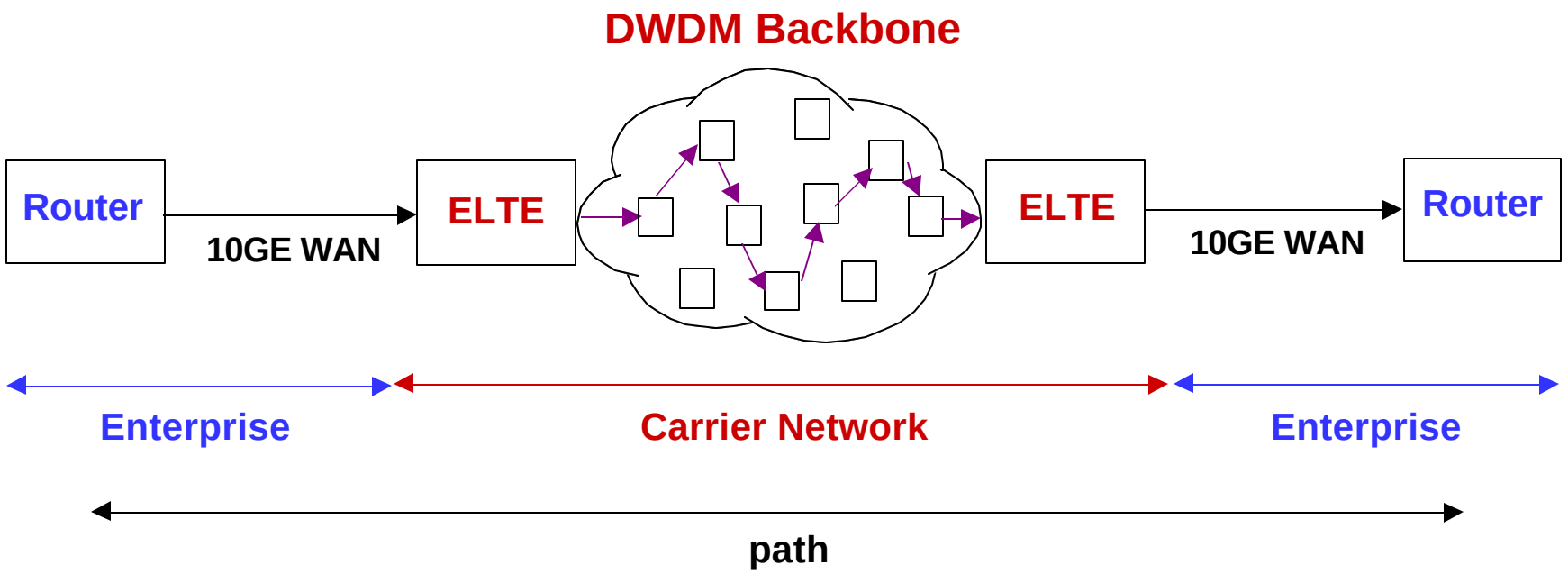


- WIS normally generates K2 = 00010000
- The setting of bits 6-8 = 110 is done by WIS only upon detection of a receive Line Fail

Line Fail = LOS + LOF + AIS-L
LOS = Loss Of Signal
LOF = Loss Of Frame
AIS-L = Alarm Indication Signal-Line layer
RDI-L = Remote Defect Indication-Line layer

Path Connectivity

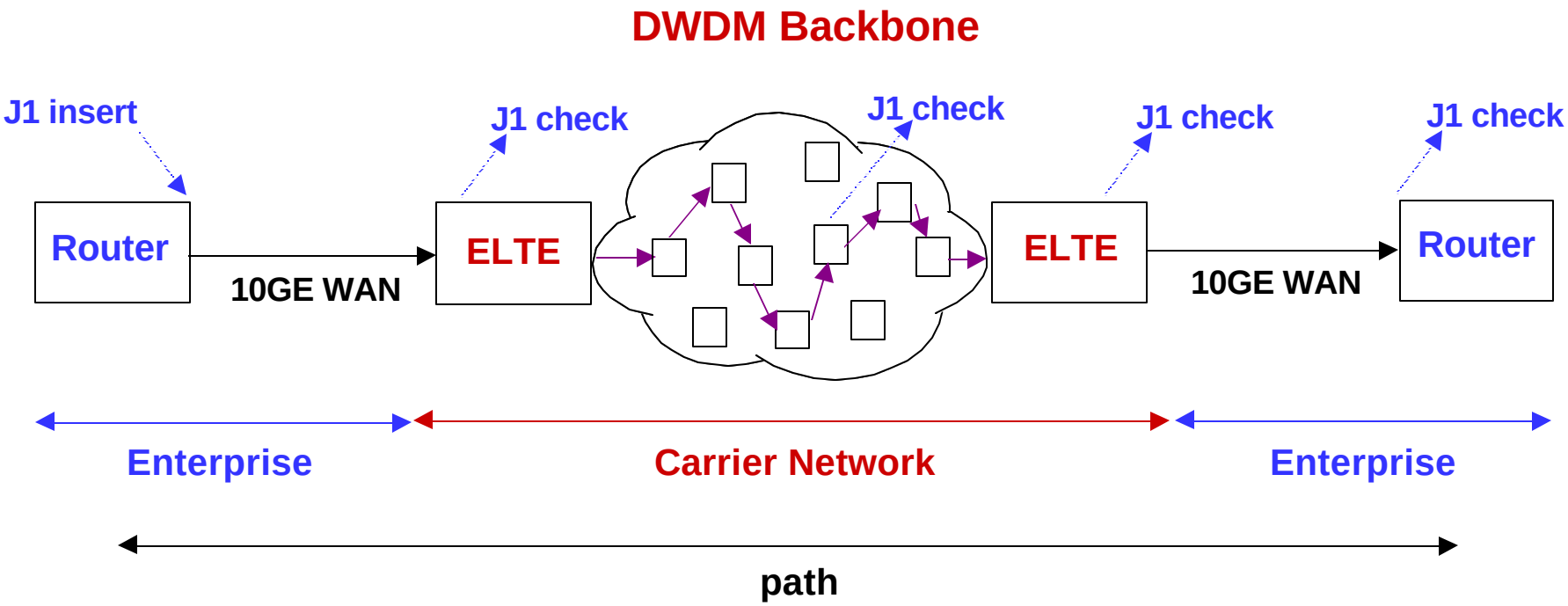
- **Ability to ensure correct connectivity across a large network.**



ELTE = Ethernet Line Terminating Equipment

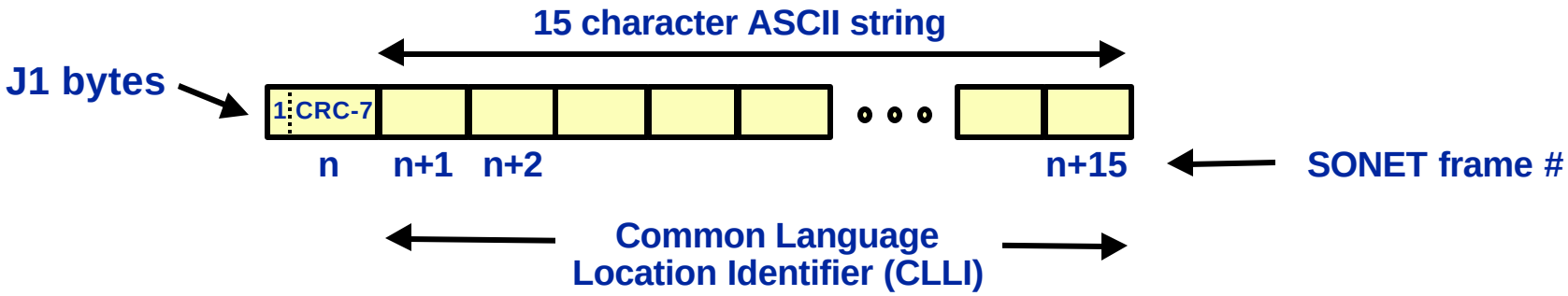
Path Connectivity Verification

- **Verify tapped J1 value is the expected value.**



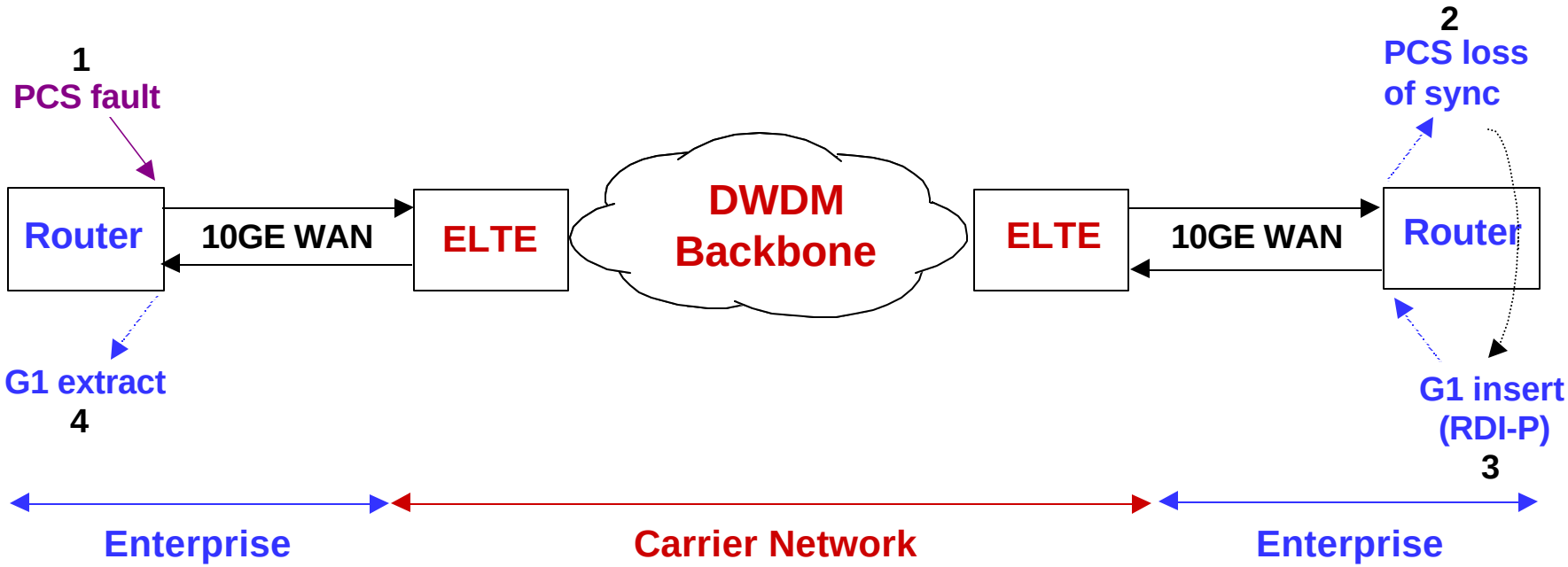
ELTE = Ethernet Line Terminating Equipment

J1 Path Trace



- **A path overhead byte sent once per frame (every 125usec) comprising a 16 byte label, verified by intended receiver and potentially at intermediate points.**

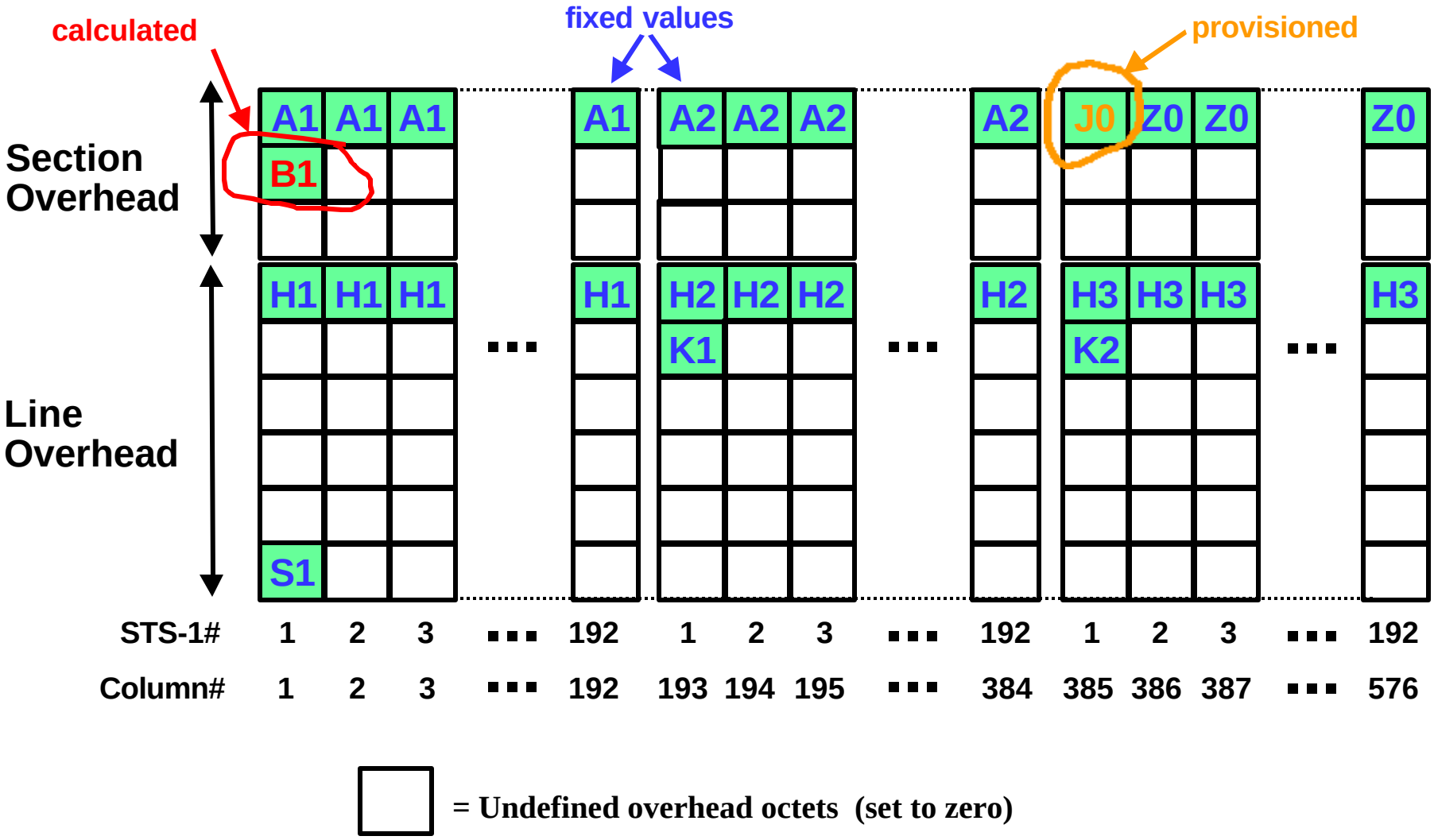
PCS Loss of Sync



- **"PCS loss of sync" (i.e. inability to sync to 64b/66b frames) is passed to WIS where it is integrated to become "LCD-P", then the outgoing G1 byte is coded with "Payload Defect" in RDI-P field**
  - notifies source of a payload problem (i.e. in PCS sublayer)

LCD-P = Loss of Cell Delineation-Path
RDI-P = Remote Defect Indication-Path

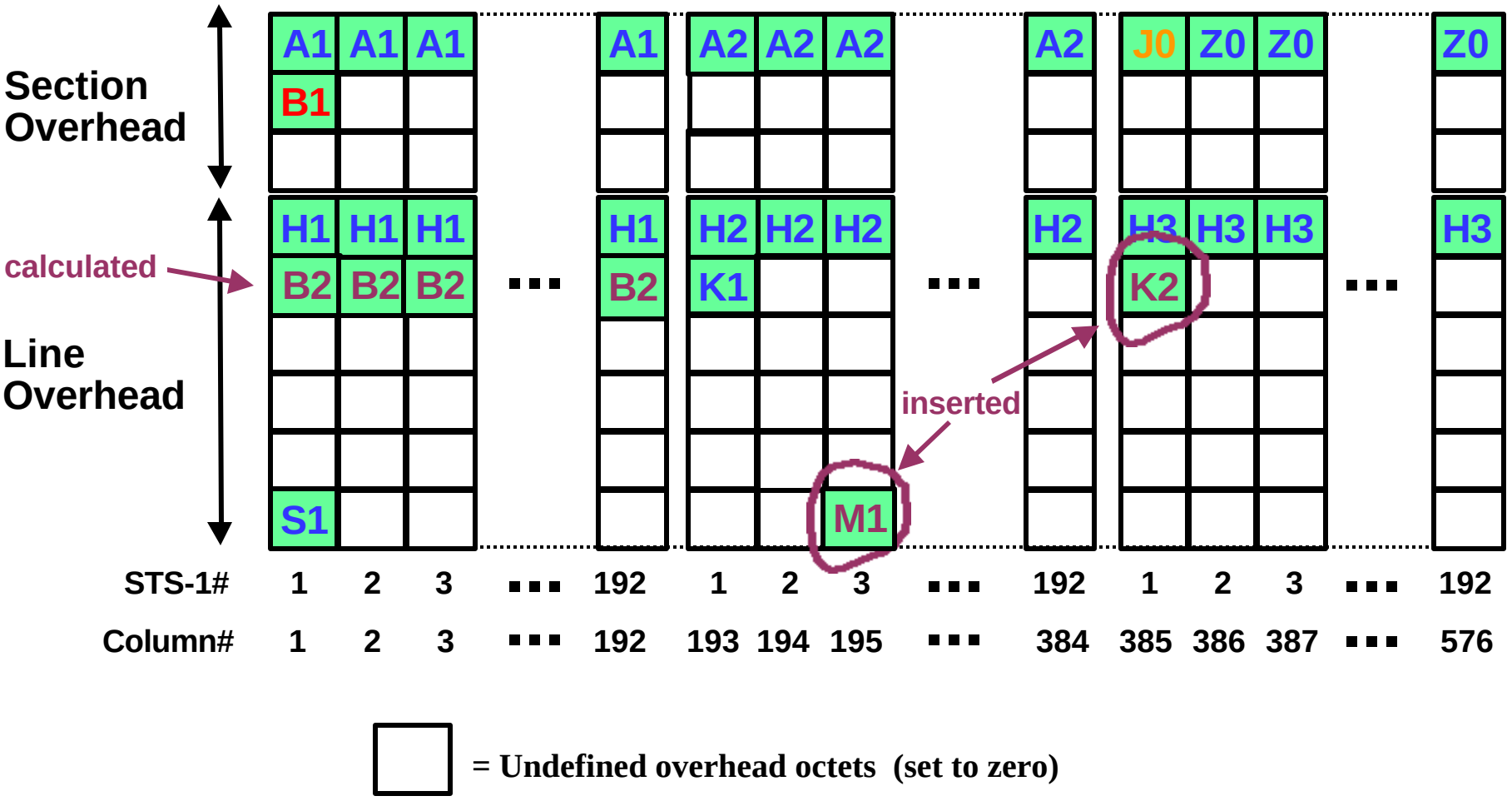
Transport Overhead (D1.0)



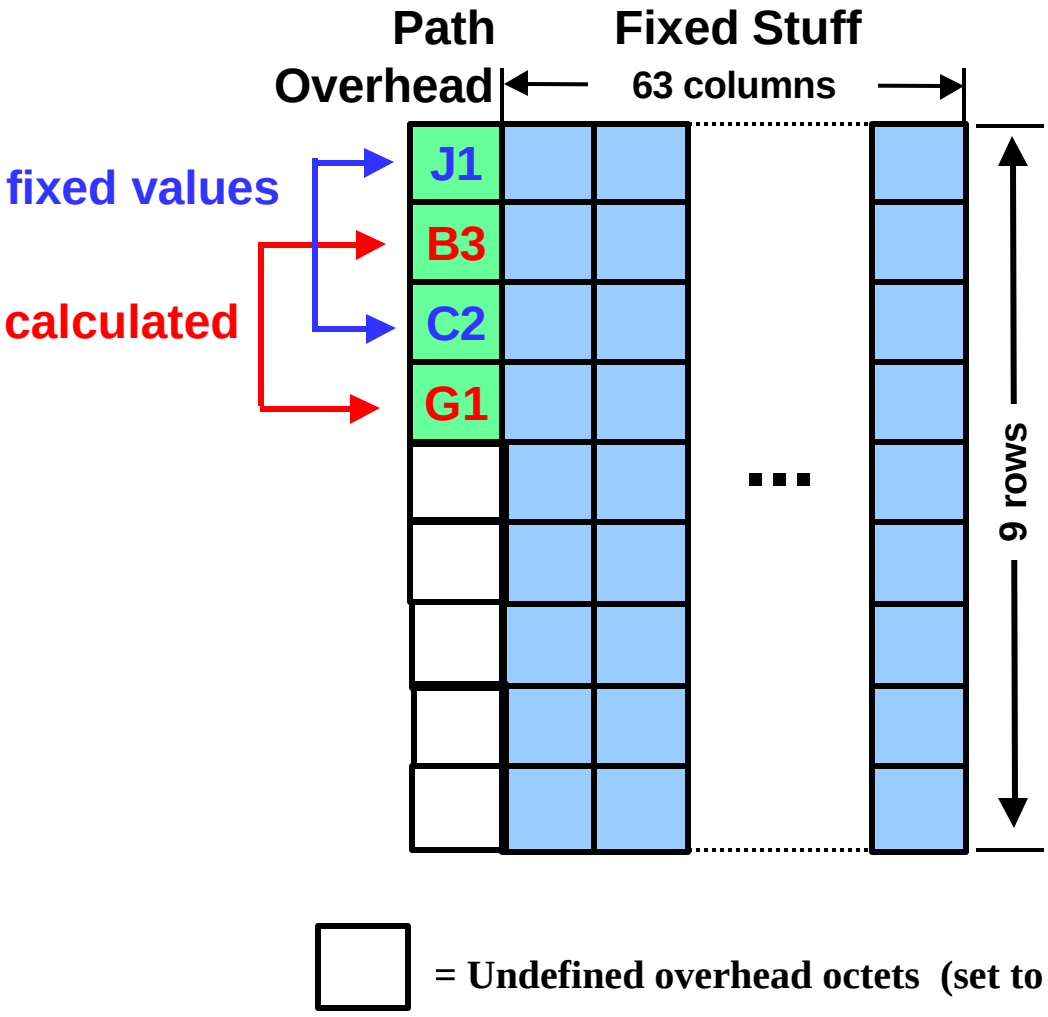
= Undefined overhead octets (set to zero)

From - http://grouper.ieee.org/groups/802/3/ae/public/jul00/figueira_1_0700.pdf

Transport Overhead - Addition



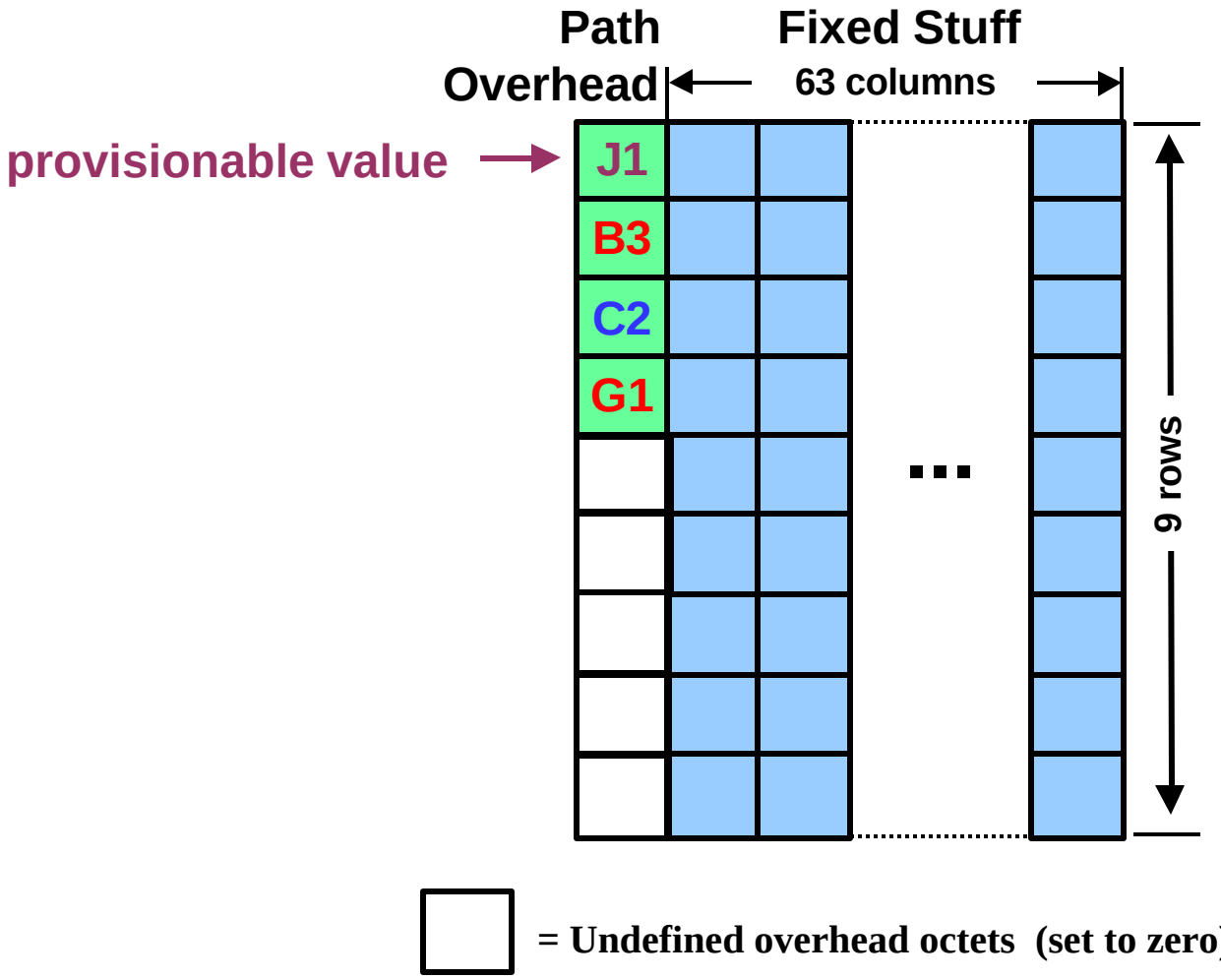
Path Overhead and “Fixed Stuff” (D1.0)



“Fixed Stuff” columns provide compatibility with SONET/SDH byte-interleaving and concatenation rules (set to zero)

From - http://grouper.ieee.org/groups/802/3/ae/public/jul00/figueira_1_0700.pdf

Path Overhead - Addition



"Fixed Stuff" columns provide compatibility with SONET/SDH byte-interleaving and concatenation rules (set to zero)

= Undefined overhead octets (set to zero)

Overhead Addition Summary

- **B2 calculation/insertion & error detection/reporting**
  - four 192x8 DPRAMs + ~1000 gates
- **M1 insertion & reporting**
  - ~70 flops + ~500 gates
- **RDI-L insertion & detection/reporting, plus AIS-L detection/reporting**
  - ~20 flops + ~200 gates
- **J1 (provisionable) insertion & reporting**
  - ~300 gates + two 16x8 RAMs
- **PCS loss of sync integration to LCD-P**
  - ~5 flops + 50 gates

All calculations at 32-wide (311MHz), except B2 DPRAMs at 16x 8-wide (78 MHz)

How to Modify the WIS Clause

- **Proposes changes to the definitions by cross-references contained in the "WIS Update" presentation approved for D1.0**
  - http://grouper.ieee.org/groups/802/3/ae/public/jul00/figueira_1_0700.pdf

- **WIS Clause still written by cross-referencing ANSI T1.416-1999**
  - ANSI T1.416-1999 can be obtained at the following URL: http://www.atis.org/atis/docstore/index.asp

Changes to Cross-References

- **Section 4 “Common Criteria”**
  - Referring to Table 1 (SONET Overheads at NIs)
  - Add support for the following
    - Section: B2 and M1
    - Path: J1
  - Note: B2 and M1 support are to be added to the WIS draft per instructions contained in the presentation indicated below for the case where these overheads are supported.
    - “WIS Update” used as the basis for D1.0 http://grouper.ieee.org/groups/802/3/ae/public/jul00/figueira_1_0700.pdf
  - Note: J1 support is to be added to the WIS draft per instructions (to follow) referencing ANSI T1.269-2000 Section 5 & Annex A.

Changes to Cross-References (cont'd)

- **Section 4 "Common Criteria" (cont'd)**
  - Change the following overhead to be partially supported
    - Line: K2 (set to 00010xxx)
      - Where bits 6-8* (i.e., xxx) shall be set to either RDI-L or 000. No other codes for bits 6-8 shall be generated by the WIS.
      - A receiver WIS shall only process bits 6-8 of K2. All other bits of K2 shall be ignored
      - A receiver WIS shall only detect AIS-L and RDI-L codes on bits 6-8 of received K2. All other codes (including 000) shall be ignored and shall have no effect on the receiver WIS
      - Note: K1/K2 settings still indicate a working channel rather than the protection channel

(*) This slide uses the SONET bit numbering convention, where bits are numbered from 1 (MSB) to 8 (LSB) and bit 1 is the leftmost bit.

Changes to Cross-References (cont'd)

- **Section 7 "Maintenance"**
  - Section 7.1, Table 2 "Near-end events and far-end reports"
    Add support for the following

    - Defects: AIS-L (as defined in Section 7.4.1)
      The WIS shall not generate AIS-L, but shall detect the presence of AIS-L in the received signal

      RDI-L (as defined in Section 7.4.1)

  - Note: BIP-N(L) and REI-L support is to be added to the WIS draft per instructions contained in the presentation indicated below for the case where B2 and M1 are supported.
    - "WIS Update" used as the basis for D1.0
      http://grouper.ieee.org/groups/802/3/ae/public/jul00/figueira_1_0700.pdf

Changes to Cross-References (cont'd)

- **Section 7 "Maintenance" (cont'd)**
  - Add LCD-P to the list of supported defects:
    - Uses same G1 RDI-P Payload Defect code as PLM-P
    - LCD-P is indicated when the *PCS loss of sync* signal is continuously asserted for a period of 3 ms
    - The LCD defect terminates when the *PCS loss of sync* signal is de-asserted for a period of 1 ms
    - *PCS Loss of sync* is a signal from the PCS and defined in the PCS clause