Tolerance Analysis of Resistive Discovery

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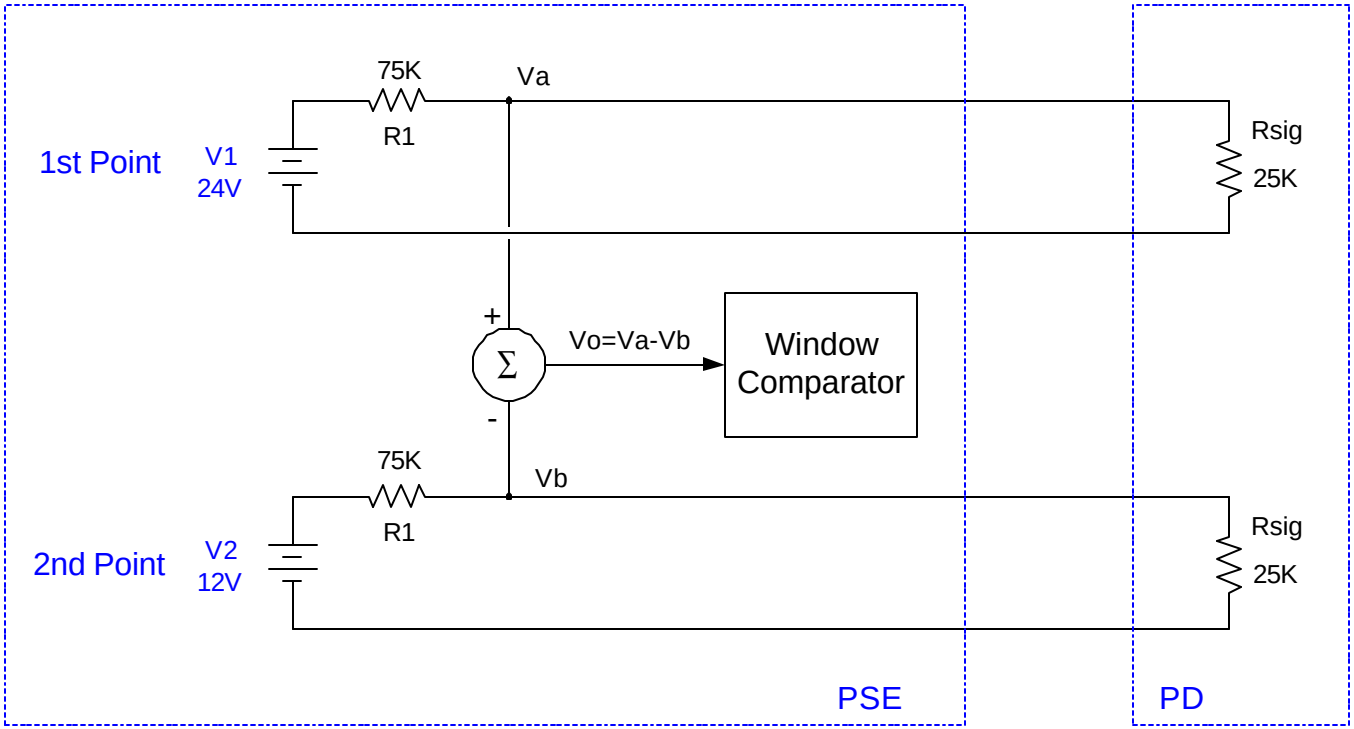
Basic Two Point Resistive Discovery Process

- **The Avaya protocol specifies a 2 point detection, where the two results are then subtracted**
  - 1st point: 24V open circuit, 320 µA short circuit
  - 2nd point: 12V open circuit, 160 µA short circuit



  - the min and max definitions are:

$$R1\_max = 75K \cdot (1 + res\_tol)$$

$$R1\_min = 75K \cdot (1 - res\_tol)$$

$$V1\_max = 24V \cdot (1 + src\_tol)$$

$$V1\_min = 24V \cdot (1 - src\_tol)$$

$$V2\_max = \frac{V1}{2} \cdot (1 + src\_rel\_tol)$$

$$V2\_min = \frac{V1}{2} \cdot (1 - src\_rel\_tol)$$

$$Rsig\_max = 26.5K$$

$$Rsig\_min = 19K$$

Basic Resistive Discovery Process

- **determination of window comparator thresholds**
  - the upper window comparator threshold is given by:

$$Vomax(a,b,c) := \left[Rsigmax \cdot \frac{(V1)\cdot(1 + a\cdot src\_tol) - \left[\frac{V1\cdot(1 + a\cdot src\_tol)}{2}\right]\cdot(1 + c\cdot src\_rel\_tol)}{R1\cdot(1 + b\cdot res\_tol) + Rsigmax} \right]$$

  - the lower window comparator threshold is given by:

$$Vomin(a,b,c) := \left[Rsigmin \cdot \frac{(V1)\cdot(1 + a\cdot src\_tol) - \left[\frac{V1\cdot(1 + a\cdot src\_tol)}{2}\right]\cdot(1 + c\cdot src\_rel\_tol)}{R1\cdot(1 + b\cdot res\_tol) + Rsigmin} \right]$$

  - where a, b, and c each take on values of +1, or -1 during the worst case analysis

- **tabulation of the results for various source and resistor tolerances**

Table of Window Comparator Thresholds				
res_tol	src_tol	src_rel_tol	Upper Threshold	Lower Threshold
10%	10%	1%	3.758V	2.001V
5%	5%	1%	3.450V	2.194V
2%	2%	1%	3.276V	2.316V
1%	1%	1%	3.220V	2.358V

Basic Resistive Discovery Process

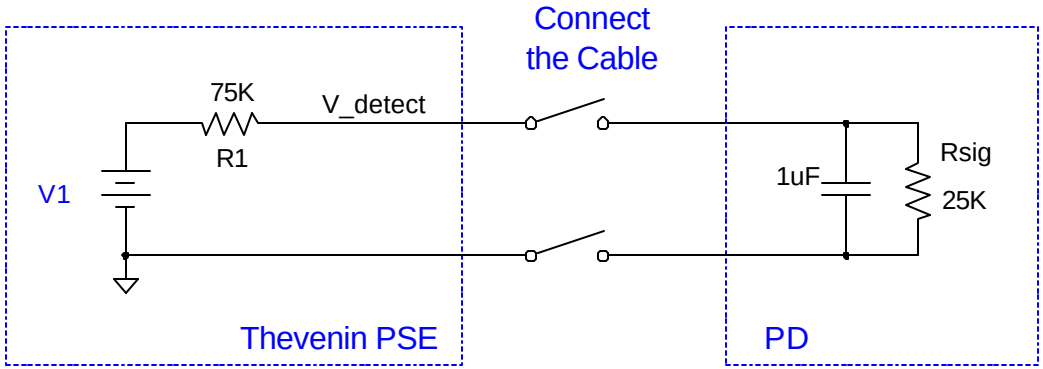
- **Given the window comparator Thresholds that are now set, the following table shows the signature resistance that is guaranteed to be rejected (again using worst case analysis)**

res_tol	src_tol	src_rel_tol	Always reject signatures below	Always reject signatures above
10%	10%	1%	11.923K ohm	44.722K ohm
5%	5%	1%	14.840K ohm	34.672K ohm
2%	2%	1%	16.946K ohm	29.956K ohm
1%	1%	1%	17.719K ohm	28.555K ohm

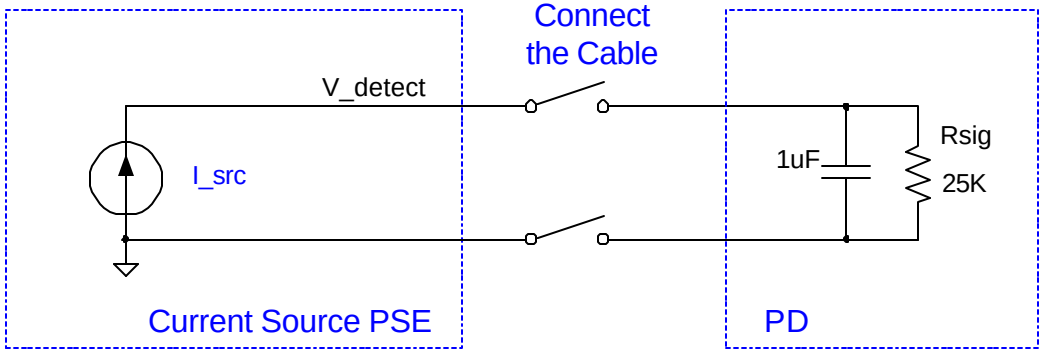
- **Summary of the basic 2 point resistive discovery method:**
- **In order to meet the present version (12/18/2000) of the PSE, PD specs, the PSE will need to have tolerances that are less than 1%, since:**
  - this analysis assumes a perfect window comparator, comparator thresholds, ADC, etc…
  - this analysis does not include the whole system implementation
  - this analysis does not include any timing or interference constraints
  - this analysis does not include capacitive loads
  - this analysis does not include the effects of noise

What About Capacitive Loads within the PD, or PSE?

- **Thevenin (or Norton) PSE, 1 µF capacitive load**



- **pure current source PSE , 1 µF capacitive load**

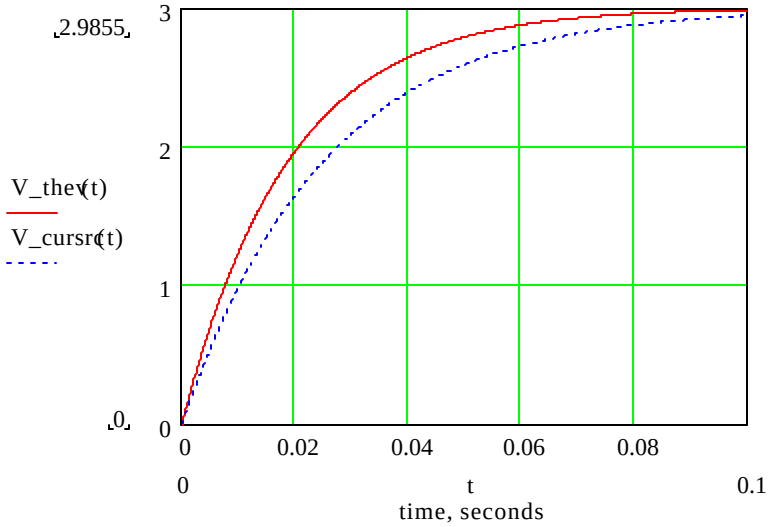


Capacitive Load Settling Time for a single 12V step

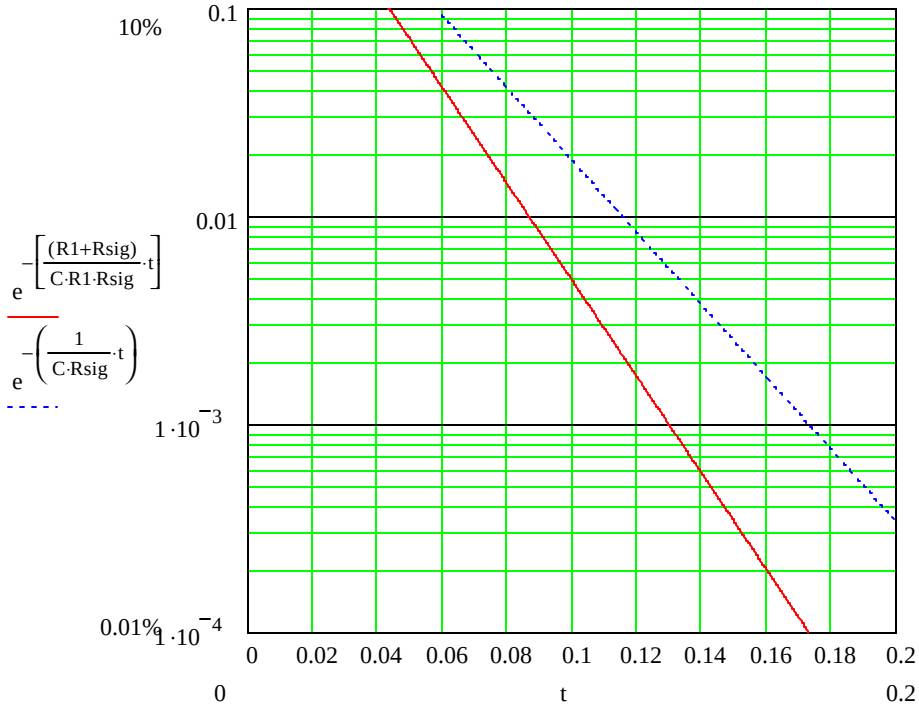
- **detector voltage settling time:**

$$V\_thev(t) := \frac{-Rsig \cdot V1}{((R1 + Rsig))} \cdot e^{-\left[\frac{(R1+Rsig)}{C \cdot R1 \cdot Rsig} \cdot t\right]} + \frac{Rsig \cdot V1}{((R1 + Rsig))}$$

$$V\_cursrc(t) := Isrc \cdot Rsig \cdot \left(1 - e^{\frac{-t}{RsigC}}\right)$$



error term settling time:



- **Thevenin (Norton) source settles to within: 1% in 86.3 ms 0.1% in 129.5 ms**
- **pure current source settles to within: 1% in 115.1 ms 0.1% in 172.7 ms**

Total Discovery Time and Tolerance Analysis Summary

- **A Thevenin, or Norton PSE with the following:**
  - 75K +/- 1% source resistor, zero output capacitance
  - 24V +/- 1% 1st source
  - 12V +/- 0.1% 2nd source
  - 0.1% settling time allowed due the possible capacitive load
- **It will take 259ms to do a single 2 point "slope" discovery with no repetitions**
- **A pure current driven PSE would take 345ms to do a 2 point discovery with no repetitions**
  - assuming 0.1% settling time is needed for discovery
- **However, 350 ms is the maximum specified discovery time**
- **Tolerance Analysis Summary and Recommendations:**
  - try to eliminate the need for 1% tolerances within the PSE
    - higher relative cost
    - eliminate the need to use a micro-controller with an accurate ADC for discovery
  - lower the signature resistance to speed up discovery time and allow for repeating the 2 point discovery process
  - readjust the signature tolerances so that the dead bands are larger relative to the valid signature window
  - have a means of auto-calibration within the PSE
  - shape the PSE voltage or current drive waveforms to speed up discovery time
  - lower the maximum allowed capacitive load by an order of magnitude, including PSE and PD
  - keep the nominal signature value centered within the tolerance bands