Specifying PD input capacitor

- Specifying “input capacitance” complicates qualification testing
- We need a input inrush spec based on time, voltage, and/or current

Method for testing input capacitance

- C = I*dt/dv, so we can force either I or dv and measure dt to determine capacitance
- Testability:
  - forcing I and measuring dv/dt can be fooled if a PD inrush limiter is present - requires a two-part test
  - forcing dv/dt and measuring I requires only a single test

Proposed spec

- “The input current shall not increase over the nominal value by more that [CMAX * 1000] when a 1V/ms positive voltage slope starting at >= 44V is applied to the input terminals at the PD”
- The force-current analog can be used if a two-part test is used to detect inrush limiting circuitry
  - Run test below UVLO?
  - Use negative dv/dt?