IEEE802.3af
DTE Power via MDI task Force.

Proposal for Test Circuits and Test procedures

Rev 002

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Conceptual approach:

1. Each test setup contains the necessary information for the specified test without dependence in previous tests.
2. Single equivalent test setup can be used for all tests.
3. Equivalent test setups and procedures may be used

Table 33-5-Items 1, 4a and 14:
Output Voltage, polarity and continuous output power

Tested Parameters

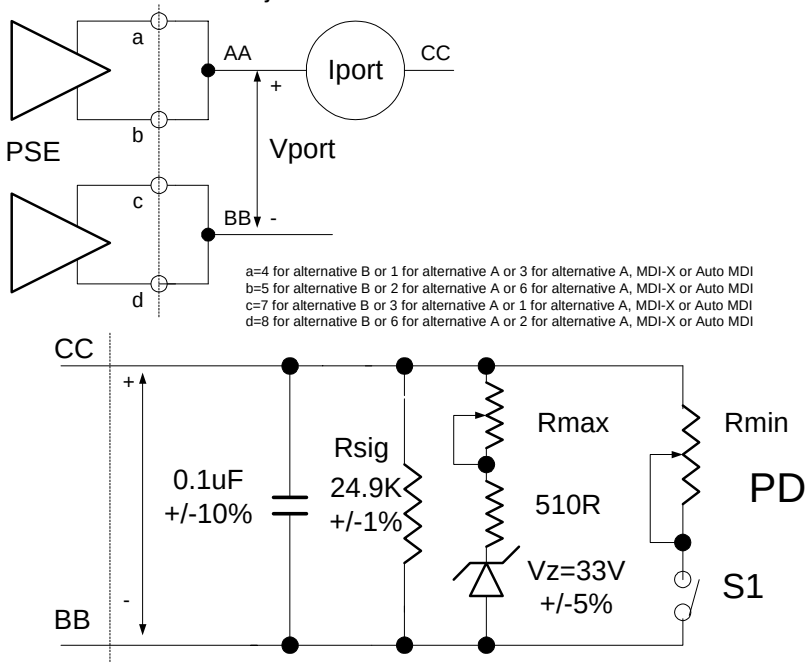
1. Output voltage, Vport.
2. Voltage polarity (Table 33-1)
3. Output Current at normal powering mode
4. Continuous min output power, Pport.

Test setup

Will be tested as indicated in Figure 33-5-1

Test procedure

1. Wait 1sec min and measure Vport at Rmax (S1 open).
   Rmax shall be adjusted to generate Iport_min=10mA.
2. Wait 1sec min and measure Vport at Rmin (S1 close).
   Rmin shall be adjusted to have a total load of 15.4W min.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$R\min < \frac{Vport^2}{15.4 - Vport * Iport\_\min}$$

$$44V \le Vport \le 57$$

Figure 33-5-1

Table 33-5-Item 2: Load Regulation

Tested Parameters

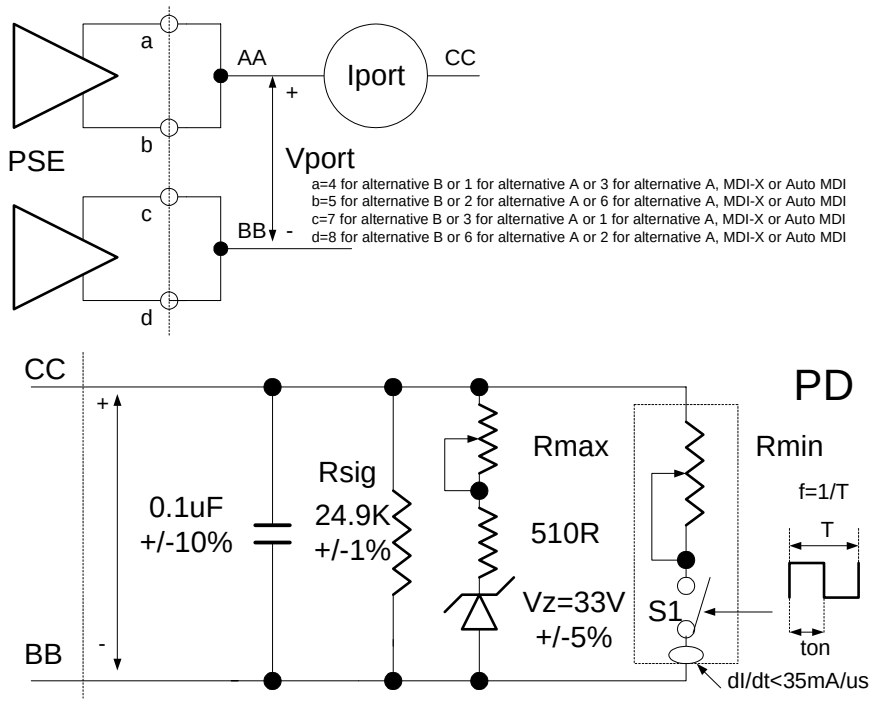
1. Voltage transients during load changes.

Test setup

Will be tested as indicated in Figure 33-5-2

Test procedure

3. Wait 1sec min and measure Vport at Rmax (S1 open).
   Rmax shall be adjusted to generate Iport_min=10mA.
1. Wait 1sec min and measure Vport at Rmin (S1 close).
   Rmin shall be adjusted to have a total load of 15.4W min.
2. Change load from Rmax to Rmin and from Rmin to Rmax at f=10Hz,
   Duty cycle =ton/T=0.5 ±20% while monitoring Vport.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$R\min < \frac{Vport^2}{15.4 - Vport * Iport\_\min}$$

$$44V \le Vport \le 57$$

Figure 33-5-2

Table 33-5-Item 3: Ripple and Noise

Tested Parameters

1. Ripple and noise Voltage transients during load changes.

Test setup

1. Will be tested as indicated in Figure 33-5-1
2. Filter network may be used to isolate PSE port noise from external noise sources.

Test procedure

4. Wait 1sec min and measure Vport at Rmax (S1 open).
   Rmax shall be adjusted to generate Iport_min=10mA.
1. Wait 1sec min and measure Vport at Rmin (S1 close).
   Rmin shall be adjusted to have a total load of 15.4W min.
2. Measure Vport ac noise and ripple at Rmax (S1 open) and at Rmin (S1 closed)
   by using Spectrum Analyzer or equivalent equipment.

Table 33-5-Item 4: Output Current at Normal Powering Mode.

See test 33-5-1.

Table 33-5-Item 5: Output Current at Startup Mode.

Tested Parameters

1. Inrush current and its timing limits during startup: I_{INRUSH} and T_{LIM}.

Test setup

Will be tested as indicated in Figure 33-5-5
Test setup principles:

- S1 function is to connect a large capacitive load when the port voltage exceeds 42V.
- S1 shall be designed to allow the transition from OFF to ON with less than 50us.
- The capacitive load value designed to force a short circuit condition for more than 75ms.
- Test can be repeated only if the voltage across the capacitive load is less than 0.7V and S1 was reset.

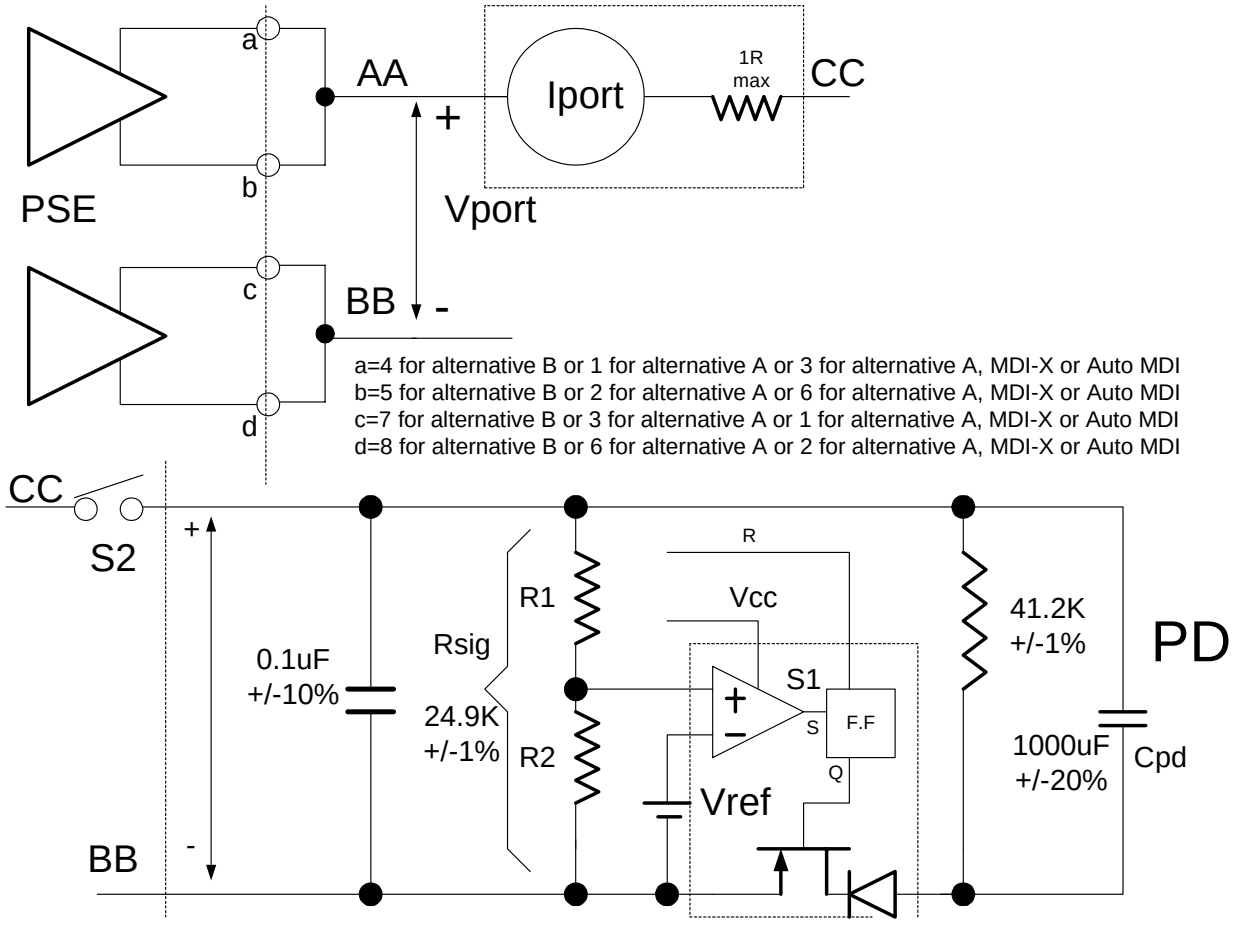


Figure 33-5-5

Test procedure

1. Set S2 to Off. Verify that the voltage on Cpd is less than 0.7V.
2. Set S2 to ON. Monitor Vport and Iport when S1 (electronic switch in figure 33-11) has turned ON.
3. Verify that Iport is within the limits as indicated by figure 33-5-5.1.

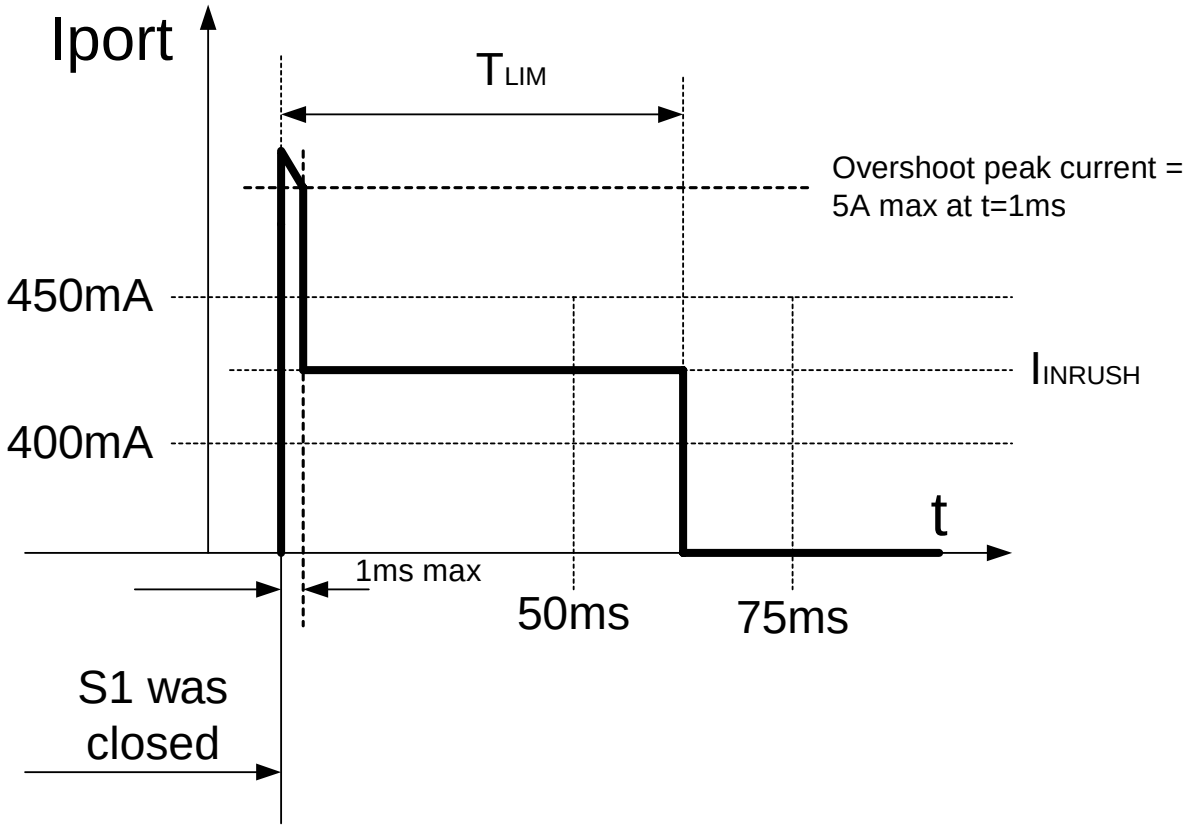


Figure 33-5-5.1

Table 33-5-Items 6a and 7: Power off mode current
(Option (a) as indicated in paragraph 33.2.11)

Tested Parameters

1. Power off mode current, $I_{MIN1.}$
2. Disconnect detection time, T_{PMDO} min and max.

Test setup

Will be tested as indicated in Figure 33-5-6

Test procedure

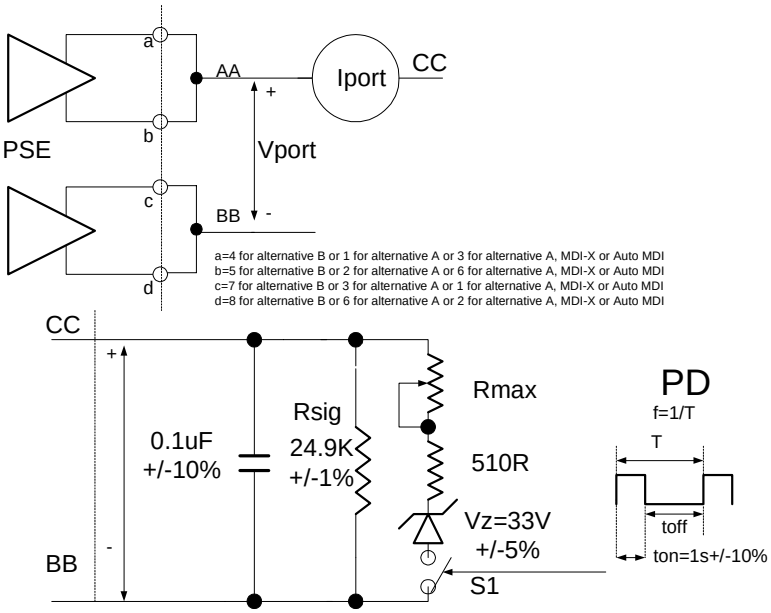
1. Wait 1sec min and measure Vport at Rmax (S1 close).
   Verify that $44V \le Vport \le 57$
   Rmax shall be adjusted to generate Iport_min=10mA.

2. Increase Rmax and verify that the power is removed from the port by verifying that Vport decreases by 1V at Iport>=5mA

3. Repeat step 1.

4. Adjust S1 control to: S1 off time 299.0 ms. Verify that Vport is stable and within its initial values (Power is not removed from the port).

5. Adjust S1 control to: S1 off time 400.0 ms.
   Verify that power was removed from the port within 400ms max of the 1st cycle from the time that S1 was opened. See figure 33-16 for timing relationship.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

Figure 33-5-6

Table 33-5-Items 4c, 8 and 9:
Overload current detection range
Overload timings.

Tested Parameters

1. Over load current detection range, $I_{CUT.}$
2. Over load time limit, T_{CUT} min and max.

Test setup

Will be tested as indicated in Figure 33-5-2

Test procedure

1. Set Rmax (S1 open) and Rmin (S1 close) according to:
   (Rmax shall be adjusted to generate Iport_min=10mA.)
   Verify that $44V \le Vport \le 57$
2. Close S1. Decrease slowly Rmin until power is removed from the port and record Iport=I_{CUT}.
   (Power is removed when Vport decreases by 1V from its initial value and Iport reduced to less than 5mA)
3. Verify that $\frac{15.4}{Vport} < I_{CUT} \le 400mA$.
4. Repeat step 1.
   Adjust S1 control to: Iport> $I_{CUT.}$ S1 on time: 50.0ms.
   Verify that power is not removed from the port.

   Adjust S1 control to: Iport> $I_{CUT.}$ S1 on time: 75.0ms.
   Verify that power is removed from the port.

   See figure 33-5-8 for more info.

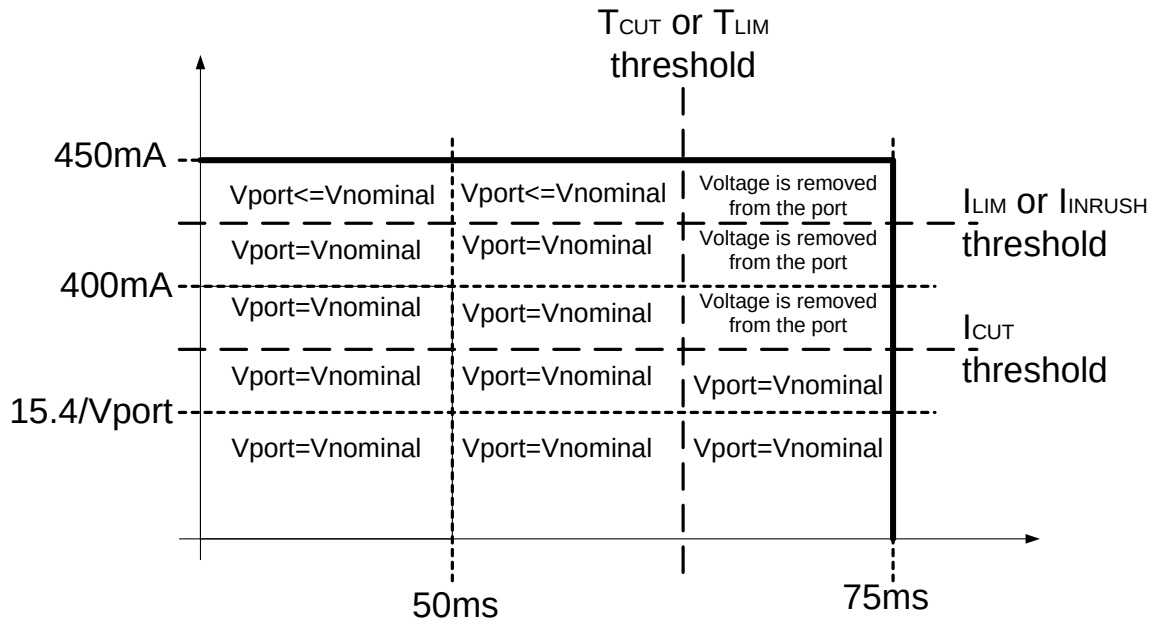


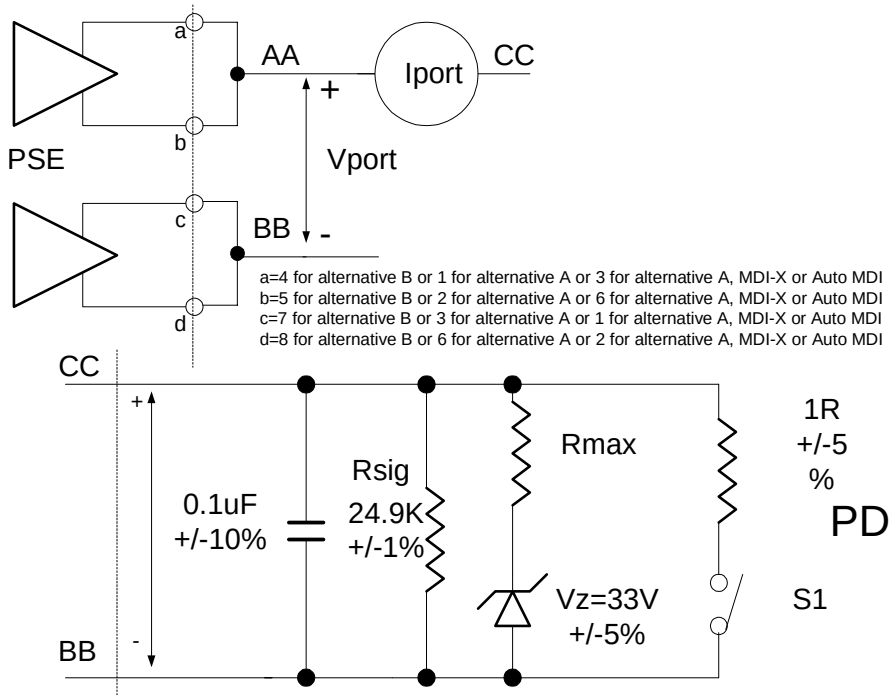
Figure 33-5-8

Table 33-5-Items 10 and 11: Output Current at Short Circuit

Tested Parameters

1. Iport and its timing limits during short circuit condition: I_{LIM} and T_{LIM}.

Test setup
Will be tested as indicated in Figure 33-5-10



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$44V \le Vport \le 57$$

Figure 33-5-10

Test procedure

1. Wait 1sec min and measure Vport at Rmax (S1 open).
   Rmax shall be adjusted to generate Iport_min=10mA.
   Verify that $44V \le Vport \le 57$
2. Close S1 (see figure 33-5-10.1).
3. Verify that Iport is within the limits as indicated by figure 5.

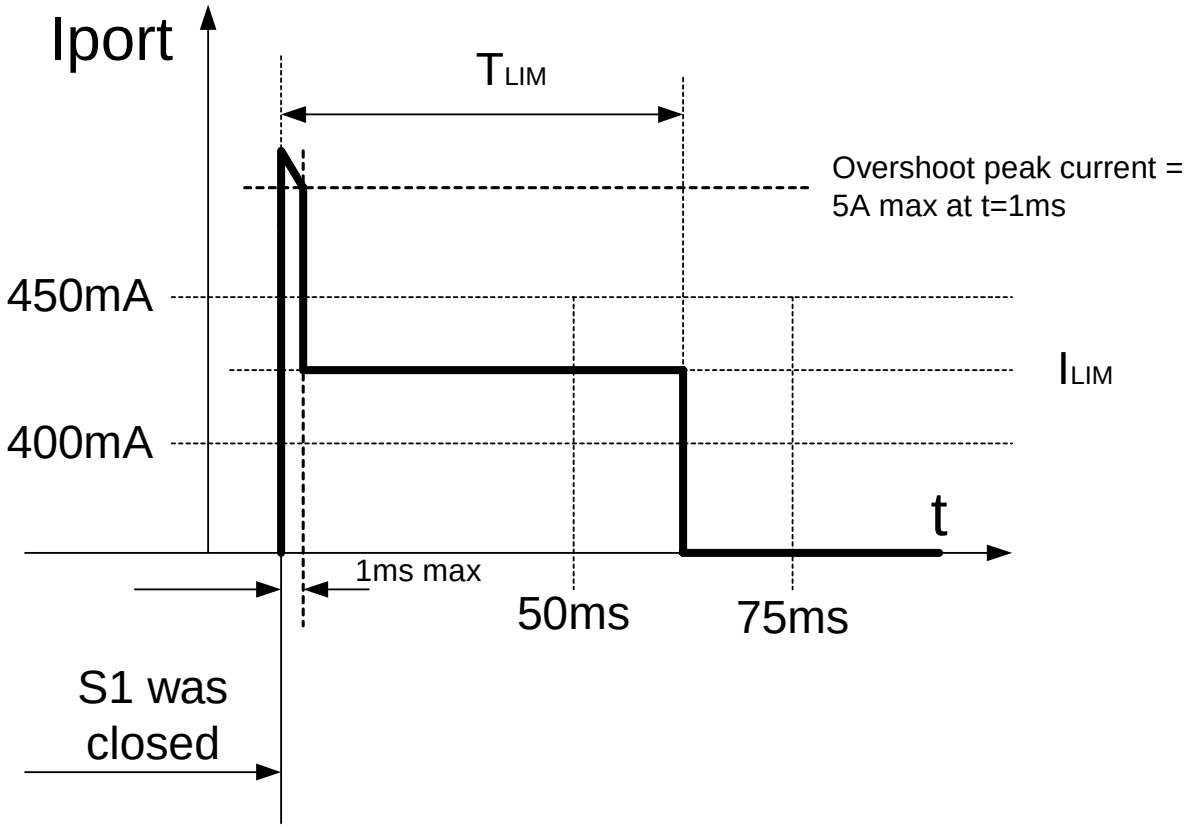


Figure 33-5-10.1

Table 33-5-Item 12: Turn on rise time

Tested Parameters

1. PSE port voltage turn on rise time, T_{RISE}.

Test setup

Will be tested as indicated in Figure 33-5-1

Test procedure

1. Measure Vport at Rmax (S1 open).
   Rmax shall be adjusted to generate Iport_min=10mA at Vport.
   Measure rise time form 10% of Vport to 90% of Vport
   See figure 33-5-16.1.
2. Measure Vport at Rmin (S1 close).
   Rmin shall be adjusted to have a total load of 15.4W min.
   Measure rise time form 10% of Vport to 90% of Vport
   See figure 33-5-16.1.

Table 33-5-Item 13: Turn off time

Tested Parameters

1. PSE port turn off time, T_{OFF}.

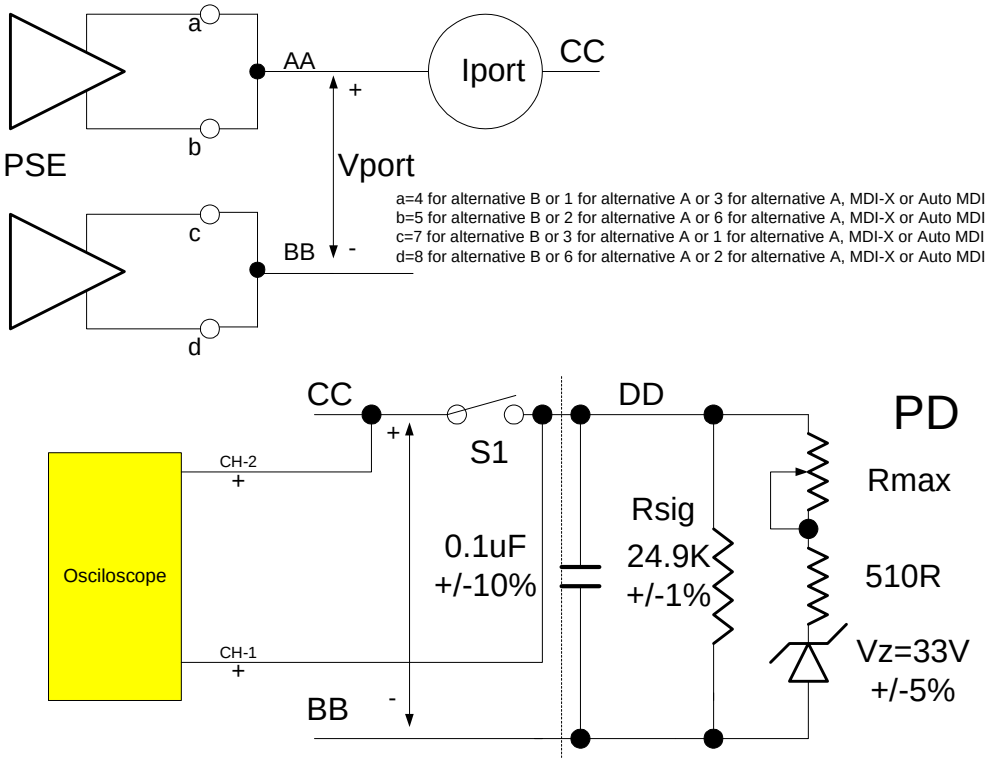
Test setup

Will be tested as indicated in Figure 33-5-13

Test procedure

1. Measure Vport at Rmax (S1 close).
   Rmax shall be adjusted to generate Iport_min=10mA at Vport.

2. Monitor Vport at PSE side (CC) and at PD side (DD).
   Disconnect PD load by turning off S1 at T_0.
   Use CH-1 as the trigger signal for measuring the timings.
   Verify that Vout has not changed during the first 300ms ($T_{1)}$ from T_0
   Verify that power is removed from the port within 400ms (T_2) max from $T_{0.}$
   Verify that Vport is less than 2.8Vdc within 500ms max from tx.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$44V \le Vport \le 57$$

Figure 33-5-13

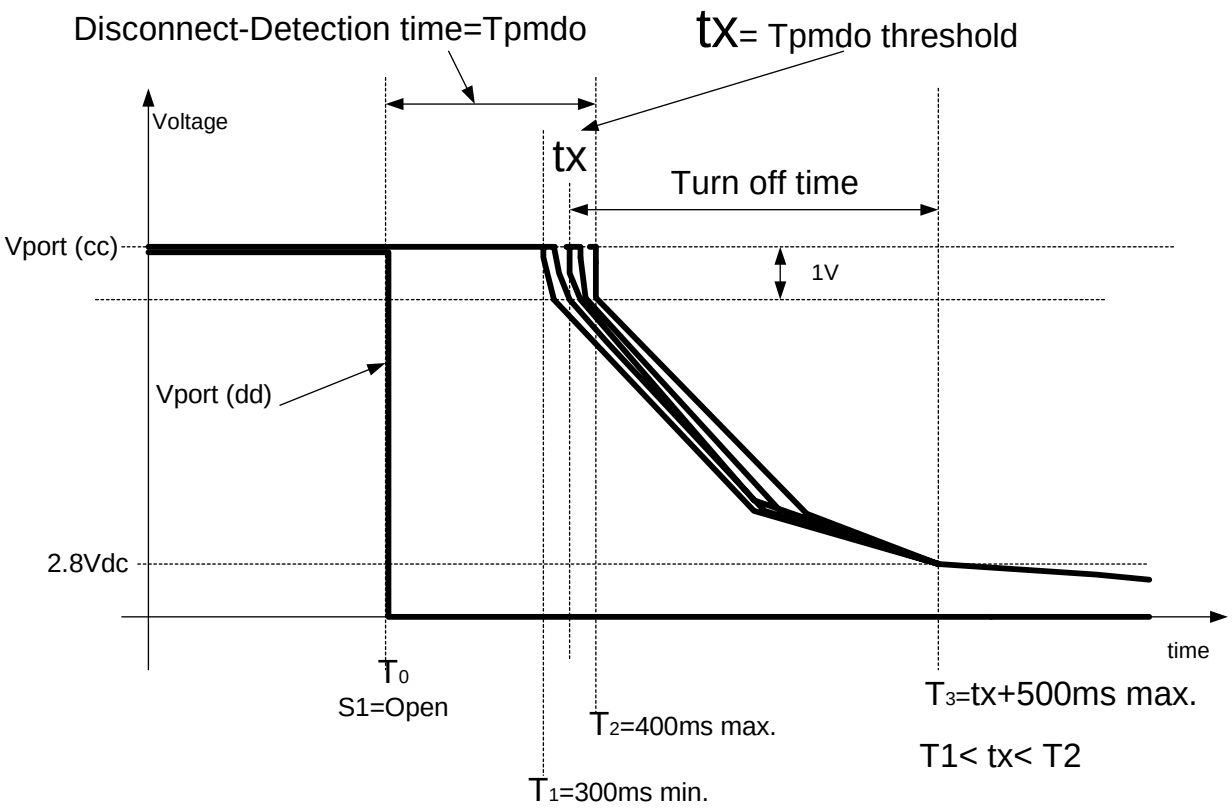


Figure 33-5-13.1

Table 33-5-Item 14: Continuous output power

See 33-5-1.

Table 33-5-Item 16: Power Turn On Time
Table 33-5-Item 19: Detection timing
Table 33-5-Item 20: Classification timing
Table 33-5-Item 21: Total Cycle time

Tested Parameters

1. PSE port turn on time after successful detection and optional classification, T_{PON}.
2. Detection timing, T_{DET}
3. Classification timing, T_{PDC}
4. Total Cycle time, T_{TOT} as function of $T_{DET} + T_{PDC} + T_{PON}$

Test setup

Will be tested as indicated in Figure 33-5-13

Test procedure

1. Wait 1sec min and measure Vport at Rmax (S1 close).
   Rmax shall be adjusted to generate Iport_min=10mA.
2. Open S1. Repeat step 1 and monitor the events vs. timings as illustrated in figure 33-5-16.1.

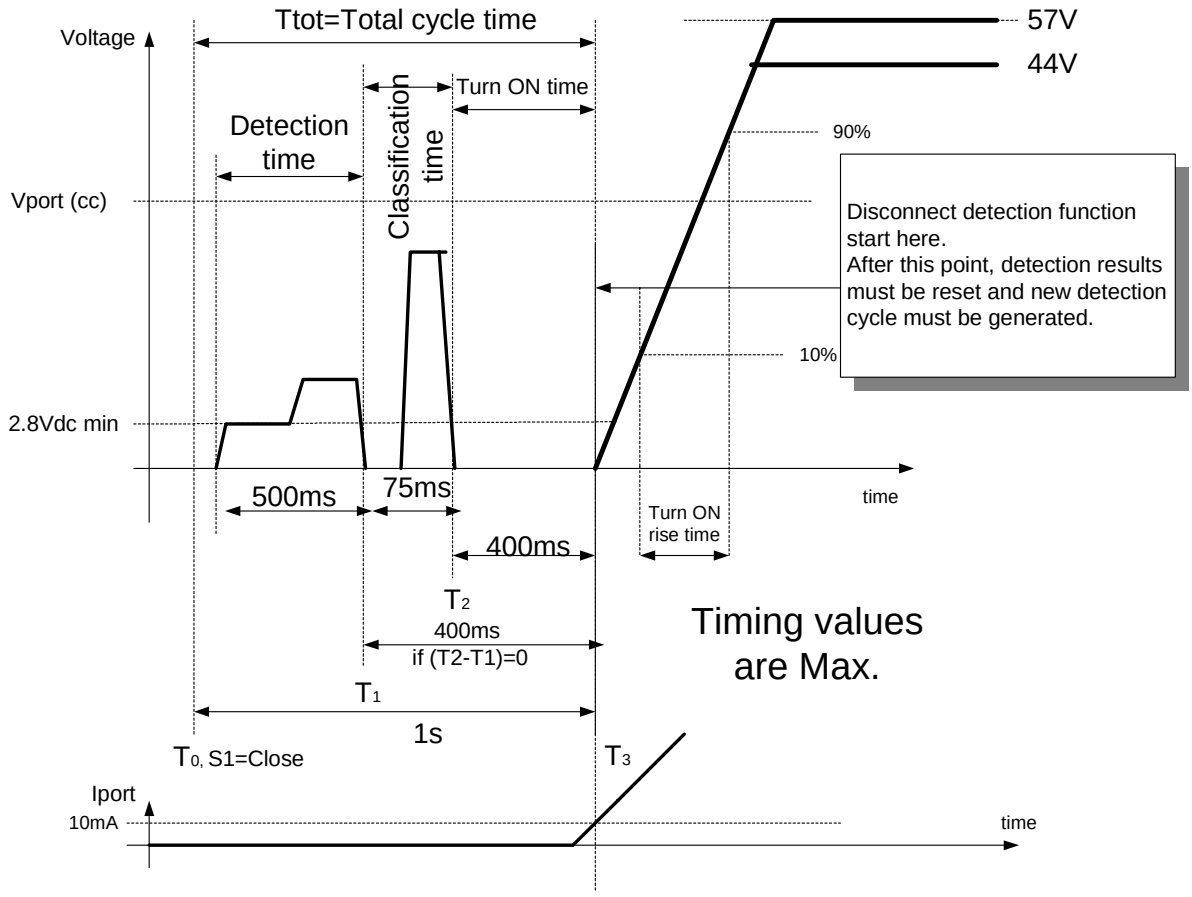


Figure 33-5-16.1

Table 33-5-Item 17: Detection back-Off Time

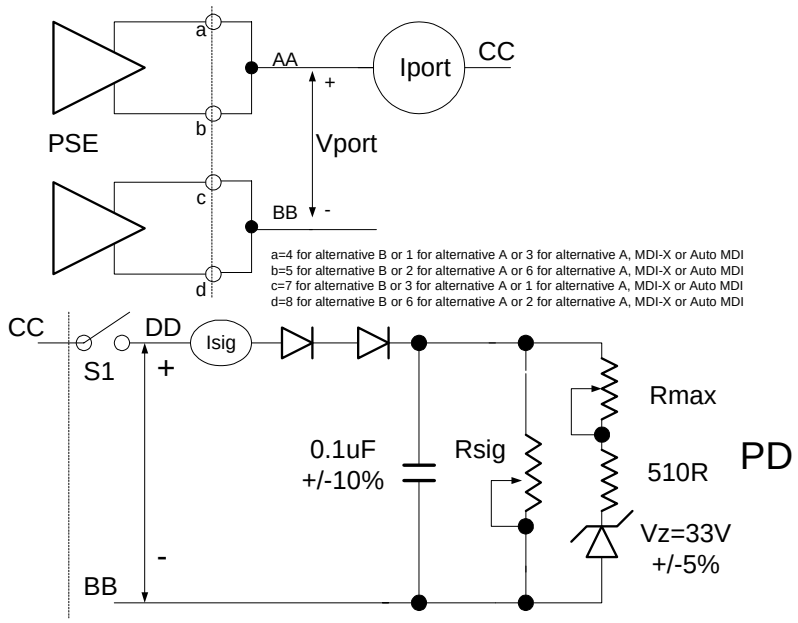
Test setup

Will be tested as indicated in Figure 33-5-17

Test procedure

1. Set Rsig to 24.9KΩ±1%. Close S1.
   Measure Vport at Rmax.
   Rmax shall be adjusted to generate Iport_min=10mA at Vport.
2. Open S1.
   Connect V1=2.9V±0.1Vdc source between points DD and BB. Record Isig1.
   Connect V2=3.9V±0.1Vdc source between points DD and BB. Record Isig2.
   Adjust Rsig until (V2-V1)/(Isig2-Isig1)=34KΩ±1%.
   Close S1.
   Verify that Vport voltage is less than 2.8V for 2sec minimum.

3. Open S1.
   Connect V1=2.9V±0.1Vdc source between points DD and BB. Record Isig1.
   Connect V2=3.9V±0.1Vdc source between points DD and BB. Record Isig2.
   Adjust Rsig until (V2-V1)/(Isig2-Isig1)=510KΩ±1%.
   Close S1.
   Verify that Vport voltages and timings are as defined in figure 33-5.16.1.



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$44V \le Vport \le 57$$

Figure 33-5-17

Table 33-5-Item 18: PSE port capacitance during detection

Tested Parameters

1. PSE port output capacitance during detection mode, C_{OUT}.

Test setup

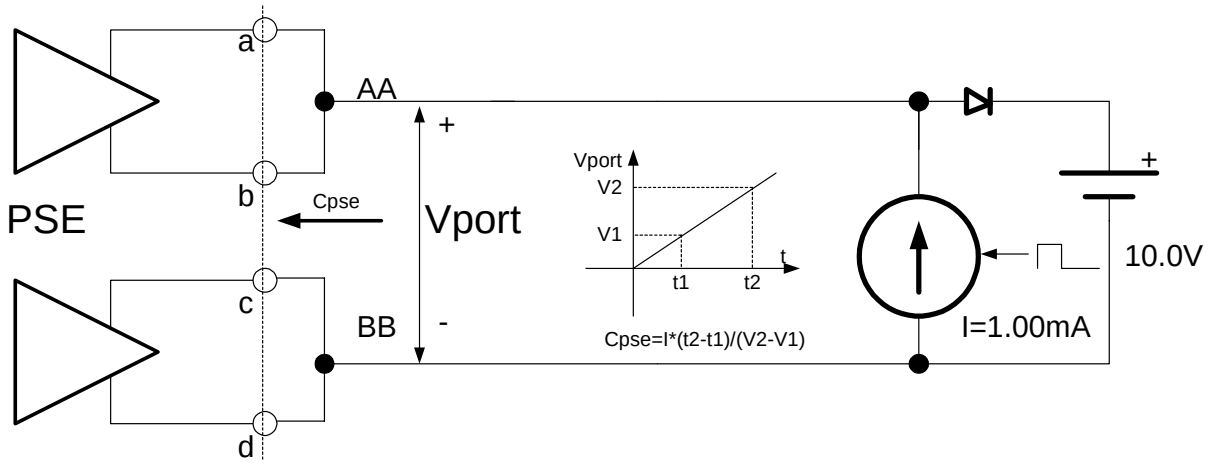
C_{OUT} is present at the port output during detection mode and during OFF mode and will be tested as indicated in Figure 33-5-18

Test procedure

1. Set PSE port to OFF mode.
   Connect switched current source, I to the PSE port.
   The current source voltage shall be clamped to 10V.
   Calculate Port capacitance by using the equation specified in figure 33-5-18.

2. Accurate LCR meter can be used as alternative. Test voltage should be less than 0.5Vpp.

3. Verify that PSE port capacitance is less than 520nF



a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI

Figure 33-5-18

Table 33-6-Items 1, 3, 4 and 5: AC disconnect pulse parameters
(Option (b) as indicated in paragraph 33.2.11)

Tested Parameters

1. AC voltage when PD is connected, V_close.
2. AC voltage when PD is disconnected, V_open.
3. Frequency of ac voltage, Fp.
4. AC signal slew rate, SR.
5. Disconnect detection time range, T_{PMDO}.
6. Max peak port voltage DC+AC, Vp.
7. AC input impedance, Zac1, Zac2 thresholds.

Test setup

Will be tested as indicated in Figure 33-6-1

Test procedure

1. Set Rsig1 value to have total of 26.25K with Rsig2=5MΩ and S1=close.
   Measure Vport and verify that $44V \leq Vport \leq 57$ and V_close<0.5Vpp
2. Monitor Vport at PSE side (CC) and at PD side (DD).
3. Disconnect PD by turning off S1 at T_0.
   Use CH-1 as the trigger signal for measuring the timings.
4. Verify that power is not removed during the first 300ms ($T_{1)}$ from T_0
5. Verify that power is removed from the port within 400ms (T_2) max from $T_{0.}$
   (Power is removed when Vport has dropped by 1V min)
6. Measure V_open, Fp, and Vp and SR. Use figure 33-6-1.1 for reference.

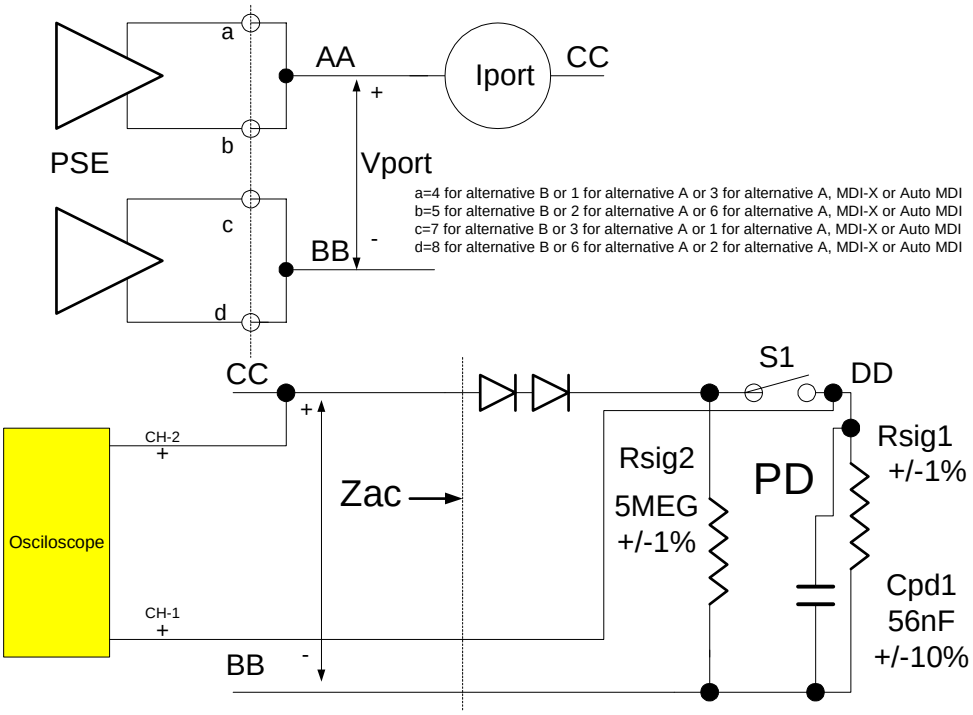


Figure 33-6-1

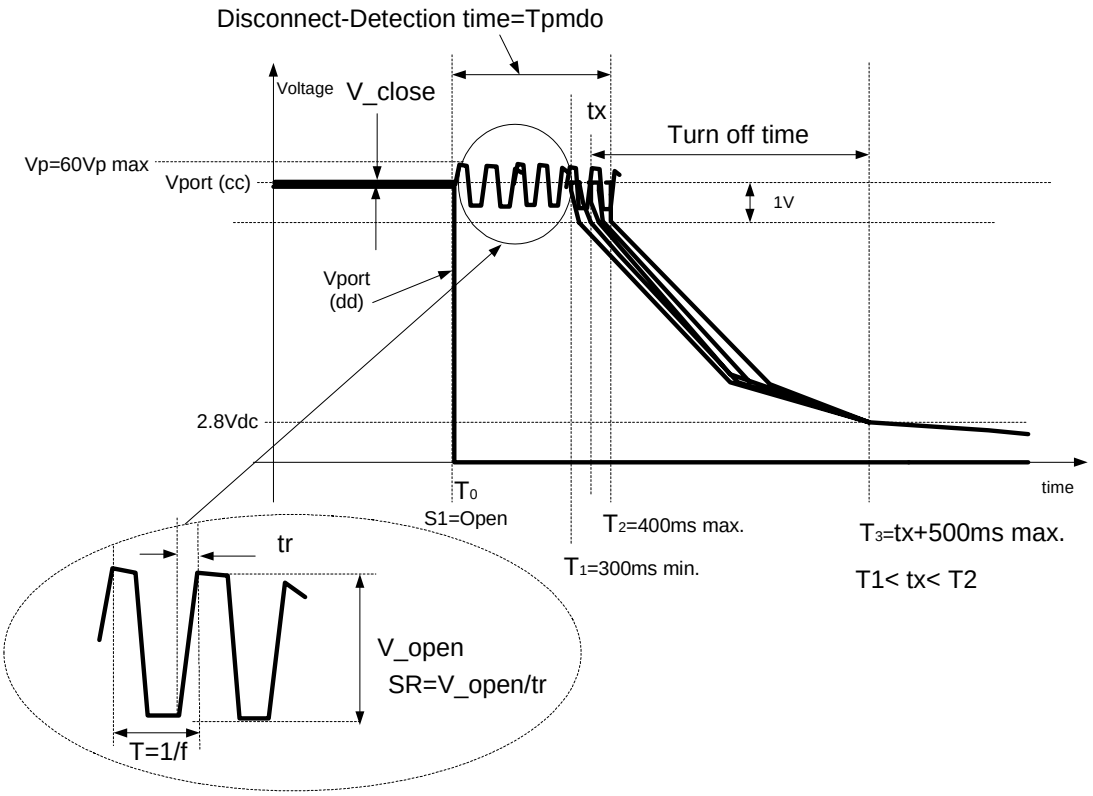


Figure 33-6-1.1

Table 33-6-Item 2: Port impedance.

Tested Parameters

1. AC source impedance, R_sac.
2. Port impedance during resistor detection mode, R_rev.
3. Zsource (Figures 33-6 and 33-7 in paragraph 33.2.5)
4. Detection short circuit current (Paragraph 33.2.5)

Test setup

Will be tested as indicated in Figure 33-6-2

Test procedure

1. Set S1=close. Monitor Iport. Verify that Iport is less than 5mA over 2sec period. (Ignore results of first 1ms)
2. Record V_open and its frequency Fp, from test 33-6-1 and calculate Ix[mApp]= V_open/5.
3. Verify that the Iport at frequency Fp is less than Ix over a 2 sec period (Ignore results of first 1ms)

4. Set S1=Open.
5. Verify that Vsense<3.625Vp ((30V-1V)*10K/ (70K+10K) over 2sec period. (Ignore results of first 26ms (5*10K*0.52uF)

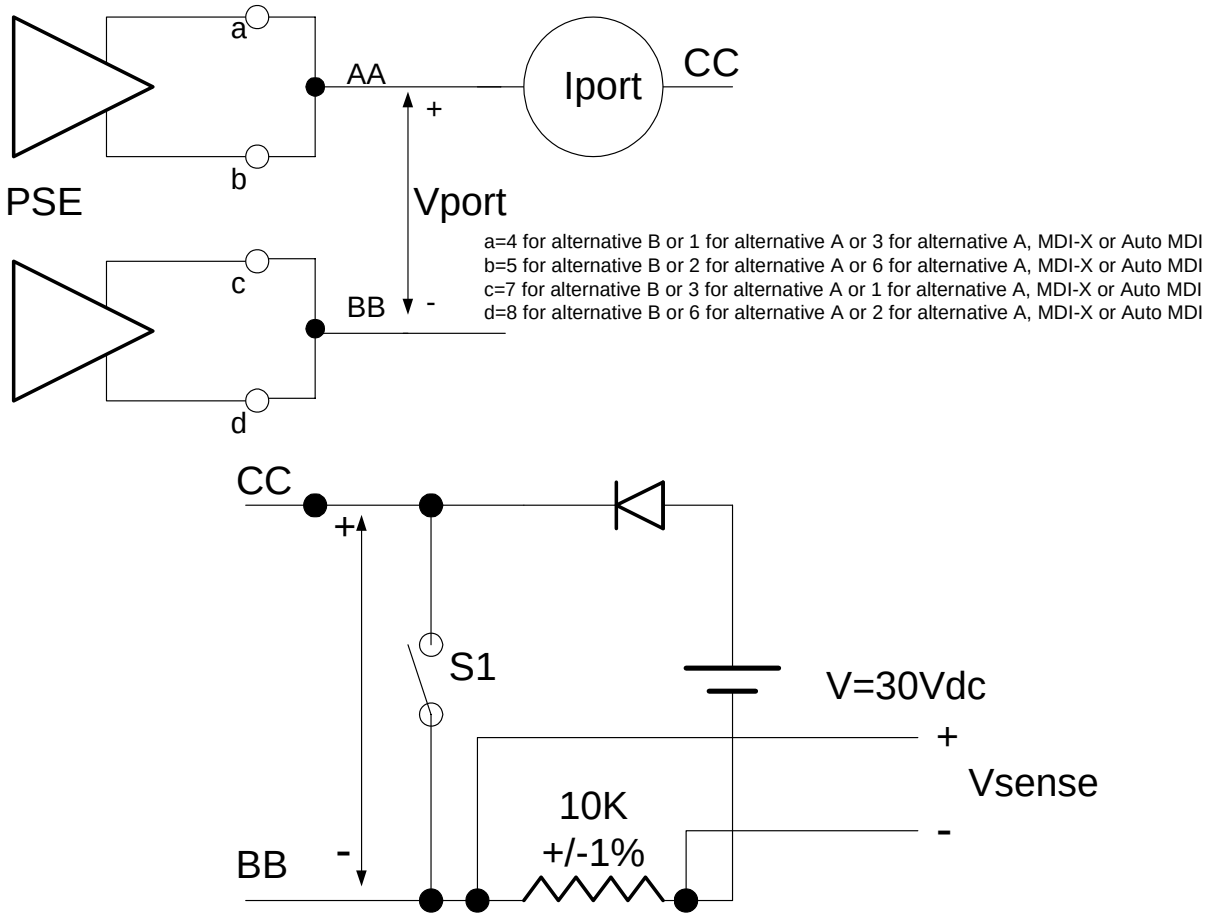

a
AA
Iport
CC
+
b
PSE
Vport
a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI
c
BB
-
d
CC
+
S1
V=30Vdc
+
Vsense
10K
+/-1%
-
BB
-

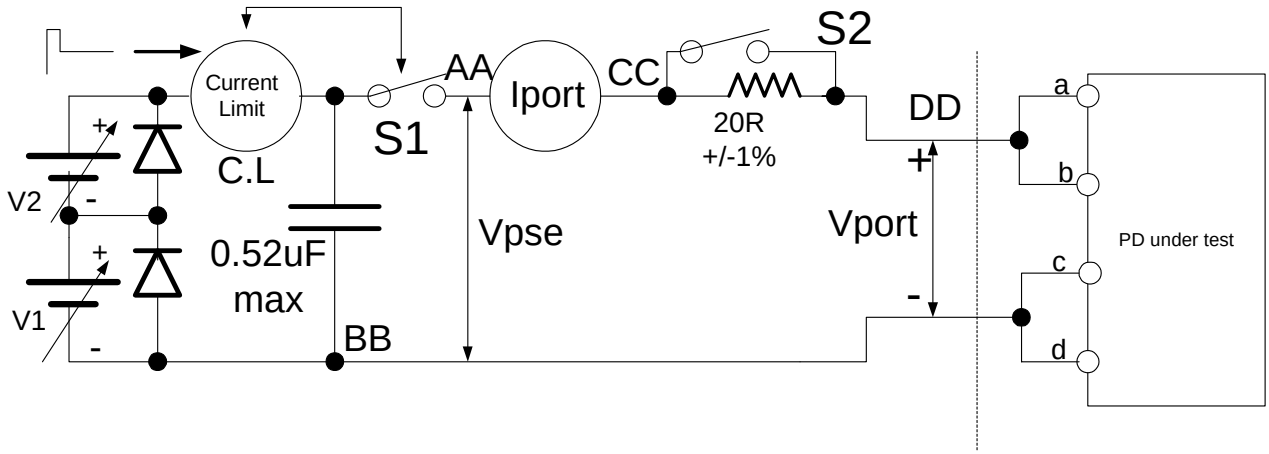
Figure 33-6-2

Test Procedure PD-1 (Table 33-13 parameters)

Test procedure PD-1 is used for testing:

a) PD turn off input voltage, Voff (Table 33-13, item 6b)
b) PD turn on input voltage, Von (Table 33-13, item 6a)
c) PD inrush current, I_{INRUSH} at Vpse=44Vdc (Table 33-13, item 5b)
d) PD inrush current time duration, T_{INRUSH} at Vpse=44Vdc (Table 33-13, item 5b)
e) PD inrush current, I_{INRUSH} at Vpse=57Vdc (Table 33-13, item 5b)
f) PD inrush current time duration, T_{INRUSH} at Vpse=57Vdc (Table 33-13, item 5b)
g) PD max average input current during normal powering mode at Vport=37Vdc, Iport (Table 33-13, item 5a)
h) PD max input power at 37Vdc, Pport_max (Table 33-13, item 2)
i) PD max input peak current at Vport=37Vdc and max load (Table 33-13, item 5c)
j) PD max average input current during normal powering mode at Vport=57Vdc, Iport (Table 33-13, item 5a)
k) PD max input power at 57Vdc, Pport_max (Table 33-13, item 2)
l) PD max input peak current at Vport=57Vdc and max load (Table 33-13, item 5c)
m) PD min input current at 37Vdc, Iport_min (Table 33-13, item 5a)
n) PD min input current at 57Vdc, Iport_min (Table 33-13, item 5a)
o) Polarity insensitive when PD implements Auto –MDI-X (33.3.1)
p) PD false under load timing limitations. (Table 33-13, item 2 note b)

Test procedure PD-1 uses Test Configuration PD-A as shown in figure 33-13-1
C.L is controlled current limit device with two threshold settings, CL1 and CL2.
CL1 and CL2 are is time limited to TCL1, TCL2. If Iport>=CL1 for t>TCL1 than S1 is open and test is failed.



a=4 for alternative B or 1 for alternative A, MDI-X or 3 for alternative A, MDI or Auto MDI-X
b=5 for alternative B or 2 for alternative A, MDI-X or 6 for alternative A, MDI or Auto MDI-X
c=7 for alternative B or 3 for alternative A, MDI-X or 1 for alternative A, MDI or Auto MDI-X
d=8 for alternative B or 6 for alternative A, MDI-X or 2 for alternative A, MDI or Auto MDI-X

Figure 33-13-1

Test Procedure PD-1 is as follows:

1. Set S1 to OFF. Set S2 to ON. Set V1 to 30.0V. Set V2=0.0V. Set CL1=CL2=1A.0A.

2. Set S1 to ON. Wait 1sec and verify that Iport<1.14mA (=30V/26.25KΩ)

3. Set S1 to OFF. Set S2 to OFF. Set V1 to 44.0V. Set V2=0.0V. Set CL1=0.4A, TCL1=50.0ms, CL2=350.0ma and TCL2=5sec. Set PD for max load mode.
4. Set S1 to ON.
5. Set S1 to ON and record the following parameters:
   I_{INRUSH}, T_{INRUSH}, V_{ON}. See figure 33-13-1.1 for reference.
6. Set S1 to OFF.
7. Set V1 to 57.0V. Set S1 to ON and record the following parameters:
   I_{INRUSH}, T_{INRUSH}, V_{ON}. See figure 33-13-1.1 for reference.

8. Set S2 to ON. Set V1 to 37.0V. Set V2=0.0V. Set CL1=0.4A, TCL1=50.0ms, CL2=350.0ma and TCL2=5sec. Set PD for max load mode.
9. Wait 1sec and record Ipor_dc and Iport_ac parameters. See figure 33-13-1.1 for reference.
10. Set V1 to 57V and repeat steps 8,9.

11. Set S2 to ON. Set V1 to 30.0V. Set V2=0.0V. Set CL1=0.4A, TCL1=50.0ms, CL2=350.0ma and TCL2=5sec. Set PD for max load mode.
12. Increase V1 until PD power supply turns ON. Verify that V1<=Von.

13. Set S1 to OFF. Set S2 to ON. Set V1 to 37.0V. Set V2=0.0V. Set CL1=0.4A, TCL1=50.0ms, CL2=350.0ma and TCL2=5sec. Set PD to min load operation.
13. Set S1 to ON. Wait 1sec and verify that Iport>=10mA
14. Set V1 to 57.0V. Verify that Iport>=10mA

15. If the PD implements Auto –MDI-X, repeat steps 3,4 and 5 and verify PD operation with reverse polarity connection.

16. Set V1=44V and V2=13V. Set PD to its minimum-operating load.
17. Wait 1sec until Iport is stable.
18. Set S3 to OFF and monitor Iport. Verify that Iport is less than 10mA for only T_{UNLD}<290ms. If Iport is not less for 10mA for any time duration, than timing requirement is ignored. See figure 33-13-1.2 for reference.

19. Set S1 to OFF. Verify that Iport<1.14mA at Vport>30.0V. Verify that Vport is less than 2.8V within 0.5sec max from the time S1 was turned OFF.
    If this requirement can't be met, PD vendor shall specifically define the time required to wait after PD disconnection for re-connection to the MDI port. . In any case this time shall note be more than 5sec

20. Verifying PD input capacitance during normal operating mode:
    Set S1 to OFF. Set S2 to ON. Set V1 to 57.0V. Set V2=0.0V. Set CL1=CL2=1.0A, TCL1=TCL2=10sec. Set PD for constant load.
21. Set S1 to ON.
22. Wait 1sec and measure Iport.
23. Set S1 to OFF while monitoring Vport. Measure the time duration, Tdrop for Vport to drop from 57.0 to 56V.0.
    Calculate C=Iport*Tdrop/1V. Verify that 5uF<C<180uF.

    If C>180Uf, Set CL1=CL2=1.0A. TCL1=TCL2=5s.
    Repeat all tests regarding inrush current limitation and verify that inrush current is limited by the PD to 0.4A max.

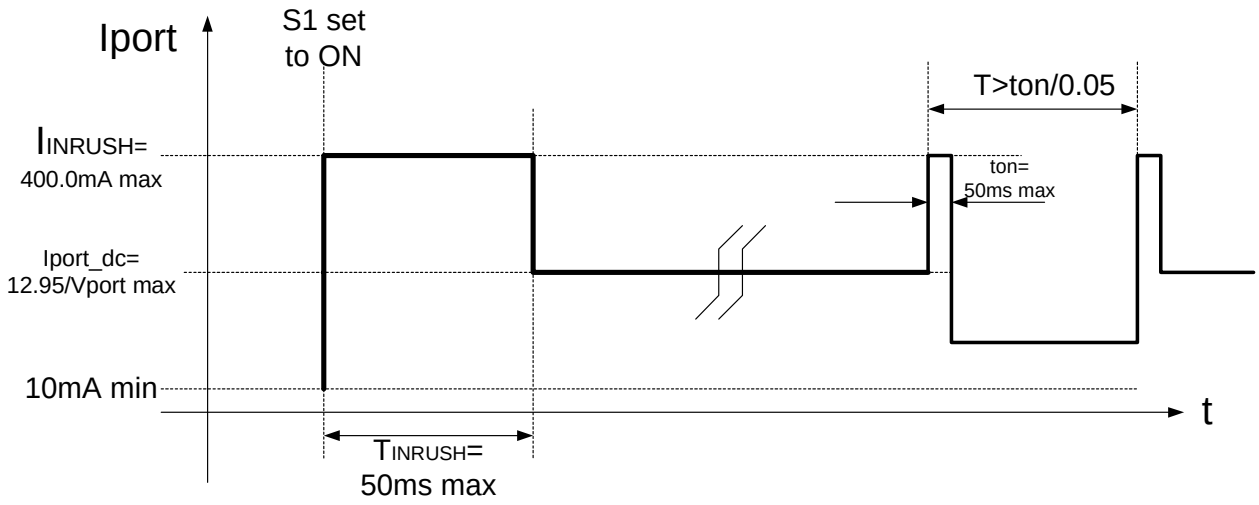


Figure 33-13-1.1

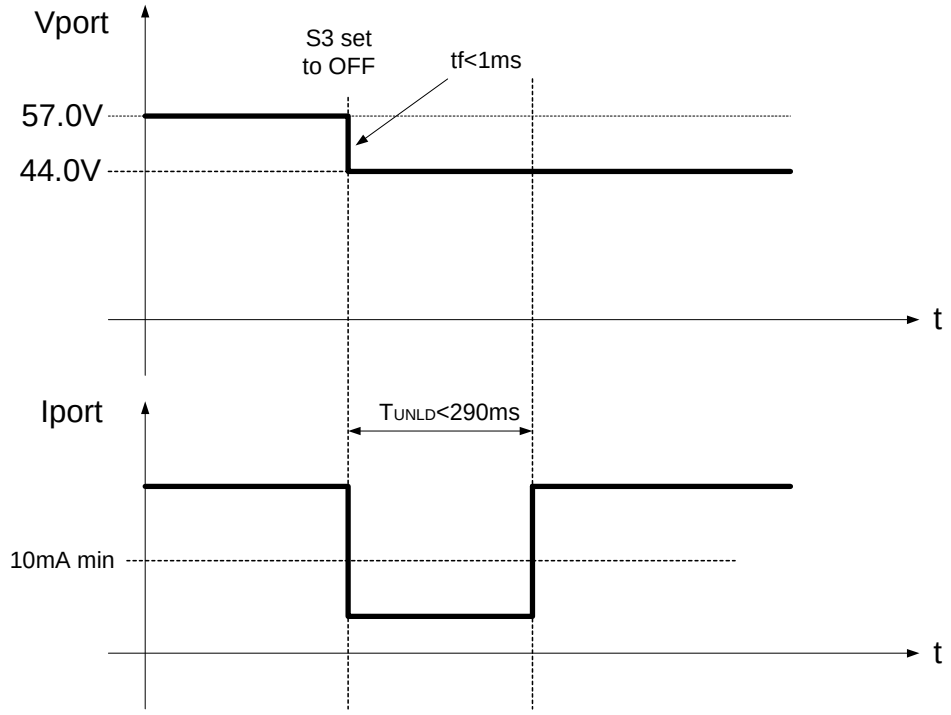


Figure 33-13-1.2

Test Procedure SIG-1, PD signature characteristics.

Tested Parameters

1. V-I slope (Table 33-8)
2. Voffset (Table 33-8)
3. Input capacitance (Table 33-8)

Test setup

Will be tested as indicated in Figure 33-8-1

Test procedure

1. Set S1 to ON, S2 to OFF. Limit the current of V_N to 4-5mA.
2. Change V_N from 2.70V to 10.1V in steps of 0.370V and measure I_N for each V_N value.
3. Calculate $Rsig_N = (VN_{+1} - V_N)/(IN_{+1} - I_N)$
4. Verify that $23.75K\Omega <= Rsig_N <= 26.25K\Omega$

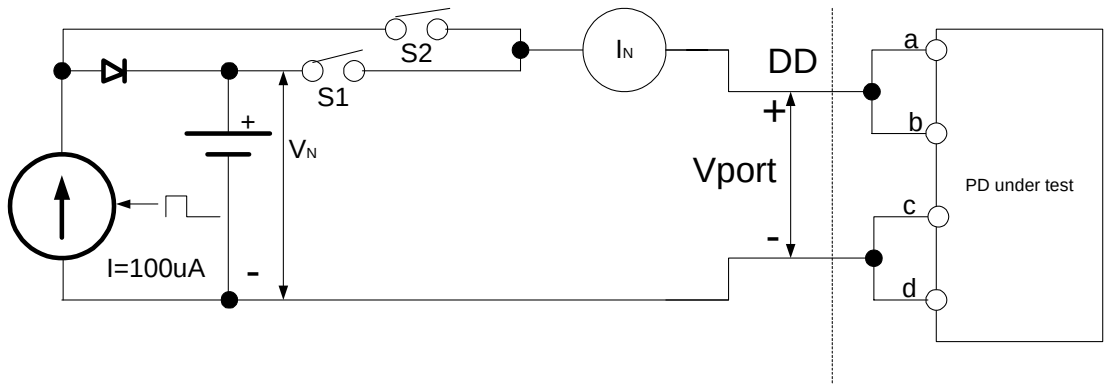
Note: The concept of this setup is to measure the equivalent Rsig as seen at the PD port and includes all possible errors caused by series diode voltage drop (V_{OFFSET}), leakage current (I_{OFFSET}) and component accuracy.
Rsig is calculated with minimum of two point measurements to simulate PSE operation.

5. Change V_N from 0.00V to 2.70V in steps of 0.20V and measure I_N.
6. Plot the results of I_N vs V_N from steps 1 and 5 and find V_{OFFSET}. See figure 33-8-1.1 for reference.

7. Set S1 to OFF, S2 to ON. Set V_N to 10.0V.
8. Activate the switched current source.

Note: The concept of this setup is to calculate capacitance value by ramping the capacitance voltage with constant current source and using the equation I*t=V*C. This method is useful when series diodes are present.

9. Calculate Port capacitance by using the equation specified in figure 33-8-1.2.
10. Accurate LCR meter can be used as alternative. Test voltage should be less than 0.5Vpp.
11. Verify that PD port capacitance is between 50nF to 110nF.



a=4 for alternative B or 1 for alternative A, MDI-X or 3 for alternative A, MDI or Auto MDI-X
b=5 for alternative B or 2 for alternative A, MDI-X or 6 for alternative A, MDI or Auto MDI-X
c=7 for alternative B or 3 for alternative A, MDI-X or 1 for alternative A, MDI or Auto MDI-X
d=8 for alternative B or 6 for alternative A, MDI-X or 2 for alternative A, MDI or Auto MDI-X

Figure 33-8-1

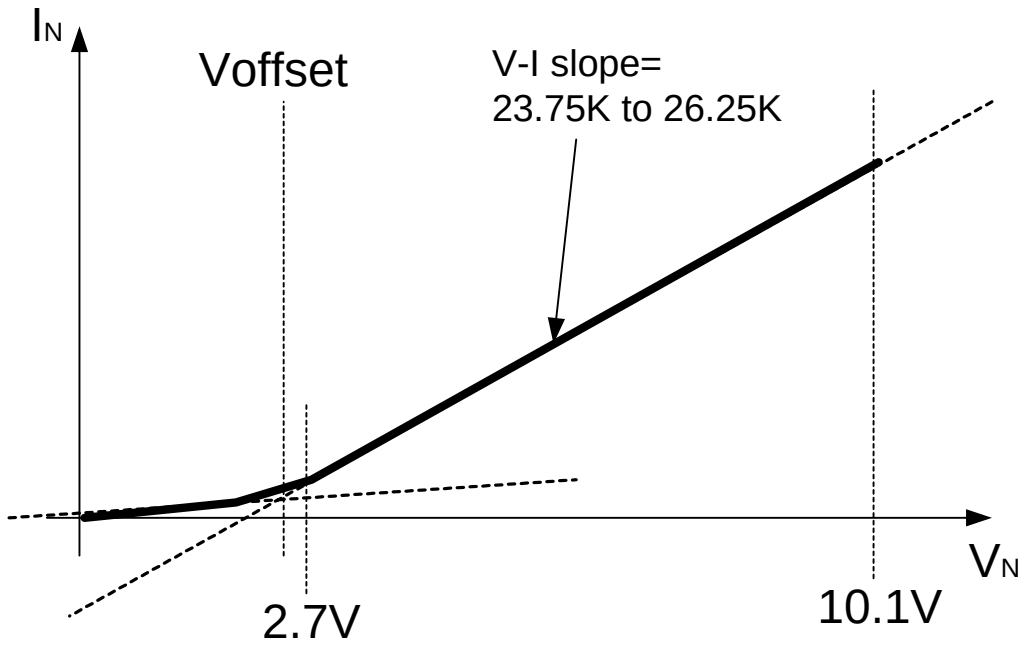
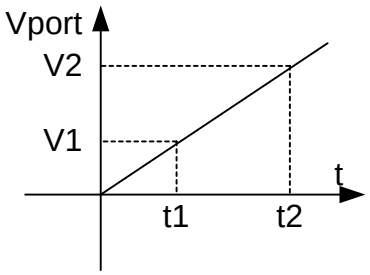


Figure 33-8-1.1



Cpd=I*(t2-t1)/(V2-V1)

Figure 33-8-1.2

Test Procedure SIG-2, PSE signature detection.

Tested Parameters

1. PSE port impedance during detection– See test procedure PSE-14
2. Parallel diode across the port (Paragraph 33.2.5 figures 33-6 and 33-7)
3. Detection open circuit voltage (Paragraph 33.2.5)
4. Detection short circuit current (Paragraph 33.2.5)
5. Detection minimum/maximum Voltages (Paragraph 33.2.5.1)
6. Two-point detection voltage difference (Paragraph 33.2.5.1)
7. Detection Criteria (Paragraph 33.2.6.1)
8. Rejection Criteria (Paragraph 33.2.6.2)
9. Detection voltages slew rate (Paragraph 33.2.5.1)
10. Detection and Power on the same leads (Paragraph 33.2.6.3)

Test setup

Will be tested as indicated in Figure 33-2-5

Test procedure
Set S1, S2 and S3 to OFF.

Step 1: Parallel diode across the port (Paragraph 33.2.5 figures 33-6 and 33-7)
1. Turn system OFF (No voltages across PSE port). Set V1 to 5.0V. Set S1 and S2 to ON. S3=OFF.
2. Measure Iport. Verify that Iport>3mA.
3. Reverse V1 polarity. Verify that Iport < 40uA
4. Set S2 to OFF.

Step 2: Detection open circuit voltage (Paragraph 33.2.5)

1. Set S1, S2 and S3 to OFF
2. Verify that Vport < 30Vp during the detection phase for 500ms max out of 1sec period.
   Verify that Vport average is <=2.8Vdc when the PSE is not in detection phase.
3. Verify that Voltages slew rate is less than 0.1V/uS
4. It is allowed to have no detection signals or single point detection if the PSE identifies that the Port is open.

Step 3: Detection short circuit current (Paragraph 33.2.5)

See Test Procedure PSE-14.

Step 4:
Detection minimum/maximum Voltages (Paragraph 33.2.5.1)
Two-point detection voltage difference (Paragraph 33.2.5.1)
Two-point detection voltage difference.
Detection Criteria (Paragraph 33.2.6.1)
Rejection Criteria (Paragraph 33.2.6.2)
Detection voltages slew rate (Paragraph 33.2.5.1)
Detection and Power on the same leads (Paragraph 33.2.6.3)

Step 4.1

1. Set Rs=0. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 23.75KΩ. , Adjust Rsig to 19.0K by adjusting Rp.
3. Adjust V_{OFFSET} to 2.0V

Step 4.2

1. Set S1 and S3 to ON. Set S2 to OFF.
2. Measure detection voltages V1 and V2.
   Verify that V1 and V2 are between 2.8V to 10V and |V2-V1|>=1V
3. Verify that 44V min connected to the port for 299ms min.
4. Verify that the slew rate of all the switched voltages is less than 0.1V/us.

Step 4.3

1. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 26.25KΩ. Set Rp=Open. Adjust Rsig to 26.5KΩ by adjusting Rs.
3. Adjust V_{OFFSET} to 2.0V
4. Repeat step 4.2

Step 4.3
1. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 15KΩ. Set Rs=0. Adjust Rsig to 14.9KΩ by adjusting Rp.
3. Adjust V_{OFFSET} to 2.0V.
4. Set S1 and S3 to ON. Set S2 to OFF.
5. Verify that power is not applied to the port.

Step 4.4

1. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 33.0KΩ. Set Rp=Open. Set Rsig=0.
3. Adjust V_{OFFSET} to 2.0V.
4. Set S1 and S3 to ON. Set S2 to OFF.
5. Verify that power is not applied to the port.

Step 4.4

1. Set Rsig1=24.9KΩ. Set Rp=Open. Set Rsig=0. Set Csig=10.0uF
2. Adjust Voffset for 2.0V.
3. Set S1 and S3 to ON. Set S2 to OFF. Verify that power is not applied to the port.
4. Repeat step 4.4 for Rsig1=open.

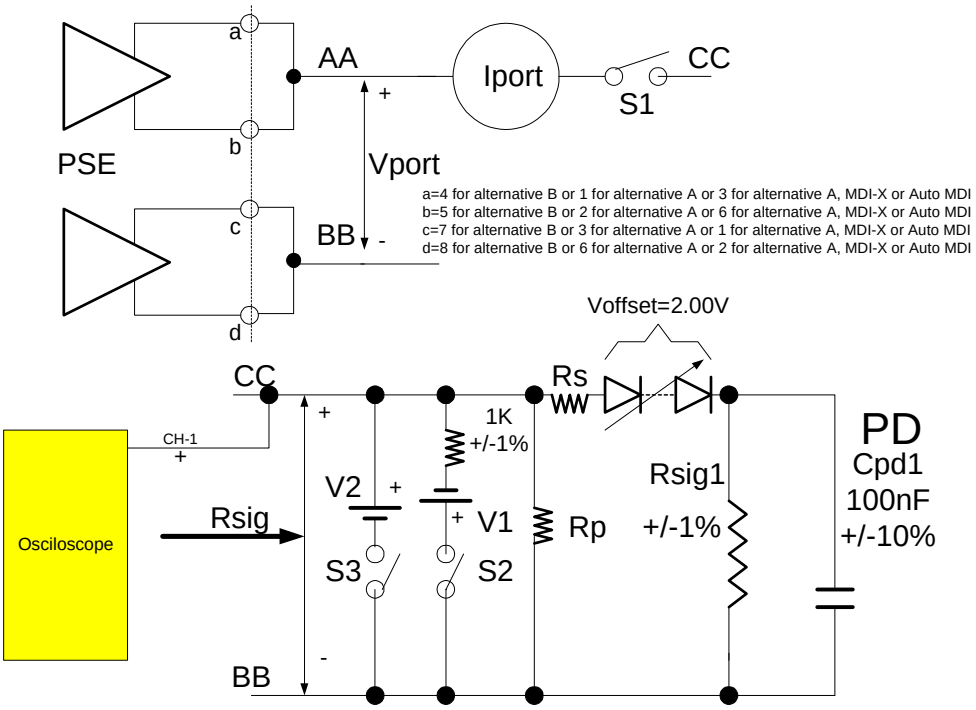

a
b
c
d
PSE
AA
Iport
CC
S1
+
Vport
-
BB
a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI
Voffset=2.00V
CC
Rs
PD
Cpd1
100nF
+/-10%
1K
+/-1%
Rsig1
+/-1%
CH-1
+
Osciloscope
Rsig
V2
V1
Rp
S3
S2
BB

Figure 33-2-5

To be added in draft 3.1 to paragraph 33.2.9

33.2.9.xxx PSE-PD stability - PSE requirements

In order to prevent the potential for oscillations between PSE and PD the PSE port output impedance (Zo_port) + the cable impedance (Zc) + the PD input port circuitry impedance (Zpd_cir) + the PD EMI output filter impedance (Z_emi) should be lower that the PD power supply input impedance (Zin_ps_pd).
This paragraph will be focused on the PSE part.

Port output impedance consist of two parts:
a) PSE power supply output impedance (Zo_ps) followed with
b) Series elements (Z_ser) which connect the PSE power supply output to the port so the total Port output impedance during normal powering mode is Zo_port=Zo_ps+Z_ser .
Zo_ps is function of the load (Pport)

In order to maintain PSE-PD stability the following principles should maintain:
a)- Zo_ps max =300miliOhm at frequencies up to 100Khz at Pport=15.4W .
Zo_ps can be extracted from Zport by measuring Vport/Iport (with external power dynamic analyzer system) as function of frequency and subtracting from Zport the value of Zser (f=DC) which is limited by the value of Zser at DC (low frequency)
b)- If Zo_ps<Zo_ser and Vport is kept to be 44V min, 57Vmax during dynamic load changes from DC to 100Khz than the value of Zo_ps is not limited.

Compliance to the above requirements should be made by measuring Port output impedance from DC to 100KHz at 15.4W load at short cable length or by presenting simulation results.
See Figure 33-5.xx1 for PSE-PD system impedance allocation and figure 33-5.xx2 for test setup.

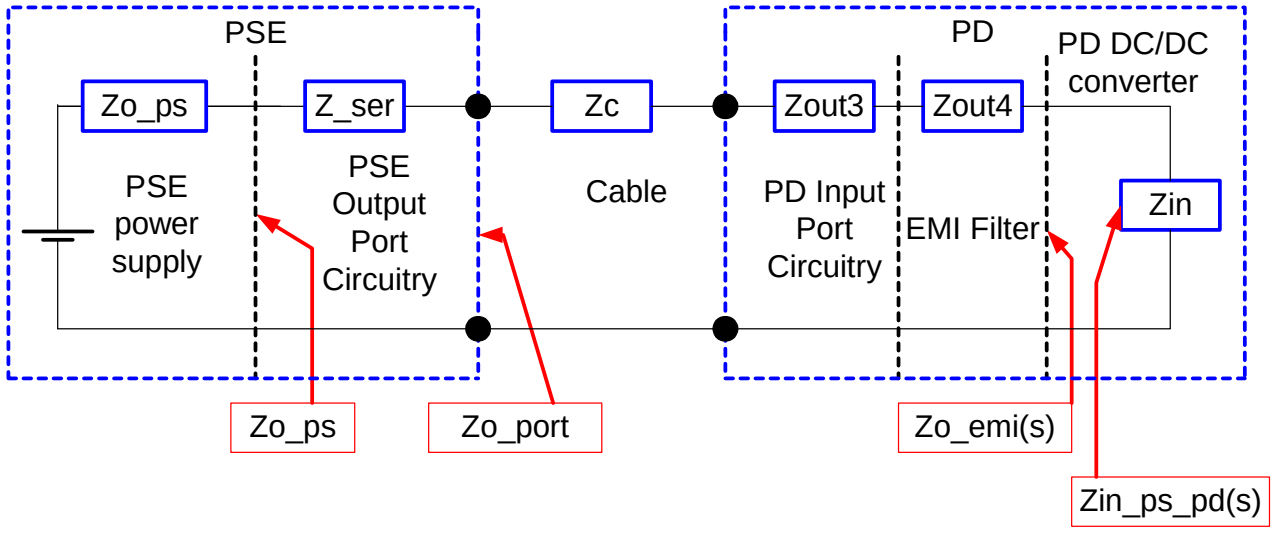


Figure 33-5.xx1-PSE-PD system impedance allocation

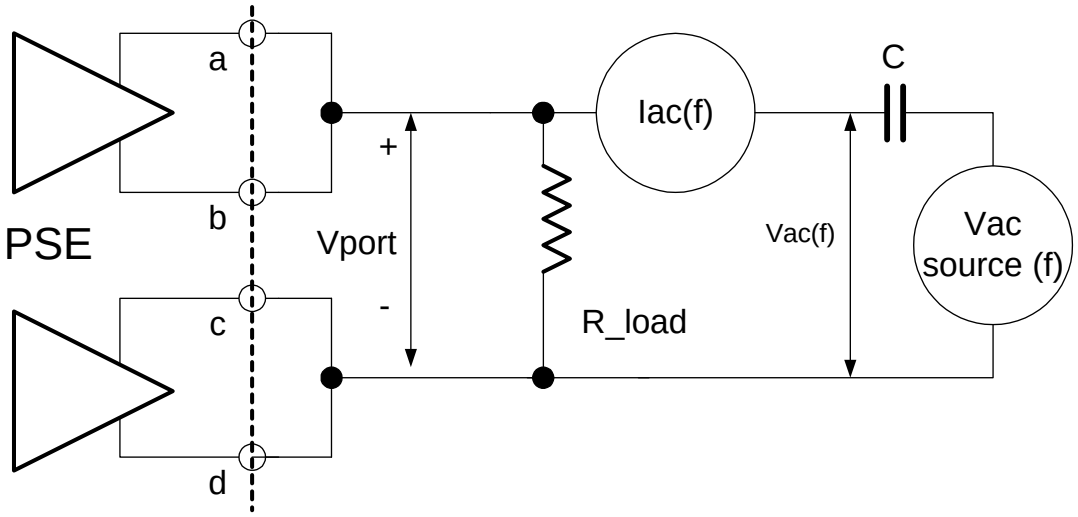


Figure 33-5.xx2-Test setup for measuring Zo_port

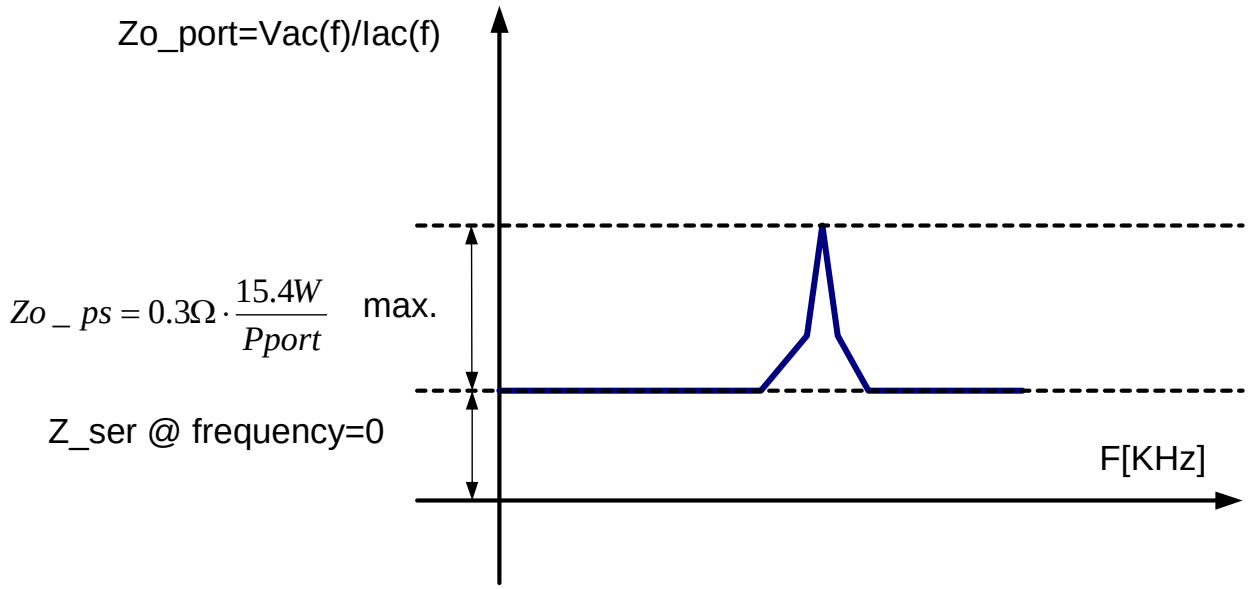


Figure 33-5.xx2.1-Test requirements for measuring Zo_port

To be added in draft 3.1 to paragraph 33.3.5

33.3.5.xxx PSE-PD stability - PD design guidelines

PD Port input impedance consist of two parts: a) PD input circuits including EMI filter (Zin_ser) and b) PD power supply input impedance (Zin_ps_pd) which is fed by the output of the EMI filter (Zo_emi).

In order to maintain stability with the PSE, The PD power supply input impedance (Zin_ps_pd) should be higher than the output impedance of the total network including the PD EMI output filter impedance fed by the cable (MDI) output impedance which is fed by the PSE port output impedance.

The worst case is when the cable (MDI) length is zero.

Due to the fact that the access to the PD input power supply is not possible through the PD port for evaluating the various impedances and derivation of the above parameters from measuring the PD input impedance is complicated, the following guide lines should be followed by the PD vendor:

a) PD power supply input impedance (Zin_ps_pd) at max load of Pport=12.95W should be higher than 30 Ohm at any frequency up to PD Power supply feedback crossover frequency.
If PD power supply is consuming less than Pport=12.95W than Zin_ps_pd min=30*12.95/Pport

b) PD power supply EMI filter output impedance should be Zo_emi=2.7 ohm max.
If PD power supply is consuming less than Pport=12.95W than Zo_emi=2.7*12.95/Pport

c) If the PD power supply is implemented by Linear Voltage regulator than the above requirements a) and b) can be ignored.

See Figure 33-5.xx1 for PSE-PD system impedance allocation