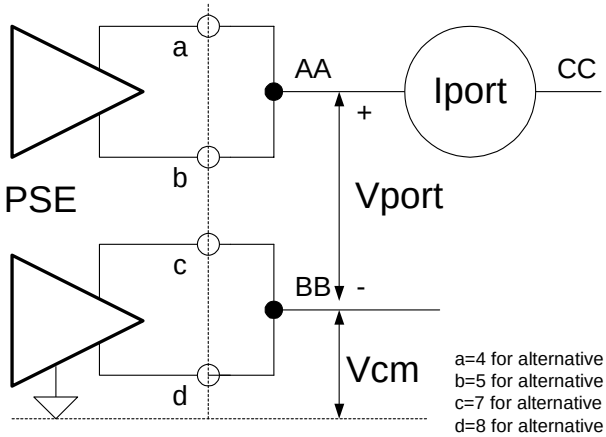
IEEE802.3af
DTE Power via MDI task Force.

Annex to my comments for draft 3.1 with updates for draft 3.1 drawings according to July/2002 meeting during the comment resolution process.

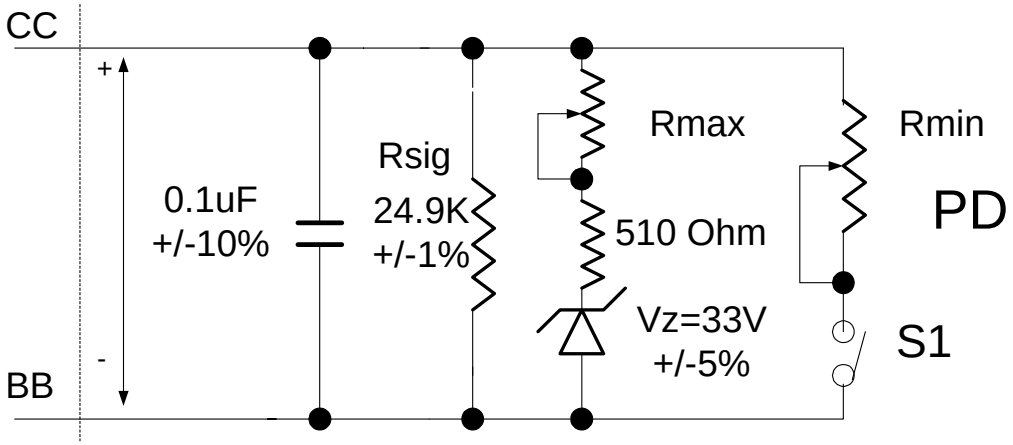
Rev 002

Yair Darshan

July 11, 2002



a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI

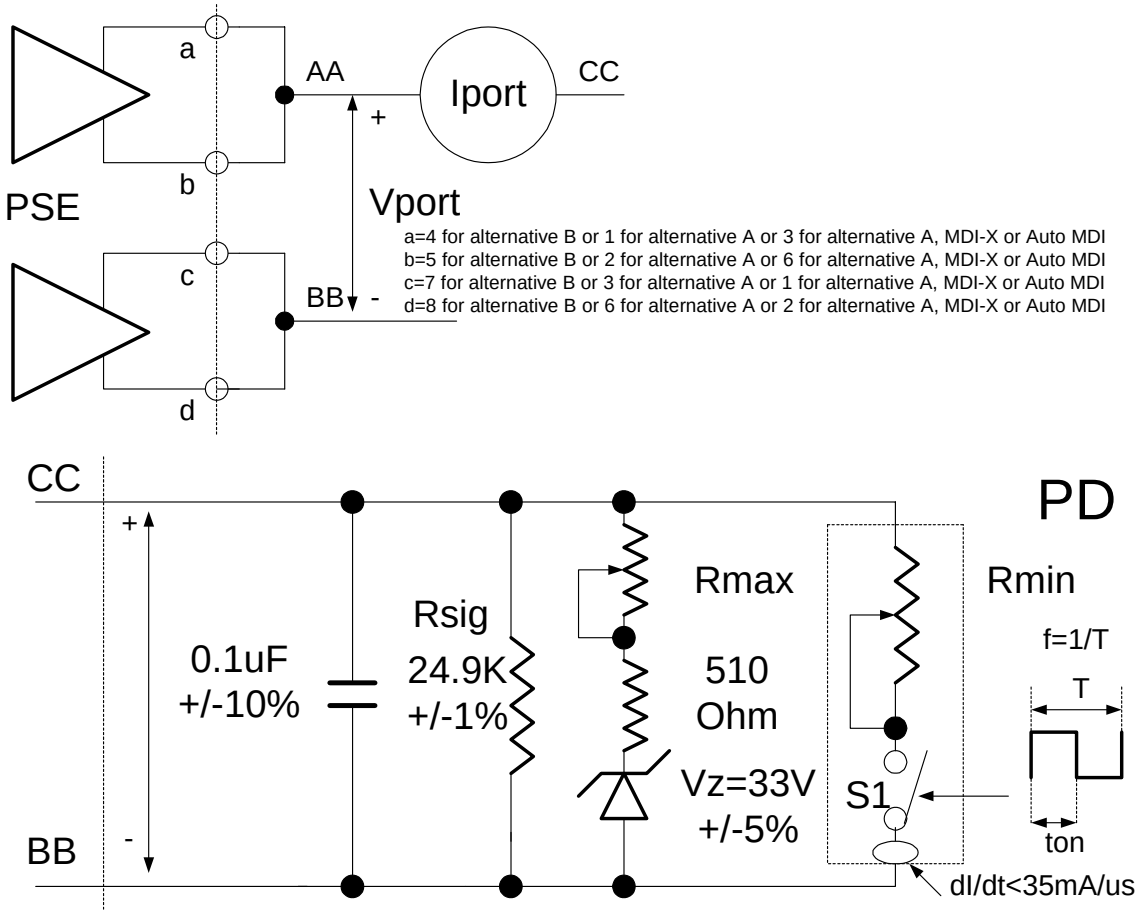


$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$R\min < \frac{Vport^2}{15.4 - Vport * Iport\_\min}$$

$$44V \le Vport \le 57$$

Figure 33-9



$$R\max < \frac{(Vport - Vz)}{10mA} - 510$$

$$R\min < \frac{Vport^2}{15.4 - Vport * Iport\_\min}$$

$44V \le Vport \le 57$

Figure 33-10

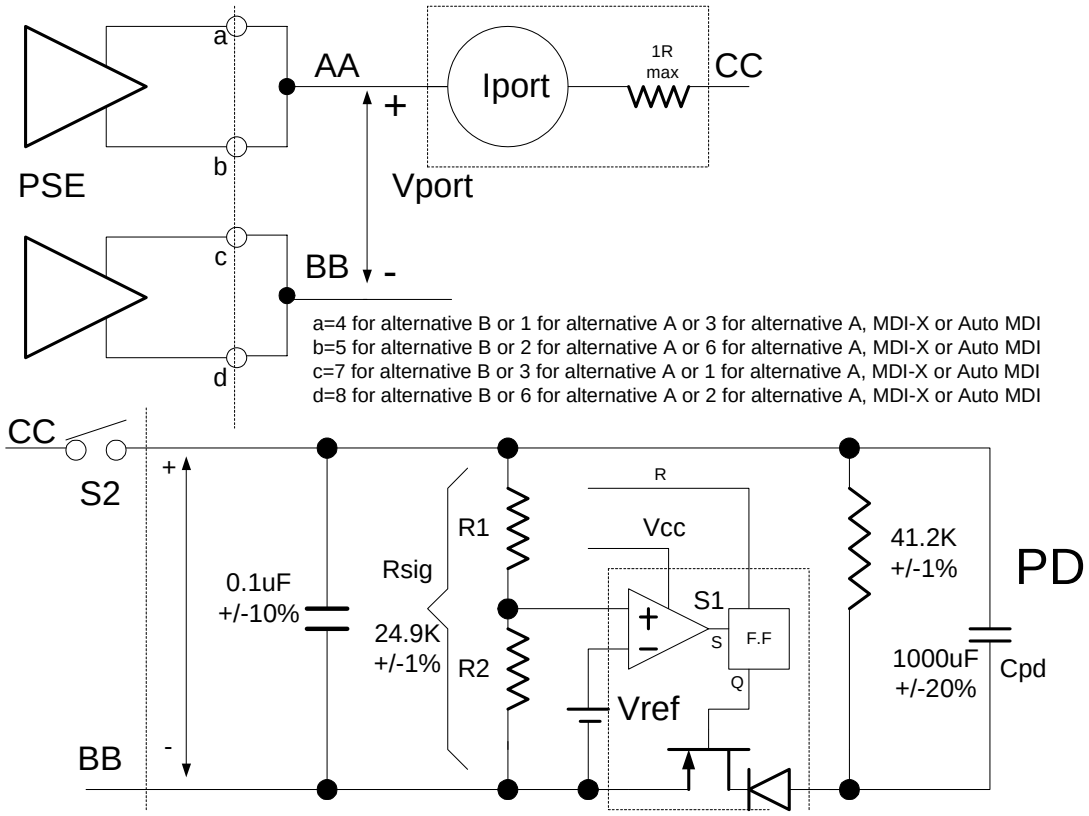

a
b
c
d
PSE
AA
BB
+
-
Vport
Iport
1R
max
CC
a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI
CC
S2
+
-
BB
0.1uF
+/-10%
Rsig
24.9K
+/-1%
R1
R2
R
Vcc
S1
S
F.F
Q
Vref
41.2K
+/-1%
1000uF
+/-20%
Cpd
PD

Figure 33-11

(Comments (T/TR) 415, 335, 166, 167) (Applies to figures 33-12 and 33-16)

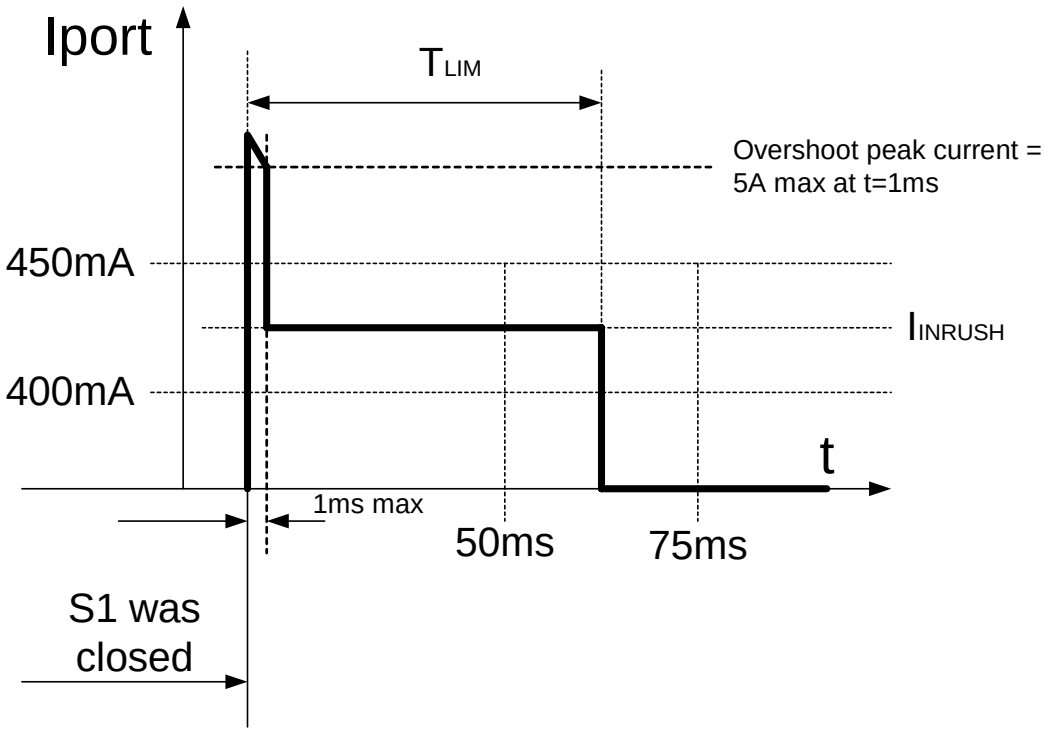


Figure 33-12

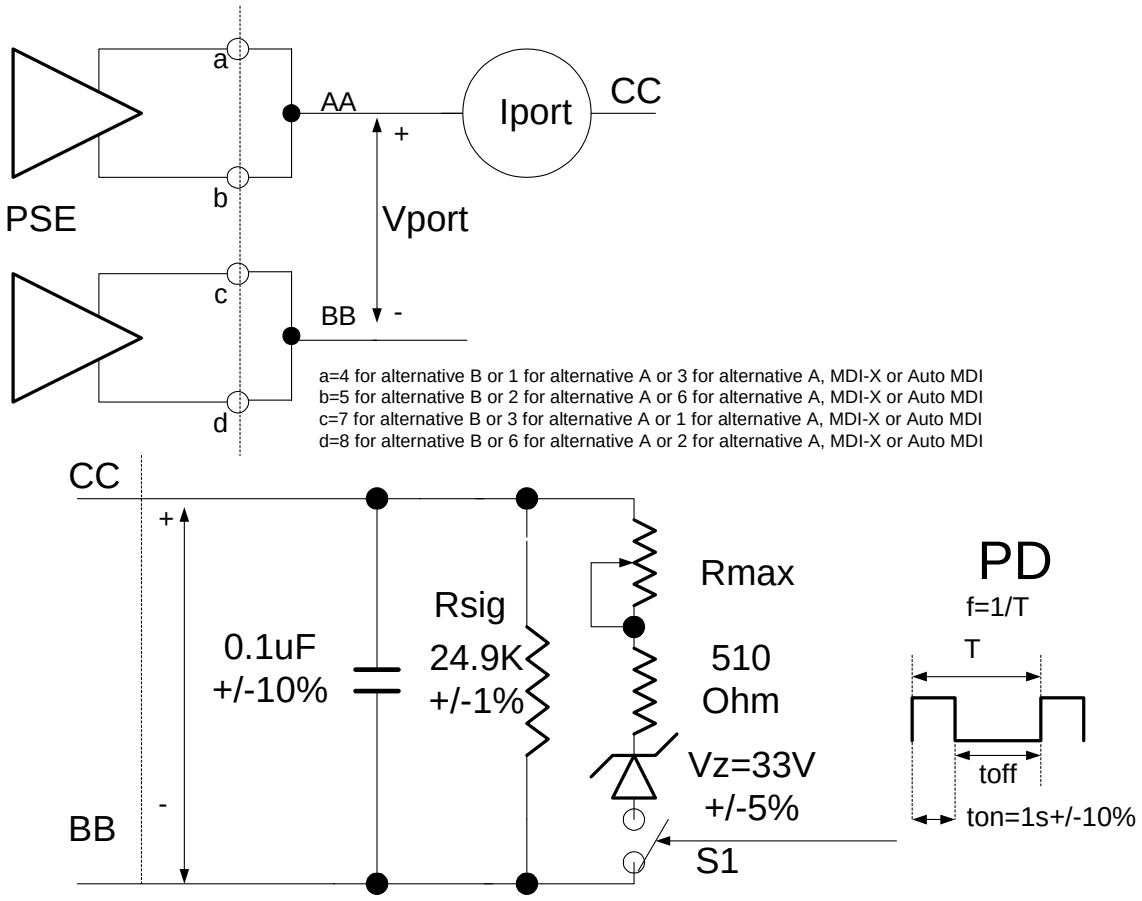

a
b
c
d
AA
BB
+
-
Iport
CC
Vport
PSE
a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI
CC
+
-
BB
0.1uF
+/-10%
Rsig
24.9K
+/-1%
Rmax
510
Ohm
Vz=33V
+/-5%
S1
PD
f=1/T
T
toff
ton=1s+/-10%

Figure 33-13

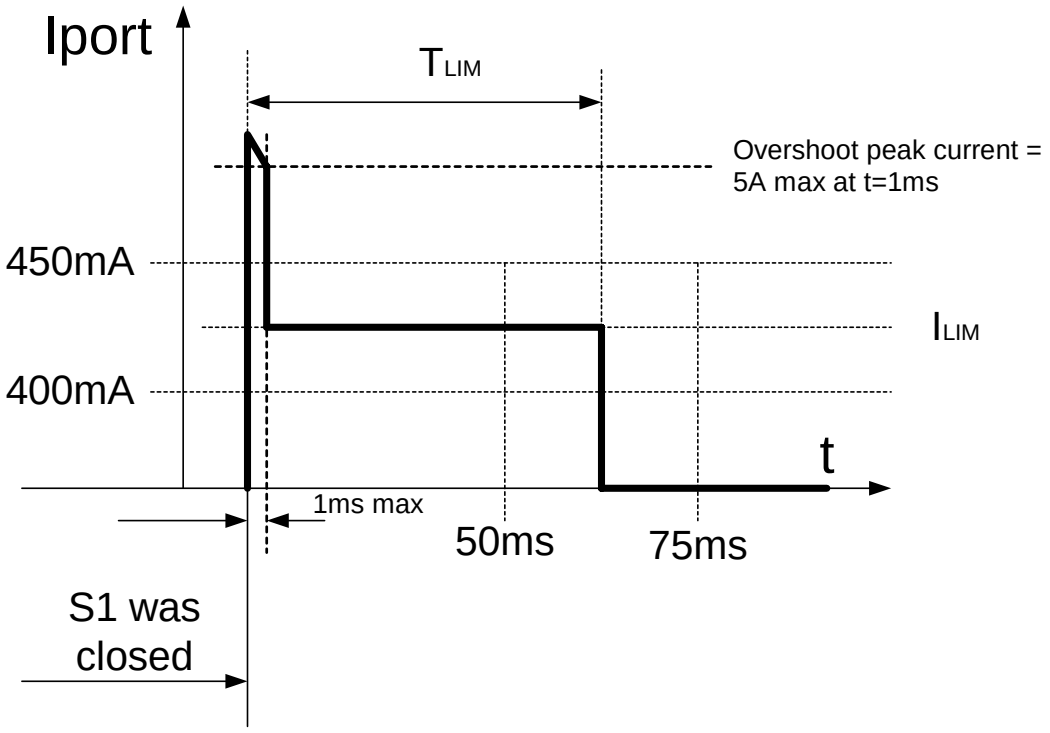

Iport
T LIM
Overshoot peak current =
5A max at t=1ms
450mA
I LIM
400mA
t
1ms max
50ms
75ms
S1 was
closed

Figure 33-16

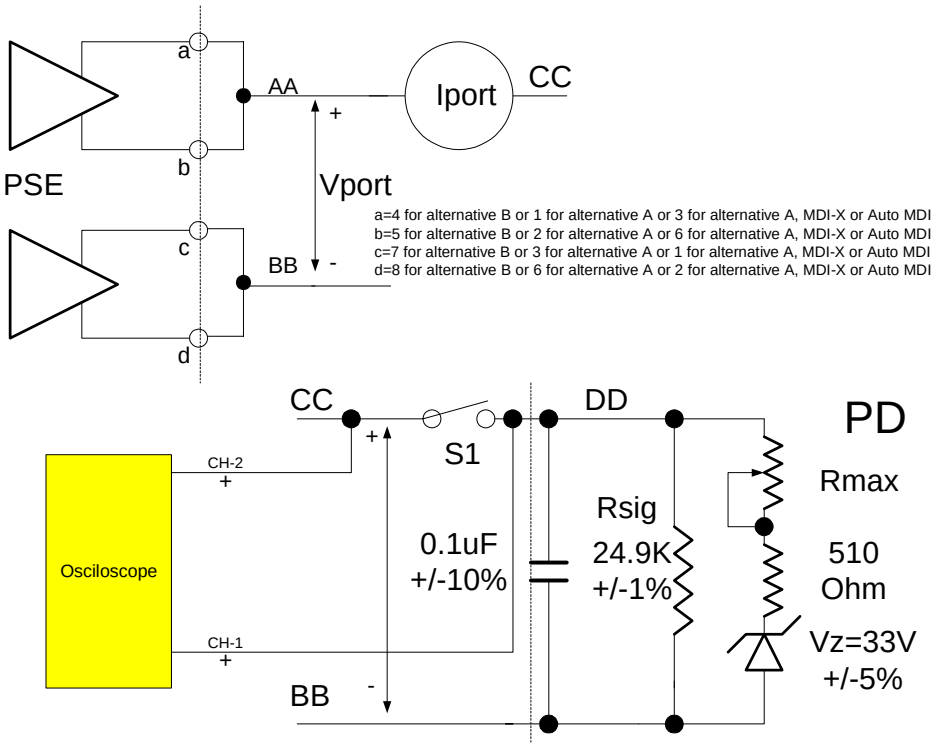

a
b
c
d
PSE
AA
Iport
CC
+
Vport
BB
-
a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI
CC
DD
PD
S1
CH-2
+
Osciloscope
CH-1
+
0.1uF
+/-10%
Rsig
24.9K
+/-1%
Rmax
510
Ohm
Vz=33V
+/-5%
BB
-

Figure 33-17

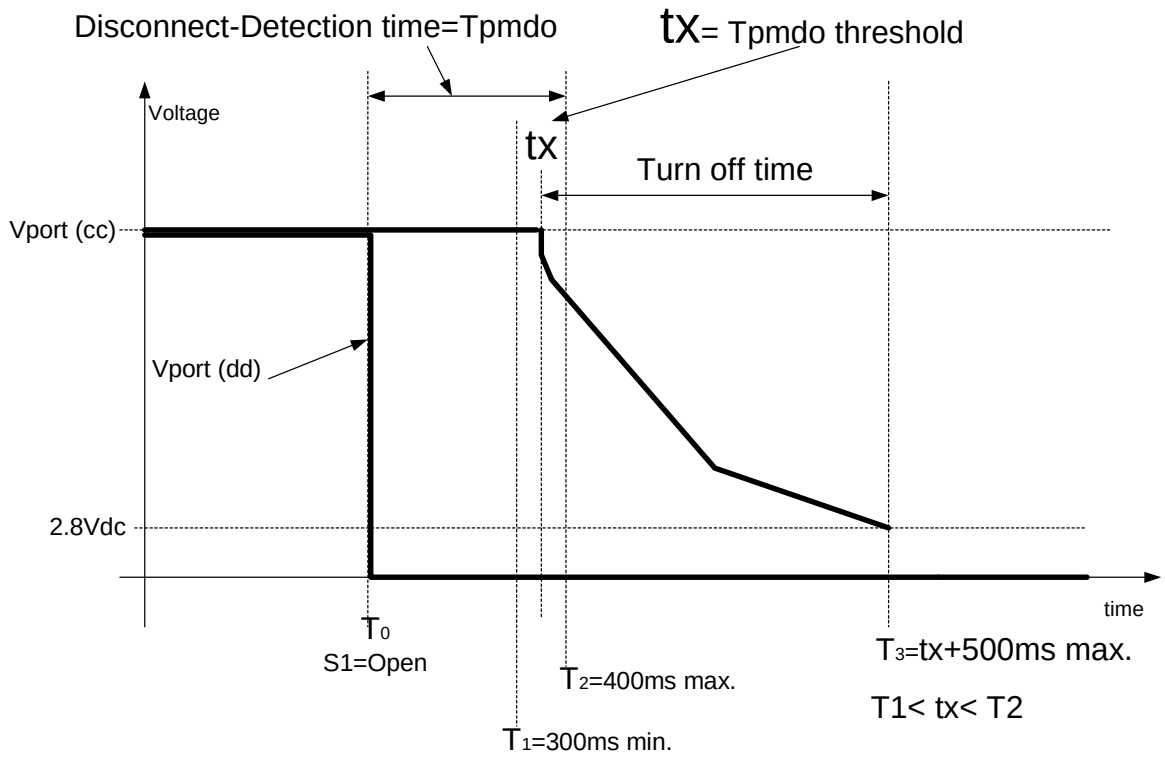


Figure 33-18

Change the following text :

Page 52, line 44: remove the words starting with “by verifying…” to the end of this sentence at line 45.

Page 53, line 16,17: delete “(Power is removed when….5mA)”

Page 63, line 2: delete line 2 “power is removed when …1Vmin”

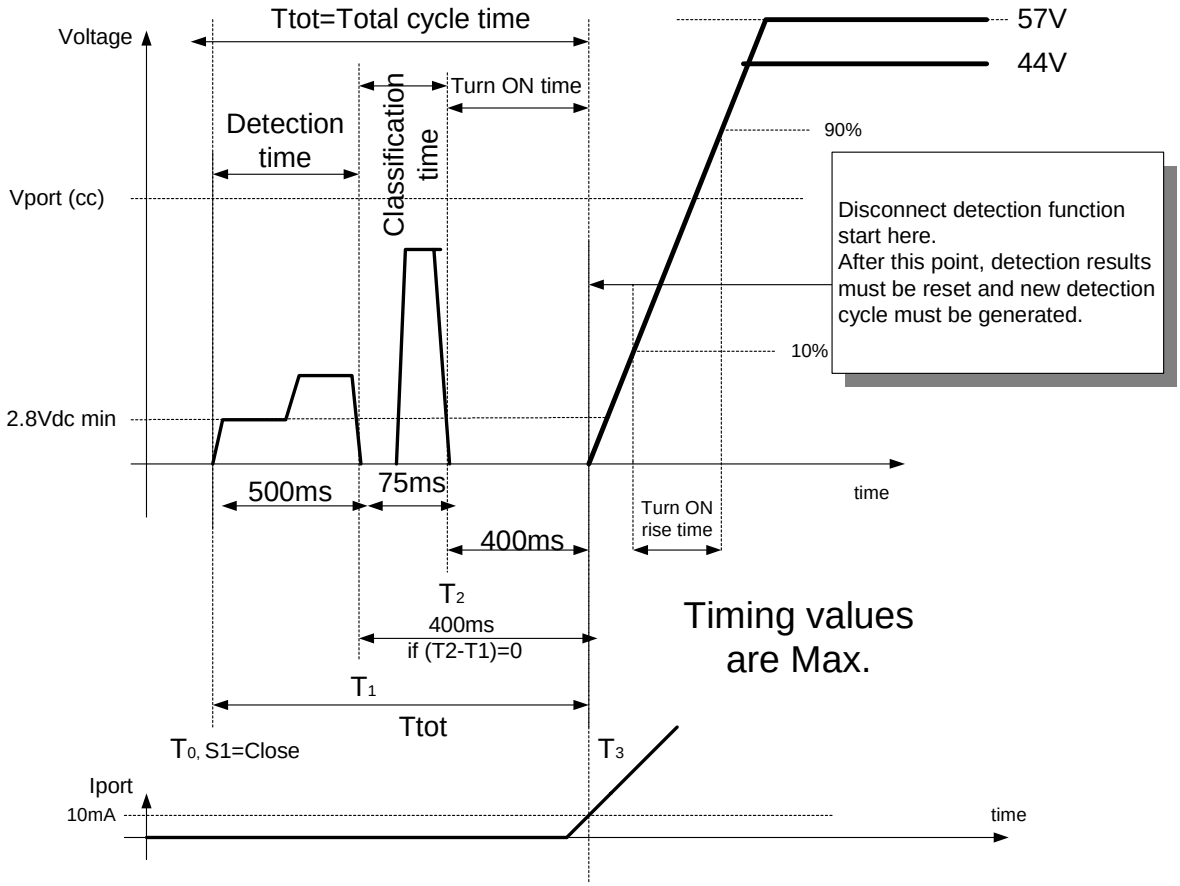
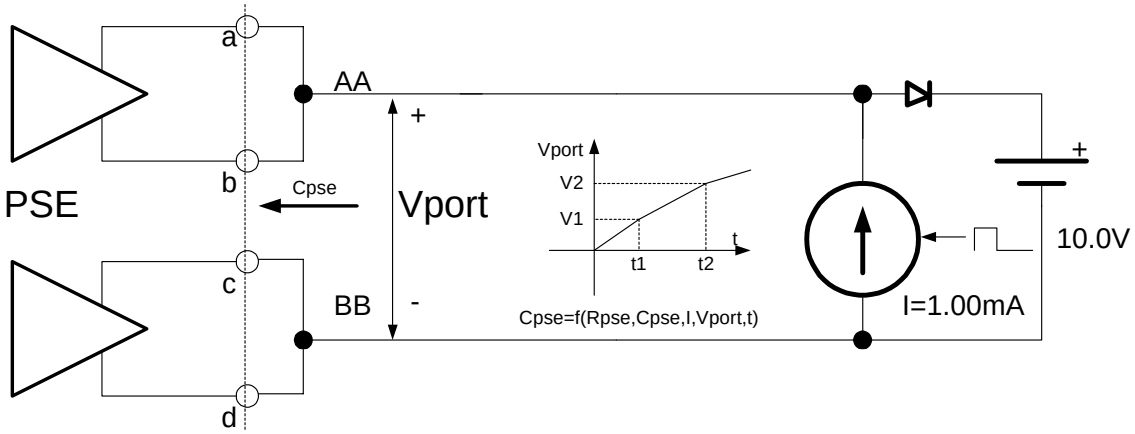

Ttot=Total cycle time
Voltage
57V
44V
Turn ON time
Detection time
Classification time
90%
Vport (cc)
Disconnect detection function start here.
After this point, detection results must be reset and new detection cycle must be generated.
10%
2.8Vdc min
500ms
75ms
time
Turn ON rise time
400ms
T2
400ms
if (T2-T1)=0
Timing values are Max.
T1
Ttot
T0, S1=Close
T3
Iport
10mA
time

Figure 33-19



a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI

Figure 33-21

Replace step 1 in page 60 line 35 with:

1. Set PSE port to OFF mode.
Connect switched current source, I to the PSE port.
The current source voltage shall be clamped to 10V.
Calculate Port capacitance (Cpse) by measuring Rpse (Port resistance) and using it in typical differential equation solution specified in figure 33-5-18.

Delete step 2, page 60 line 39.

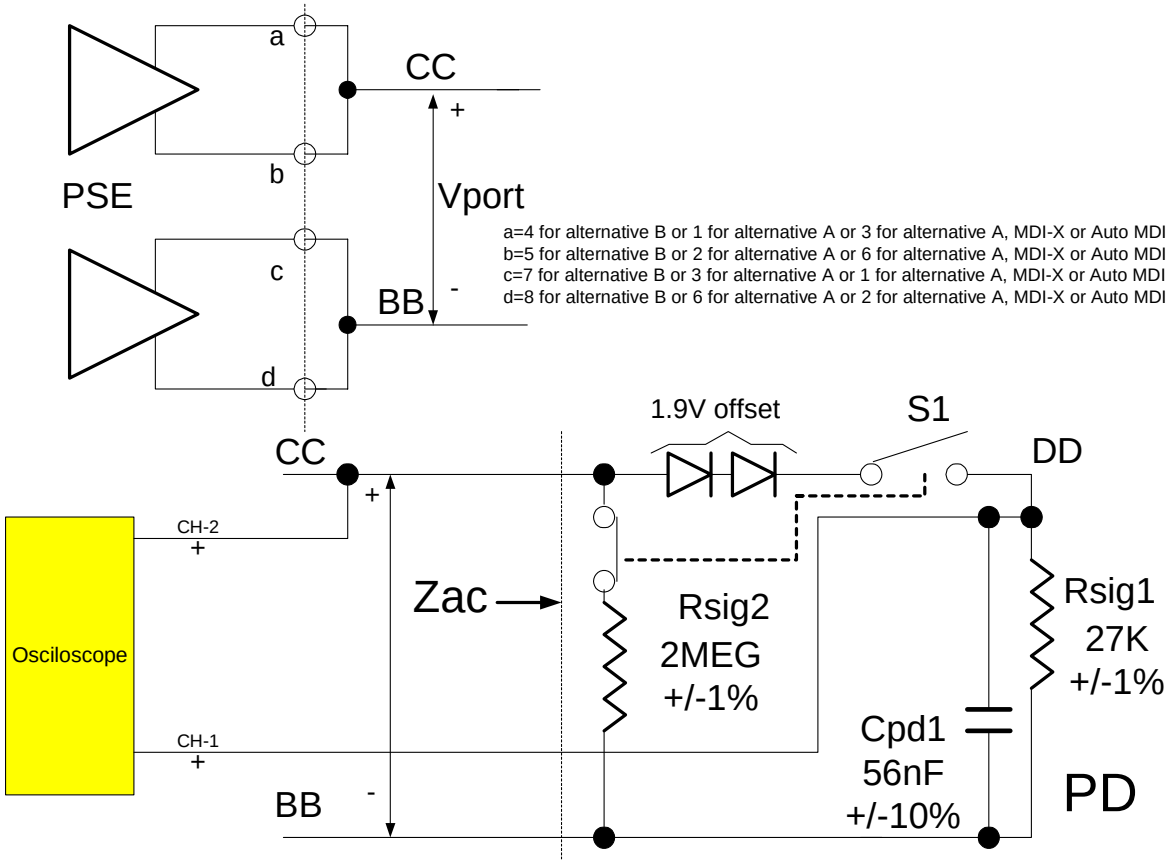


Figure 33-22

Replace step 1 in page 62 line 49 with:

"Set S1=close (Rsig1 connected to the port, Rsig2 not connected to the port).
Measure Vport and verify that $44V \leq Vport \leq 57$ and V_close<0.5Vpp"

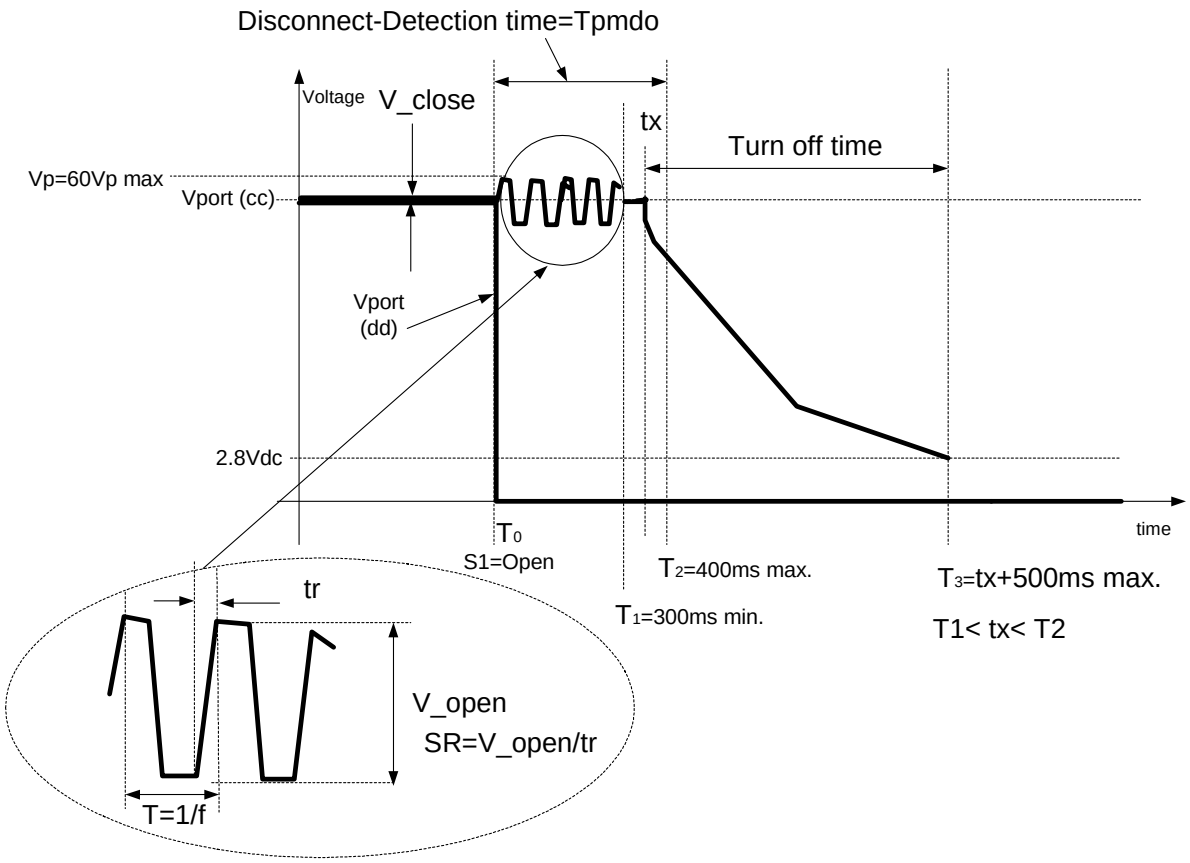


Figure 33-23

Delete line 2 page 63 “(power is removed…1V min)”
Delete line 16,17 page 53 “(power is removed…5mA)”

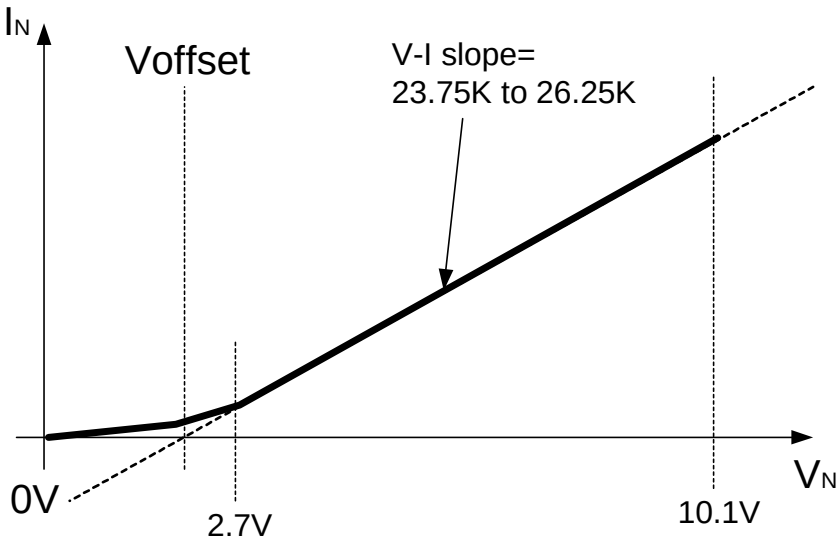


Figure 33-27

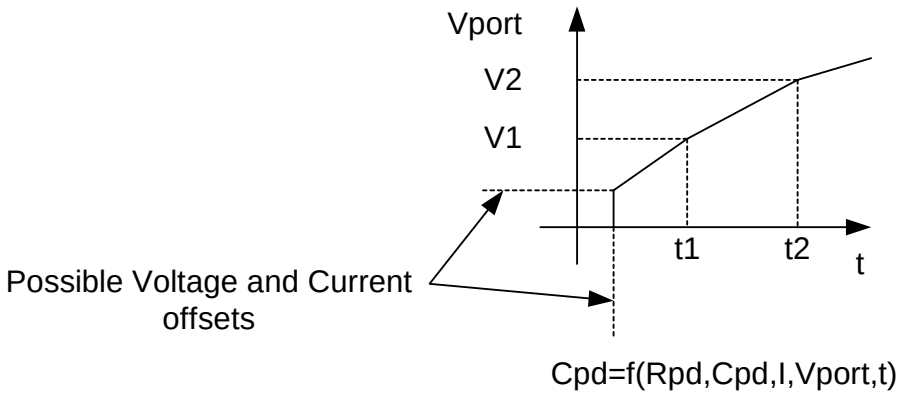
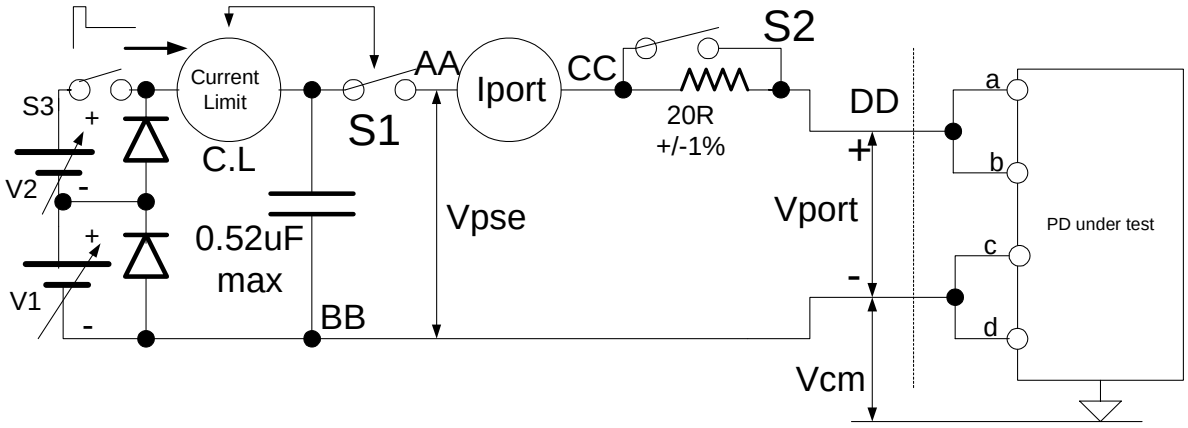


Figure 33-28

Replace step 9 in page 68 line 42 with:

1. Calculate Port capacitance (Cpd) by measuring Rpd (Port resistance) and using it in typical differential equation solution specified in figure 33-28.

Delete step 10, page 68 line 43.



a=4 for alternative B or 1 for alternative A, MDI-X or 3 for alternative A, MDI or Auto MDI-X
b=5 for alternative B or 2 for alternative A, MDI-X or 6 for alternative A, MDI or Auto MDI-X
c=7 for alternative B or 3 for alternative A, MDI-X or 1 for alternative A, MDI or Auto MDI-X
d=8 for alternative B or 6 for alternative A, MDI-X or 2 for alternative A, MDI or Auto MDI-X

Figure 33-29

Add to page 75 line 34: (Refer to comment #53)

“25) Set V1 to 44V,V2=0V, Set S1 to ON. Measure Vport and Vcm noise level at Vport 37V to 57V and at all known PD operating load conditions.“

Finalizing AC disconnect spec

(Comments (T/TR) 398, 337, 358, 69, 64, 38, 66, 67..)

Table 33-6 – PSE port parameters for AC Disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Notes
1	Pulse parameters					
a	Port probing ac voltage	V_open	Vpp	1.9	10% of the average value of Vport. for 42.4V<Vport <60V	Include noise, ripple etc.
			Vp		42.4 for Vport <=42.4	Include noise, ripple etc.
b	AC probing signal frequency	Fp	Hz	5	500	
c	AC probing signal slew rate	SR	V/uS		0.1	
2	Ac source output parameters					
a	Source output current	I_sac	mA		1	
b	PSE port impedance during resistor detection when measured from the link (MDI) to the PSE port.	R_rev	KΩ	70		This requirement already mentioned in figure 33-6 paragraph 33.2.5 and is indicated here to clarify the difference in port impedance compared to Signature detection function
3	PSE port voltage during ac disconnect detection					
a	Port ac voltage when PD is Connected		Vpp			Refer to table 33-5 item 3
b	Port voltage when PD is disconnected	Vport	Vp		60	
c	Disconnect detection time	Tpmdo	ms			Refer to table 33-5 item 7
4	AC power maintenance signature					
a	“Shall not remove power from the port”	Zac1	KΩ		27	Specified at the following conditions: Fp=5Hz, Testing voltage >2.5V See figure TBD1 for reference.
b	“Shall remove power from the port”	Zac2	KΩ	2000		See figure TBD2 for reference.

Add the following figures TBD1 and TB2 after table 33-6.

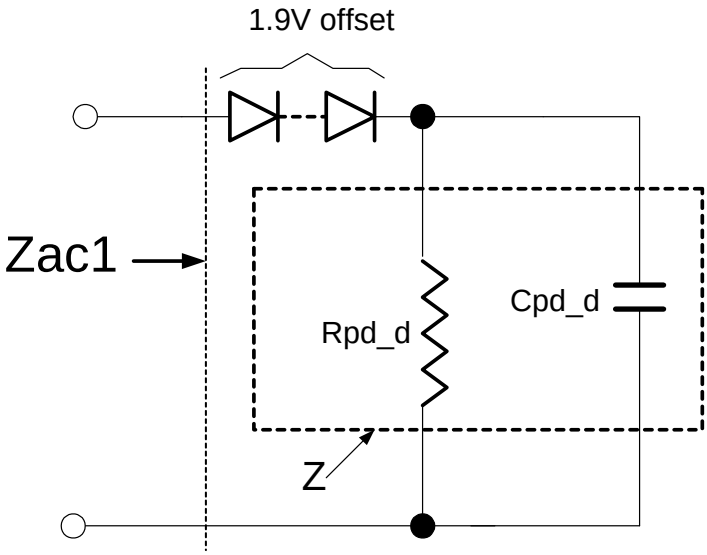


Figure TBD1 – Zac1 definition as indicated in table 33-6.
Rpd_d, Cpd_d specified in table 33-14.

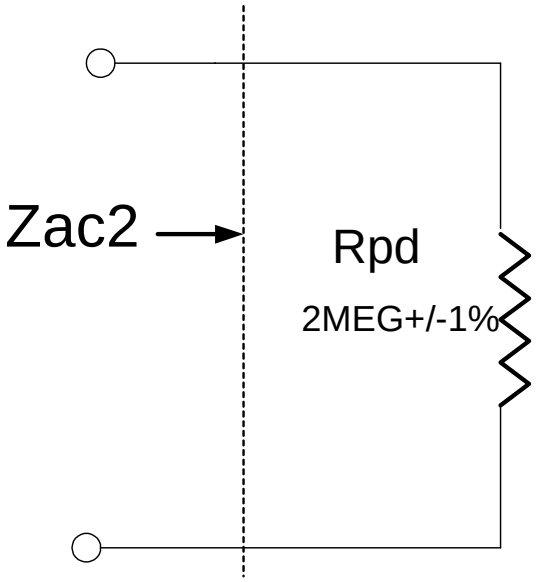


Figure TBD2 – Zac2 definition as indicated in table 33-6

Drawings for my comments regarding 33.2.9 page 46 line 34 and 33.3.5 page 73 line 33

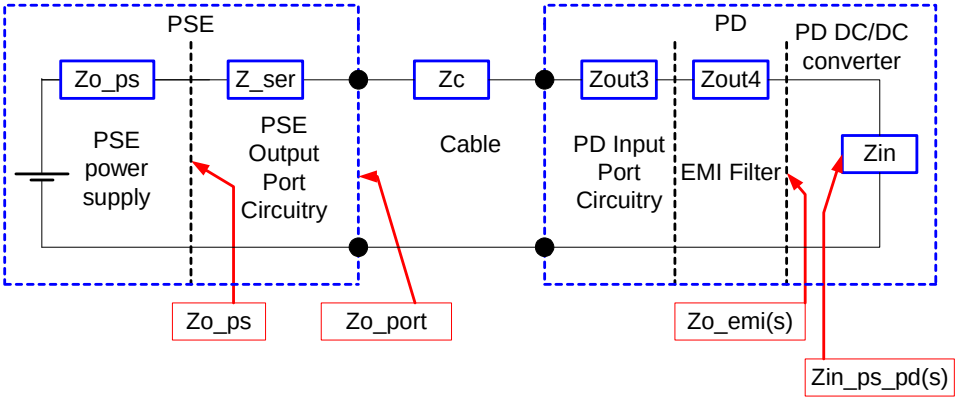


Figure TBD1 for PSE-PD system impedance allocation

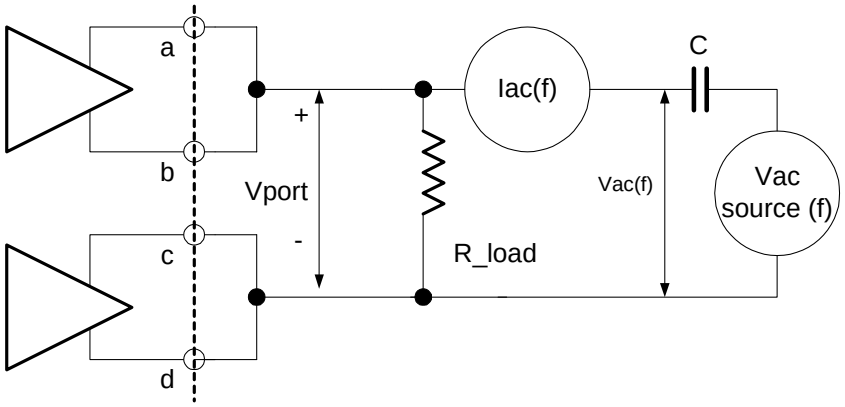


Figure TBD2- PSE-PD stability. Test setup for measuring Zo_ps

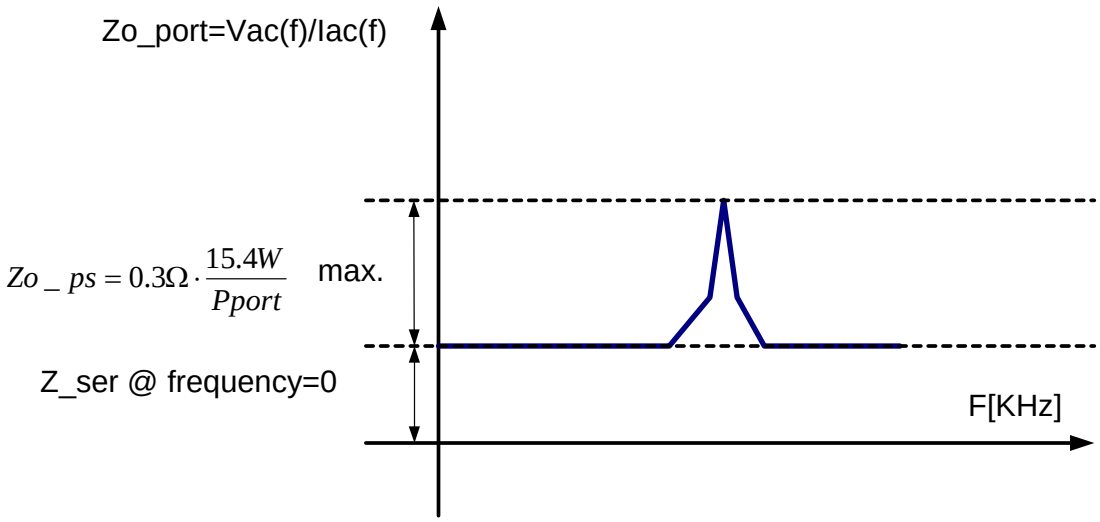


Figure TBD2.1- PSE-PD stability. Test requirements for Zo_ps.

Test Procedure SIG-2, PSE signature detection.

Tested Parameters

1. PSE port impedance during detection– See test procedure PSE-14
2. Parallel diode across the port (Paragraph 33.2.5 figures 33-6 and 33-7)
3. Detection open circuit voltage (Paragraph 33.2.5)
4. Detection short circuit current (Paragraph 33.2.5)
5. Detection minimum/maximum Voltages (Paragraph 33.2.5.1)
6. Two-point detection voltage difference (Paragraph 33.2.5.1)
7. Detection Criteria (Paragraph 33.2.6.1)
8. Rejection Criteria (Paragraph 33.2.6.2)
9. Detection voltages slew rate (Paragraph 33.2.5.1)
10. Detection and Power on the same leads (Paragraph 33.2.6.3)

Test setup

Will be tested as indicated in Figure 33-2-5

Test procedure
Set S1, S2 and S3 to OFF.

Step 1: Parallel diode across the port (Paragraph 33.2.5 figures 33-6 and 33-7)
1. Turn system OFF (No voltages across PSE port). Set V1 to 5.0V. Set S1 and S2 to ON. S3=OFF.
2. Measure Iport. Verify that Iport>3mA.
3. Reverse V1 polarity. Verify that Iport < 40uA
4. Set S2 to OFF.

Step 2: Detection open circuit voltage (Paragraph 33.2.5)

1. Set S1, S2 and S3 to OFF
2. Verify that Vport < 30Vp during the detection phase for 500ms max out of 1sec period.
   Verify that Vport average is <=2.8Vdc when the PSE is not in detection phase.
3. Verify that Voltages slew rate is less than 0.1V/uS
4. It is allowed to have no detection signals or single point detection if the PSE identifies that the Port is open.

Step 3: Detection short circuit current (Paragraph 33.2.5)

See Test Procedure PSE-14.

Step 4:
Detection minimum/maximum Voltages (Paragraph 33.2.5.1)
Two-point detection voltage difference (Paragraph 33.2.5.1)
Two-point detection voltage difference.
Detection Criteria (Paragraph 33.2.6.1)
Rejection Criteria (Paragraph 33.2.6.2)
Detection voltages slew rate (Paragraph 33.2.5.1)
Detection and Power on the same leads (Paragraph 33.2.6.3)

Step 4.1

1. Set Rs=0. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 23.75KΩ. , Adjust Rsig to 19.0K by adjusting Rp.
3. Adjust V_{OFFSET} to 2.0V

Step 4.2

1. Set S1 and S3 to ON. Set S2 to OFF.
2. Measure detection voltages V1 and V2.
   Verify that V1 and V2 are between 2.8V to 10V and |V2-V1|>=1V
3. Verify that 44V min connected to the port for 299ms min.
4. Verify that the slew rate of all the switched voltages is less than 0.1V/us.

Step 4.3

1. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 26.25KΩ. Set Rp=Open. Adjust Rsig to 26.5KΩ by adjusting Rs.
3. Adjust V_{OFFSET} to 2.0V
4. Repeat step 4.2

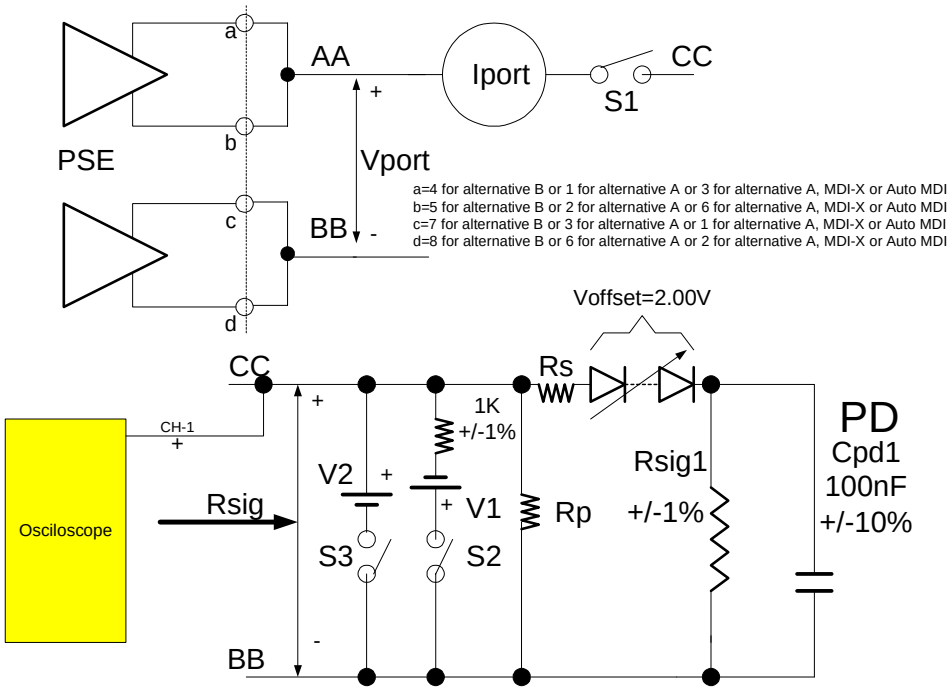
Step 4.3
1. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 15KΩ. Set Rs=0. Adjust Rsig to 14.9KΩ by adjusting Rp.
3. Adjust V_{OFFSET} to 2.0V.
4. Set S1 and S3 to ON. Set S2 to OFF.
5. Verify that power is not applied to the port.

Step 4.4

1. Adjust V_{OFFSET} to 0V.
2. Set Rsig1 to 33.0KΩ. Set Rp=Open. Set Rsig=0.
3. Adjust V_{OFFSET} to 2.0V.
4. Set S1 and S3 to ON. Set S2 to OFF.
5. Verify that power is not applied to the port.

Step 4.5

1. Set Rsig1=24.9KΩ. Set Rp=Open. Set Rsig=0. Set Csig=10.0uF
2. Adjust Voffset for 2.0V.
3. Set S1 and S3 to ON. Set S2 to OFF. Verify that power is not applied to the port.
4. Repeat step 4.4 for Rsig1=open.


a
b
c
d
AA
Iport
CC
S1
+
Vport
-
BB
PSE
a=4 for alternative B or 1 for alternative A or 3 for alternative A, MDI-X or Auto MDI
b=5 for alternative B or 2 for alternative A or 6 for alternative A, MDI-X or Auto MDI
c=7 for alternative B or 3 for alternative A or 1 for alternative A, MDI-X or Auto MDI
d=8 for alternative B or 6 for alternative A or 2 for alternative A, MDI-X or Auto MDI
Voffset=2.00V
CC
Rs
1K
+/-1%
PD
Cpd1
100nF
+/-10%
CH-1
+
Osciloscope
Rsig
V2
V1
Rp
Rsig1
+/-1%
S3
S2
BB