IEEE 802.3af DTE Power via MDI
System Considerations - PD / Detection issues

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Topics for discussion / Analysis

- Detection time vs. system parameters
- PD input signature as function of leakage caused by different sources
- Dynamics between PD power supply and UVLO functions

Detection time vs. system parameters

- PD max. input capacitance = 0.1uF max. Why?
- PD contains switching mode power supply. 100Khz + harmonics up to 30Mhz.
- RJ45 Connector may be away from PD power supply input. Far away =1 to 2cm at 10-30MHZ. (100mV across 1cm=10nH with 1A/100nSec)
- Low impedance cap. Is required to be located as close as possible to the RJ45 pins. It allows low cost high frequency filtering.
- Lab tests results and Power conversion analysis shows that for 15W,100Khz, 36V-72V input voltage range, 0.1uF max, low ESR, low ESL reduce conducted emissions at the switching frequency and its harmonic.
- Low impedance at wide frequency range can be achieved by connection 2,3 capacitors in parallel with 1nf ,8.2nF, 82nF.
- Note: this capacitor is not the only part of EMI filter block located at PDPS input

Detection time vs. system parameters

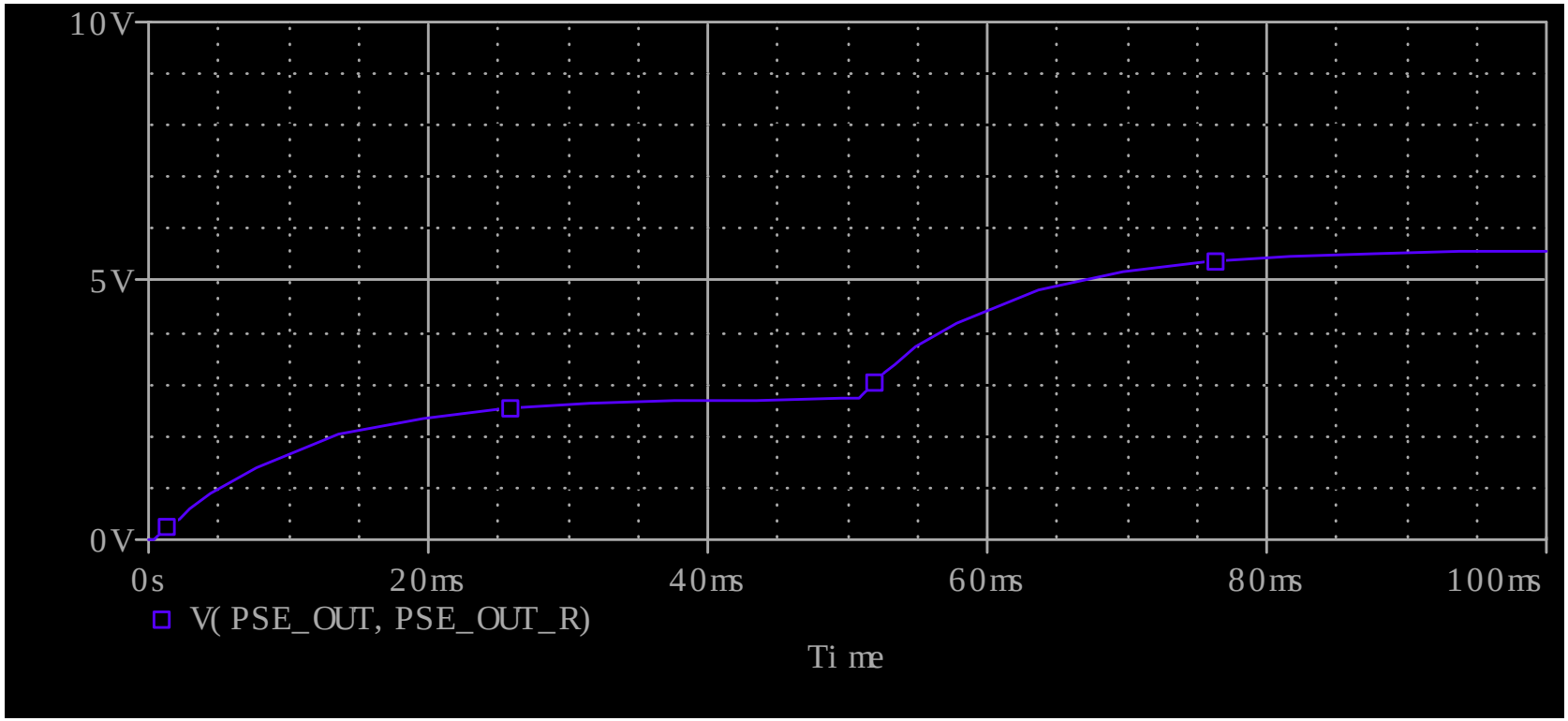
- PSE max. output capacitance - ESD point of view

- 0.47uF output port capacitance reduce ESD voltage to acceptable levels(<100V). (4KV-8KV tests)
- Capacitor can be reduce a little bit by using small inductance <1uH.
- It must be low impedance/low inductance path, otherwise it is not effective.
- High series resistor value during detection may help in some implementations In some not.
- Capacitor must be close to the RJ45 output pins. Other solutions such as relying on output port diode and switch diode can ease the problem, however it strong function of layout and components cost.
- Cost reduction is achieved by utilizing single cap for ESD and EMI reduction.
- ESD: See PowerDsine Sep. 2000 presentation for more details

Detection time vs. system parameters

- PSE max. output capacitance - EMI point of view
- The same rational as the PD EMI treatment, and even worse
  - 12-24 port noising together.
- PSE power supply output cap may located far from the RJ45 output pins and from cost reasons it is not a low impedance path for high frequency with out using additional parallel ceramic or eqv. material capacitor.
- Cost reduction is achieved by utilizing single cap for ESD and EMI reduction.
- Cable pair to pair capacitance=10nF max. ?
- From measurements:
  FTP cable = 6.8nF measured at 32Khz. 10nF max. was chosen.

Probing voltage steady state time



- @ Rsig1=75K, Rsig=25K, Ctotal=0.55uF
- Leakage effects are as reflected by the system model. Not include cable leakage effects

Detection time vs. system parameters

- System parameters
  - Total PSE output port capacitance during detection = 0.55uF
  - Equv. Probing source resistance= 20K max.
  - Two point measurements
  - Wait until 1% of final value is reached => 4.5Rt x Ct
  - Total detection time, Tdet=2x0.55uFx20Kx4.5=99mSec < 200mSec leaving 100% margin for additional signal manipulations
  - Tdet can be further reduced by different implementations of PSE output port, without impairing PSE-PD Inter-Operate

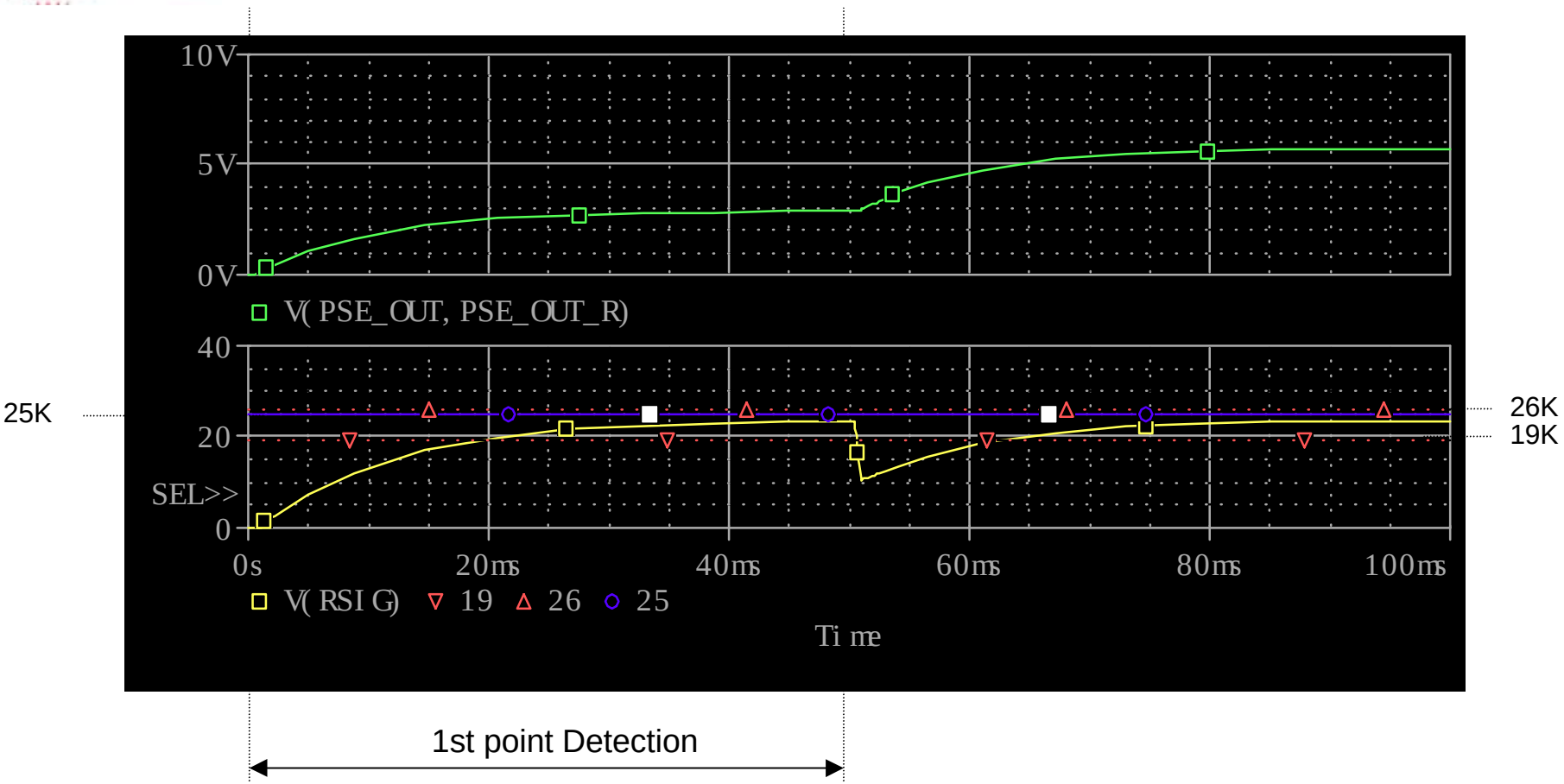
Signature value as function of leakage current

- Leakage Data

- MOSFET Leakage from Data sheet:
  50uA @ 25°C, Vds=Vdsmax and 250uA @ 100°C , Vds=0.8xVdsmax
  Using 10% of Vdsmax will reduce the leakage current by factor of 10 i.e.
  5uA @ 25°C, 25uA @ 100°C.

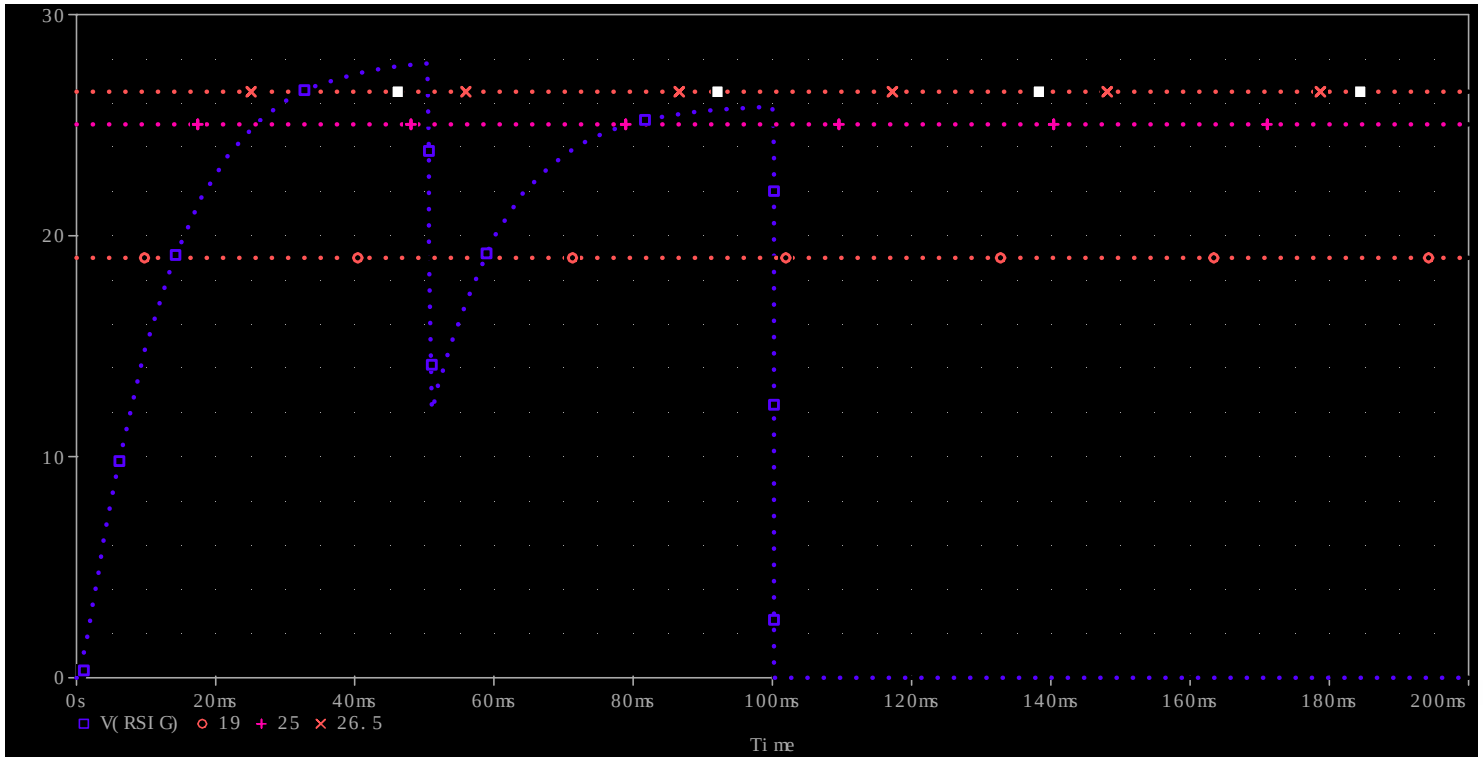
- Lab results where much better than specified in the datasheet.
  Example: for IRF530 (Power Mosfet)
  For 5V< Vds< 100V @ 25 °C , 0.4uA max and 3uA max. @ 50 °C.
- Same results for wide range of PMOS devices.
- 10 times lower results in diodes when VR_opr/VR_nominal<0.1
- Conclusion: less than 5uA Leakage current is expected from PD side.
- Less than 25uA in PSE side, not include cable effects
- Waiting for Lab results to confirm the above.

Signature value as function of leakage current



- Upper plot: Voltage across PSE port during detection
- Lower plot: Signature measurements, Y axis values are in KΩ (not volts) , without PD diode offset
- Not include cable leakage

Signature value as function of leakage current and diode offset



- Signature measurements, Y axis values are in KΩ (not volts) , with 1 diode offset
- Not include cable leakage
- With the the slope measurement, final result will be with in the valid range

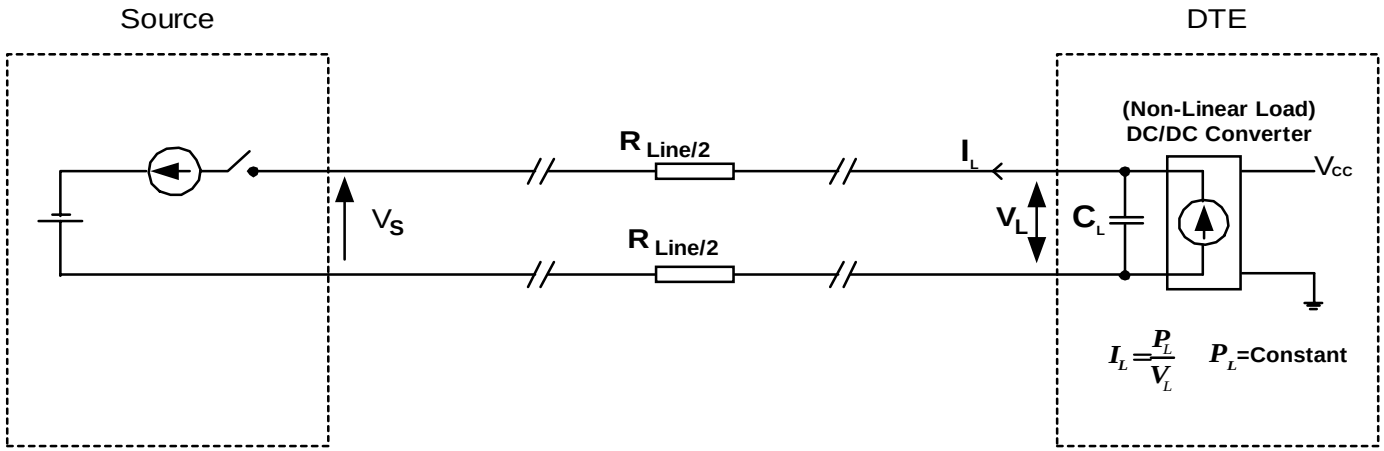
Signature value as function of leakage current

- Summary
- Current through signature resistor 120uA-240uA (for 12V,24V,75K,25K system)
- Leakage effects expected to be less than 35uA (Need data on cable leakage)
- Leakage is function of probing voltage, therefore, reducing probing voltage will reduce leakage effects.
- Signature range and tolerance should be defined within the probing voltage (2.8V to 10V as per Rick's analysis?)
- No requirements on signature value above 10V (simplifies PD input circuits)
- Signature value can be adjusted in PD to compensate for leakage and dc offset effects
- Calibration techniques will reduce the effect of leakage in PSE
- PD power supply and related circuitry must be kept OFF bellow 10V
- Wee still need lab results to support the above conclusions.

Dynamics between PD power supply and UVLO functions

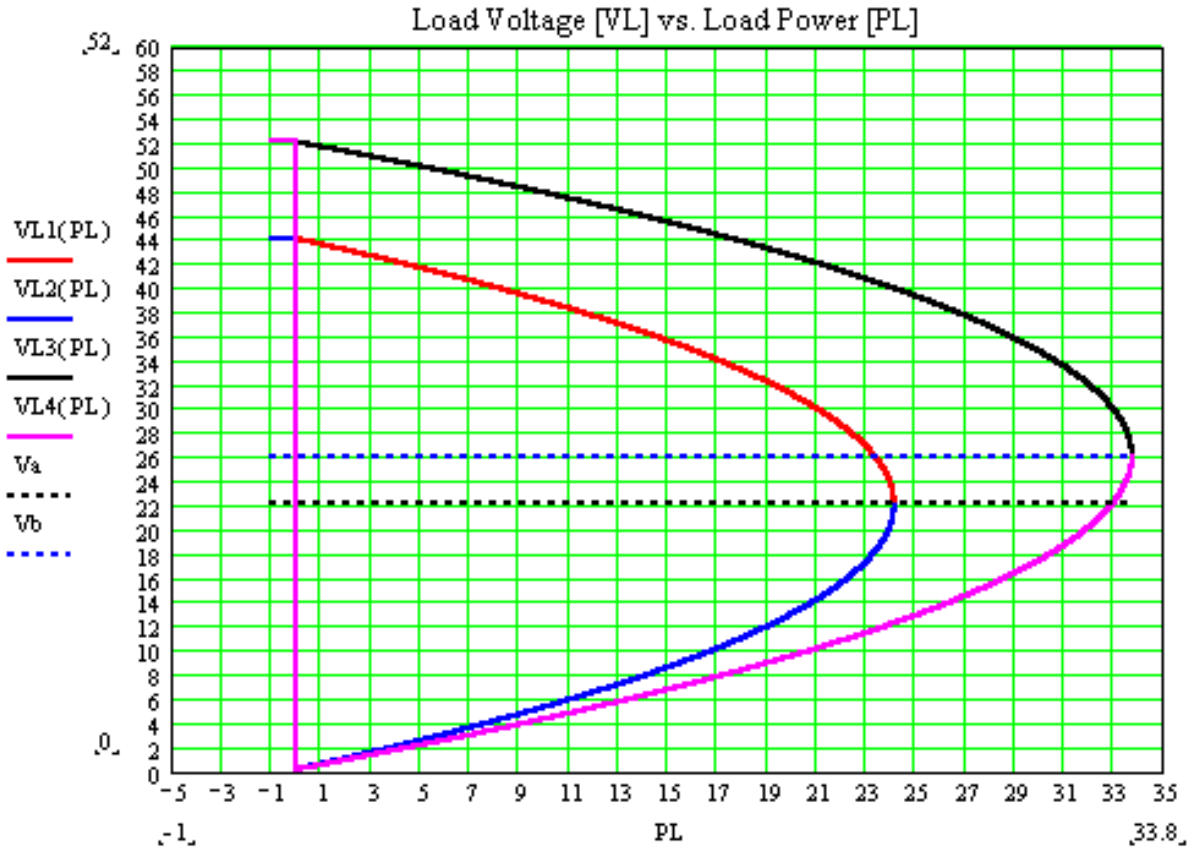
- PD switching power supply exhibits non linear load with “Negative Resistance”
- Input current is reversed proportional to its input voltage Iin=Pin/Vin, in=Constant
- Pd power supply input voltage can lock on two stable solutions.
- The lower input voltage solution exhibits overload condition, preventing reliable startup.
- If PD power supply will not contain UVLO function, startup problems expected.

Dynamics between PD power supply and UVLO functions



$$V_L1, V_L2 = \frac{\left(V_S \pm \left(V_S{}^2 - 4 \times P_L \times R_{Line}\right)^{0.5}\right)}{2}$$

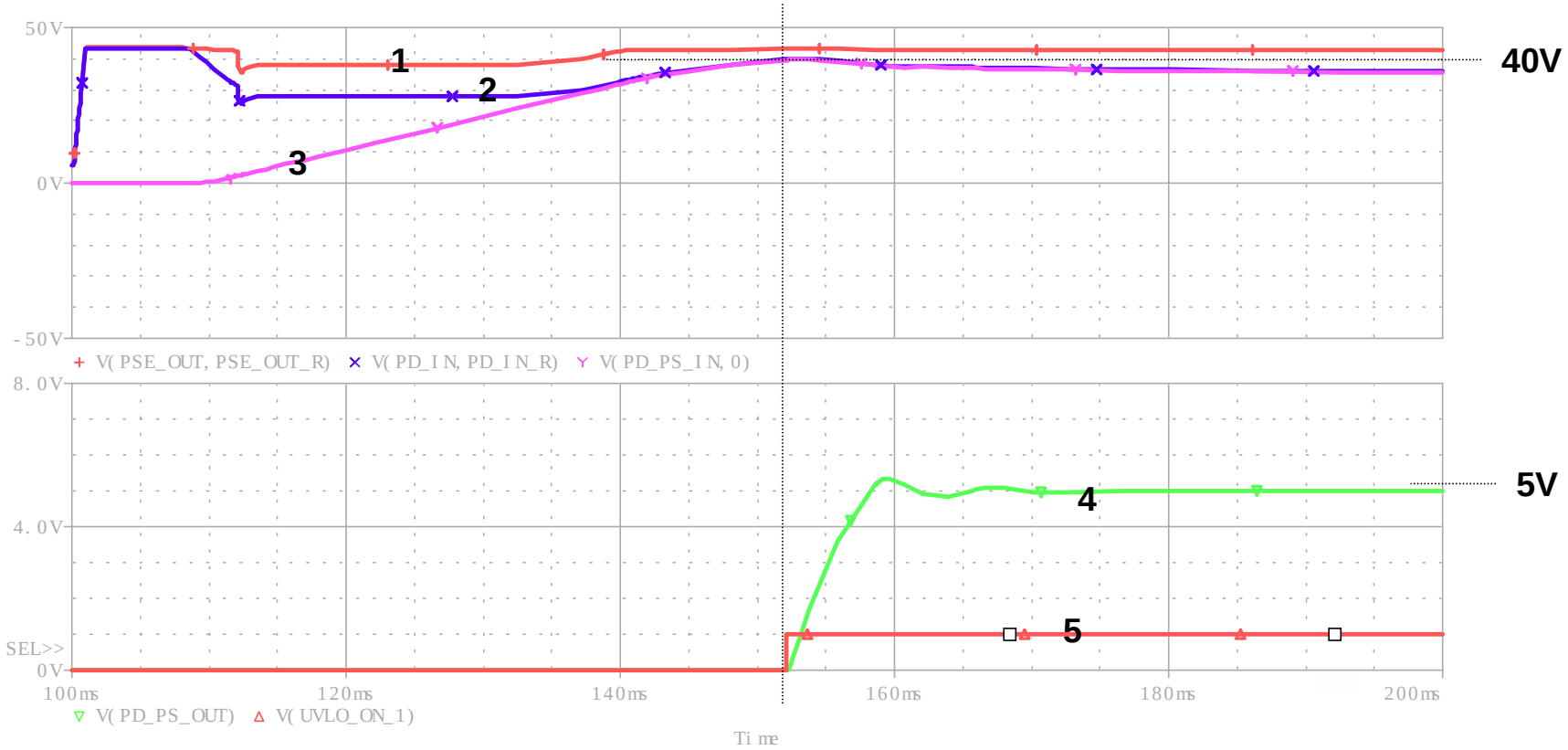
Dynamics between PD power supply and UVLO functions



$$V_L1 = V_L2 = V_L = \frac{Vs}{2}$$

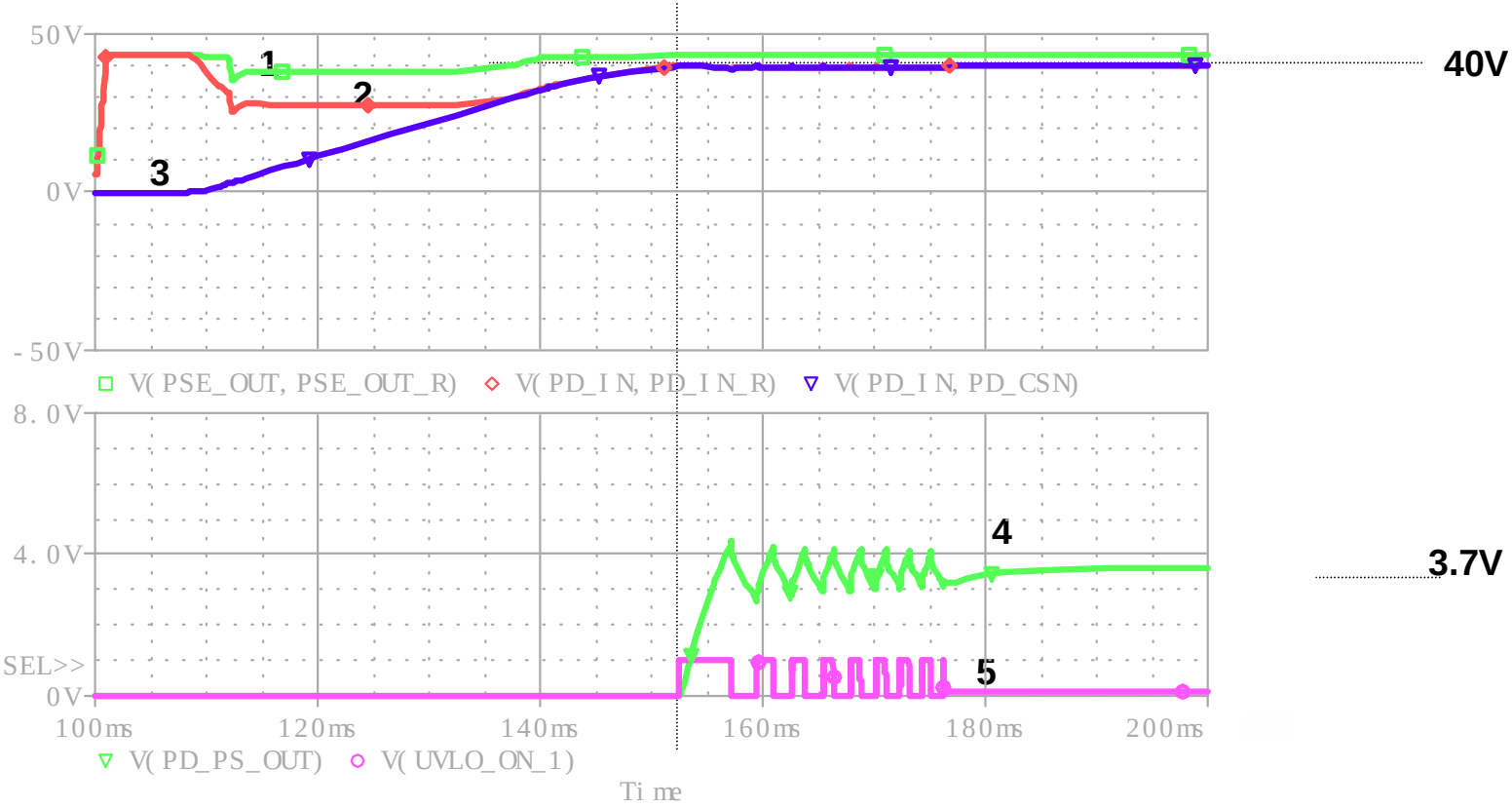
- For complete analysis see PowerDsine May, 2000 presentation.

Simulation of all system functions with UVLO



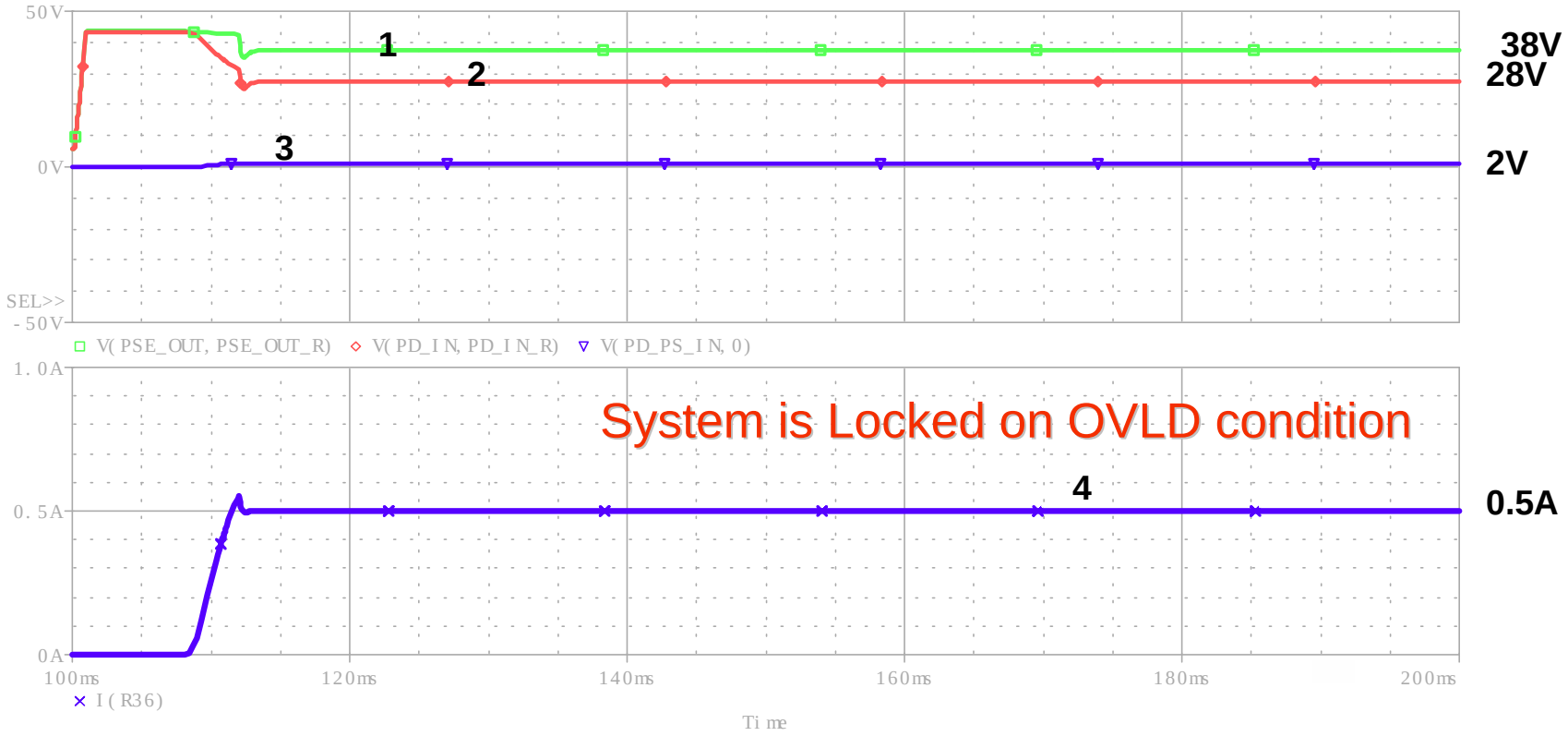
- Trace 1: PSE output voltage
- Trace 2: PD input voltage (Effects: cable drop voltage, Isolating switch turns on)
- Trace 3: PD power supply input voltage.(Effects: Big cap ramping voltage, UVLO function turn on)
- Trace 4: PD power supply output voltage.(Effects: Real dynamics,Overshoots,stability,close loop response)
- Trace 5: UVLO function (Turn on =40V, Turn off=30V,PSE C.L.=0.5A,PD C.L=NC,Pout=10W)

Simulation of all system functions: UVLO set to Turn on≈Turn Off



- Trace 1: PSE output voltage
- Trace 2: PD input voltage (Effects: cable drop voltage, Isolating switch turns on)
- Trace 3: PD power supply input voltage. (Effects: Big cap ramping voltage, UVLO function turn on)
- Trace 4: PD power supply output voltage (Effects: Startup problems, Oscilations, Overshoots, stability)
- Trace 5: UVLO function (Turn ON=40V, Turn Off=38.7V)

Simulation of all system functions - W/O UVLO function



- Trace 1: PSE output voltage
- Trace 2: PD input voltage (Effects: cable drop voltage, Isolating switch turns on)
- Trace 3: PD power supply input voltage. (Effects: Voltage drops to 2V due to entering OVLD condition)
- Trace 4: PD power supply input current (Effects: Startup problems, locked on Over-Load condition)

UVLO - Summary

- PD power supply needs UVLO function (For non-linear load only)
- UVLO should be design with different Turn ON and Turn Off values.
- Turn ON=40V-44V (Must turn on at 44V)
- Turn Off >57V/2=28.5V, Turn OFF=30V-34V (with sufficient margins)
- Keeping Turn on voltage > Turn Off voltage allow reducing PD power supply input cap, reducing PD cost.
- Isolating Switch turn off voltage threshold may be combined with UVLO turn Off voltage. (Depend on implementation)