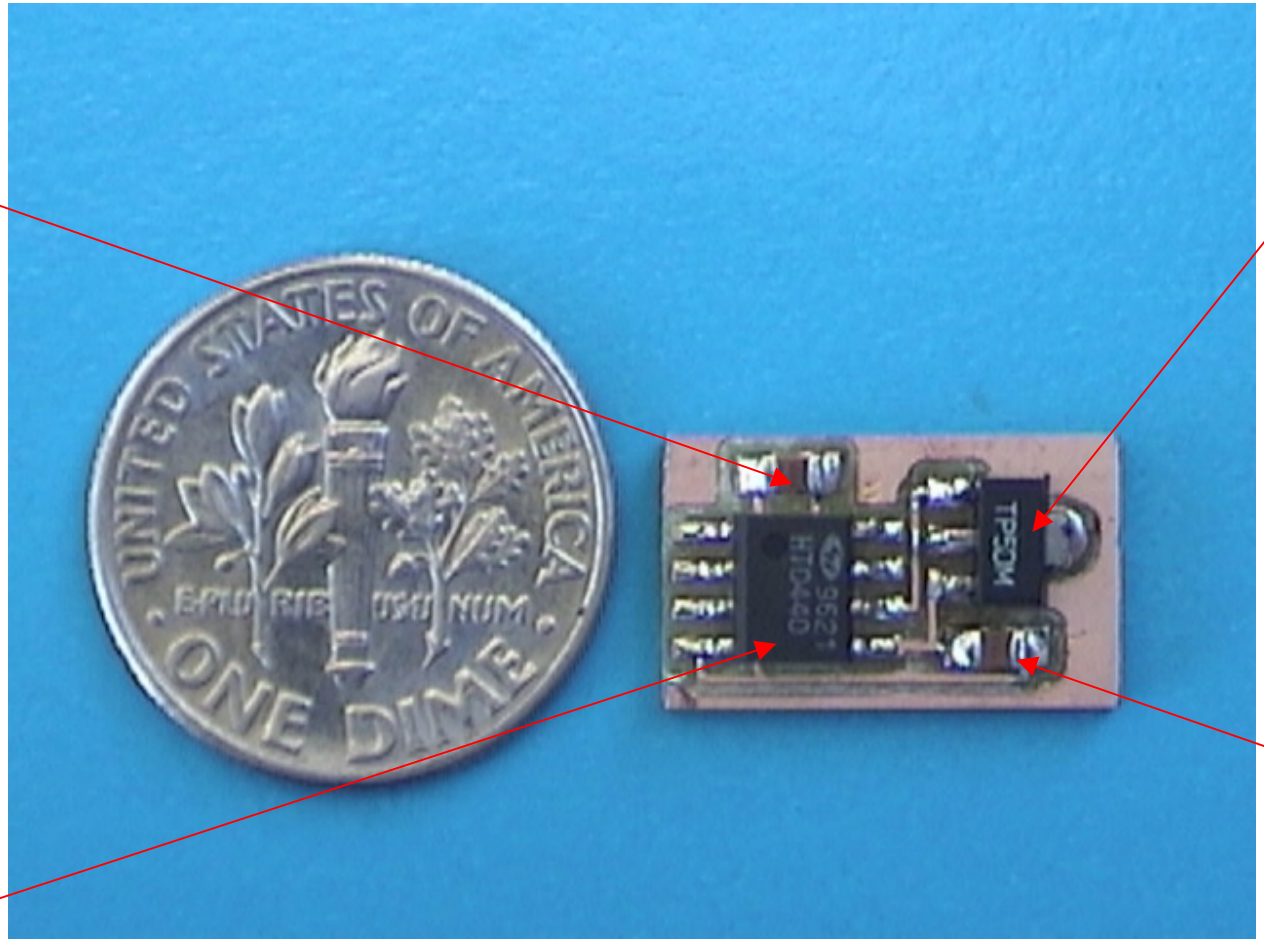
The IEEE802.3 PSE Controller and All Externals !



Flip Chip, uBGA & Other Package Solutions Available

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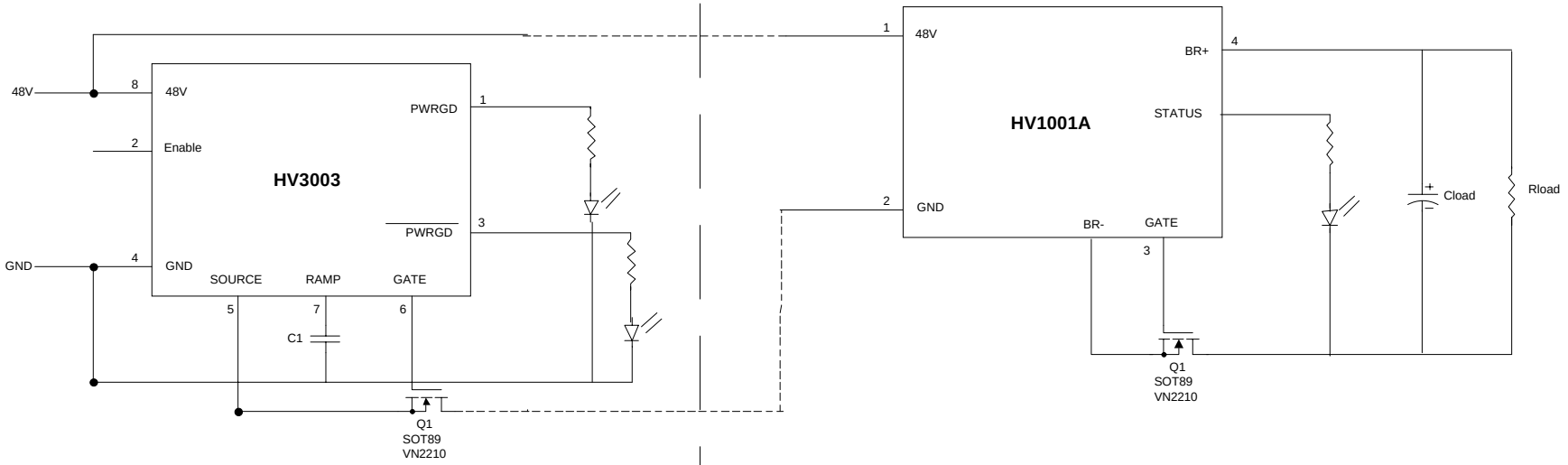
An Integrated Solution

IEEE 802.3 PSE Controller
(Port)

IEEE802.3 SIGNATURE
(IP Phone or Peripheral)



SO-8 + SOT89

SOT23-6

- Two External Components
- 2 Optional Components
- Enable & Optional LEDs
- Includes Signature Side A

- One External Component
- One Optional LED
- Includes Polarity Guard
- Includes Signature Side B

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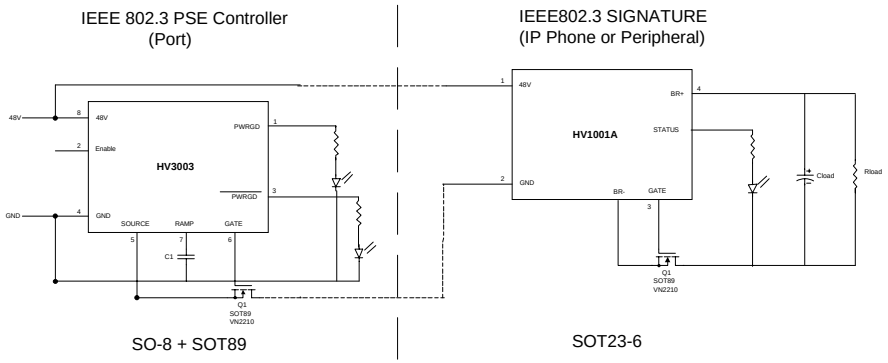

Considerations:

- Pass Elements Necessary on HV3003 for Power Management & Hotswap Functions

- Pass Element Necessary on HV1001A to Block Load Impedance During Signature

- UVLO/OVLO Necessary on Primary to Protect Against Input Bounce & Poor Power Conditions

- A 90V Process Required to Protect Against Overvoltages due to Lumped Network Impedances

- Current Monitoring is Implemented only in the HV3003 and not the HV1001A to Save Cost

- Tight Tolerance SiCr Resistor Required for Signature

- State Machine Polling Over a Multitude of Operating Points is Needed to Protect Against False Signature

- Long Polling Time & POR Protects Against RJ-45 Bounce

- Solution Should Have Low Quiescent Current Draw

- Bounces will Reset Polling Mechanism; if somehow connection occurs pulses are 350mA & di/dt limited and 10mA<I<700mA Circuit Breaker Will Likely Shutdown

- Ckt. Brkr. Retry Delay 100's of ms; Longer Than Bounces

- HV1001A Pass Element Must Be Off for Signature to Work; Causing Further Startup Delay After HV3003 Shutdown

- HV1001A Includes Polarity Guard

- Circuit Breaker has 10mA < I < 700mA Limits

- Persistence of 3.5us or longer Guards Against Transients

- PWRGD Delay + Extra Delay Holds off 10mA and Allows Logic Enable of the Load (Optional)

- An Enable & Two Status Outputs on HV3003 and Status on the HV1001A Allow Monitoring & Management

- Solution must be small Enough to Fit in Ports

- Solution must be Reliable (ESD) & Control EMI/RFI/Noise

- Entire System must be <$2 with Eventual <$1 Target

- Mechanical Connections “Bounce”
- High Voltage + Capacitive Load = Large Inrush
- Inrush/Ringing with Large di/dt’s Can Cause EMI, RFI & Conductive Glitches/Noise, Component & Port Damage
- Signature Polling Guards Against Network Bounce
- Undervoltage & Overvoltage + POR for Primary Bounce
- Soft Start Controls Inrush - Minimizes Transients & EMI
- Circuit Breaker Protects Against Short Circuits
- Circuit Breaker has Persistence Req. & Restart Delay
- True Current Loop Control & Supertex True HV Process

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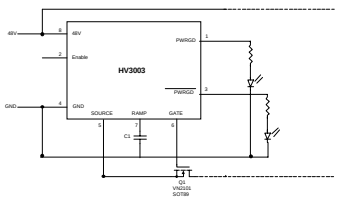
IEEE 802.3 PSE Controller
(Port)

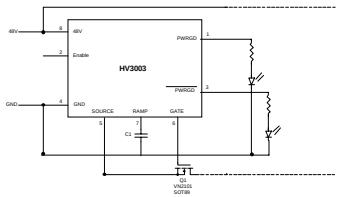


SO-8 + SOT89

HV3003

- Low Cost: HV3003, HV1001A, All Externals < $2
- Intended for Primary or Mid-Span Location
- Lumped Inductance: Overvoltage Protection, 10V to 90V
- Signature on Board Incl: SiCr Resistor + Diodes
- SiCr Resistor has Low Temperature Variation
- Timing Scalable with External Ceramic Capacitor
- Complete Hot Swap Functionality Integral To Design
- EMI, RFI, Conducted Noise Friendly
- 3kV Integral ESD Protection (up to 5kV Possible)
- Enable Logic Input & Two LED Regulated Outputs
- <1mA Active Current Draw, <400uA in Sleep Mode
- 450mA Startup Current Limit

IEEE 802.3 PSE Controller
(Port)

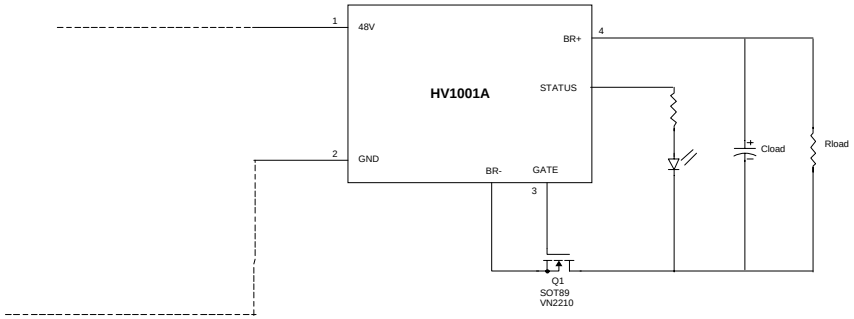


SO-8 + SOT89

HV3003

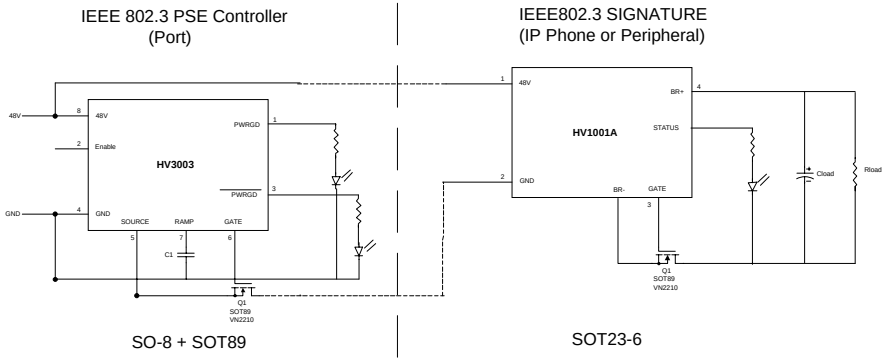
- Under and Overvoltage Lockout on Primary Side with Hys.
- Varies Current Sources to an Array of Signature Points
- Power On Reset Pulse
- 10mA Circuit Breaker Holdoff Until PWRGD Goes High + Delay
- Slow Current Turn on over >100us
- Internal Voltage Regulator for Gate & Status Outputs
- 10mA Minimum & 700mA Max. Circuit Breaker Current (Required 3.5us Persistence - can be extended)
- Circuit Breaker Retry After 100's of milliseconds
- Tiny SO-8 Footprint + SOT89 FET Saves Space
- Based on Advanced High Voltage Mixed Signal Process utilizing Supertex's Twenty Four Years of HV Experience

IEEE802.3 SIGNATURE
(IP Phone or Peripheral)



SOT23-6

- Intended to be Mounted in Remote IP Phone or Peripheral
- Impedance Signature on Board (SiCr + 2 Diodes of Bridge)
- Polarity Guard (Diode Bridge)
- Output Turn on Is Delayed w.r.t Input
- 3kV Integral ESD Protection (up to 5kV Possible)
- HV Comparator Sets Status Once Voltage Across FET < Threshold and Input Voltage > UVLO
- Internal Voltage Regulator for Gate & Status Output
- uPower Active Component Draw
- Pass Element Ensures Impedance Network Does Not See Load



Cases:

- **RJ-45 Intact But Input Voltage on Primary Bounces**
- **Primary Power is Active And RJ-45 Equipment Bounces**
- **Removal and Re-connection of IEEE802.3 Equipment**
- **Remove and Re-connection of non-IEEE802.3 Equipment**
- **Mid-Span Insertion**

Requirements:

- **Provide >40V To IEEE802.3 Device while not Causing Damage to Existing Equipment Using RJ-45**
- **Allowing Mid-span Insertion to Upgrade Existing Networks**
- **To Find a Discovery Mechanism Which Will Interoperate with Existing Equipment**
- **To Meet ESD, EMI, RFI & Conducted Noise/Glitch Requirements**

Example Startup Sequence (Begin with HV3003):

i) Bounce on Primary is Overcome Through UVLO/OVLO

ii) After UVLO/OVLO POR is Followed By Signature POLL

iii) Signature Polls for a number of milliseconds

iv) If multiple Signature Points OK Then Continue

v) If match incorrectly passed, then current will still have to draw between 10mA and 700mA or Ckt. Bkr. Will trip and Reset will Occur

vi) Bounce on RJ-45 Connector will Reset Polling Mechanism. Signature cannot match until pass element completely shutoff - added RJ-45 Bounce Protection.

vii) If Bounce does occur, pulses will have soft di/dt's and be limited to 450mA by the HV3003.

viii) Polarity Bridge Ensures RJ-45 Connector Polarity

ix) Begin Slow Turn on of Pass Element on HV3003

x) Voltage on Gate of HV1001A Pass Element is a fraction of Input Voltage.

xi) Current is Limited to 450mA by HV3003 until Current Drops (350mA IEEE802.3 Imax for load), then FET latches to Reduce Rdson- Contrast Comparator on HV3003?

xii) HV1001A Pass Element Rises to Reg. Voltage

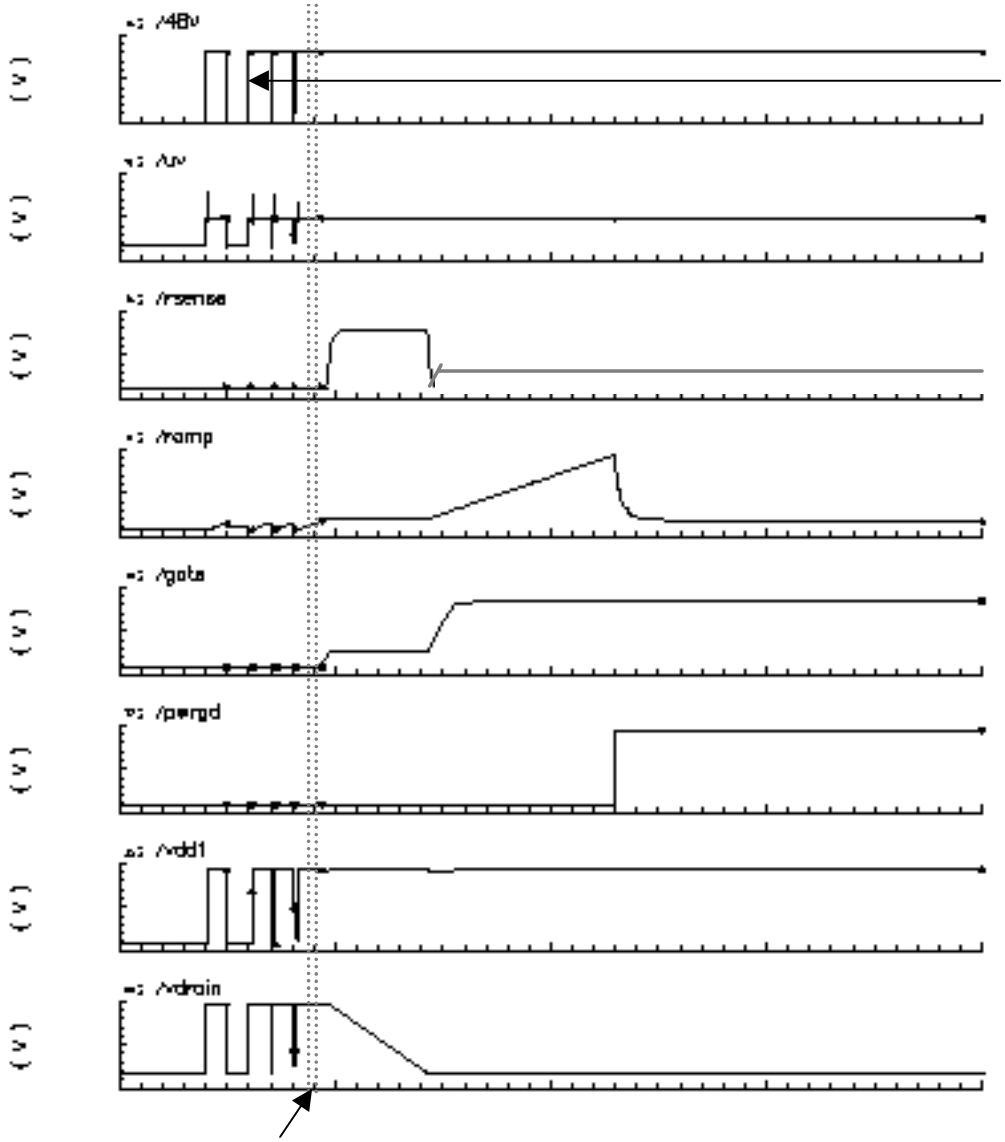
xiii) PWRGD Delay, then HV3003 Goes into Sleep Mode

xiv) Imin & Imax Circuit Breakers are Enabled

xv) IC Monitors Current and Primary Voltage

xvi) If Any Faults Persist for 3.5us (can be adjusted) then Auto-retry delay begins followed by a complete Reset.

Waveforms



>40V Mechanical Bounce

UVLO Pin

Voltage on Sense Resistor

Voltage on Timing Cap

FET Gate Voltage

PWRGD Logic

Internal Regulator Voltage

Voltage Across FET

Signature Polling / POR

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Process Roadmap

Technology	1999	2000	2001	2002	2003	Notes
Low Voltage CMOS	0.8µ – 5.0µ	0. 6µ	0.6µ	0.45µ	0.45µ	N-Well, P-Well, Twin Well
Med Voltage CMOS	2.0µ	2.0µ	1.2µ	1.2µ	1.2µ	10V – 12V
High Voltage CMOS	3.0µ – 5.0µ	2.0µ	1.2µ	1.2µ	1.2µ	2.0µ– 200V, 1.2µ– 100V
BiCMOS	3.0µ – 1.2µ	1.2µ	0.8µ	0.8µ	0.8µ	Both HV (up to 450V) & LV versions
CCD	3.0µ– 1.2µ	1.2µ	0.8µ	0.8µ	0.6µ	Large die capability
Dielectric Isolation	3.0µ	2.0µ	2.0µ	1.2µ	1.2µ	200V

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Discrete Technologies

- **Enhancement Mode DMOS**
  - N-channel 15v to 600v
  - P-channel 20v to 500v
  - Low Thresholds (as low as 1V)
- **Depletion Mode DMOS**
  - N-channel 240 to 500v
- **Lateral DMOS**
  - N-channel 16.5v to 500v
- **Small SO and SOT packages**
- **Available in die or wafer form**

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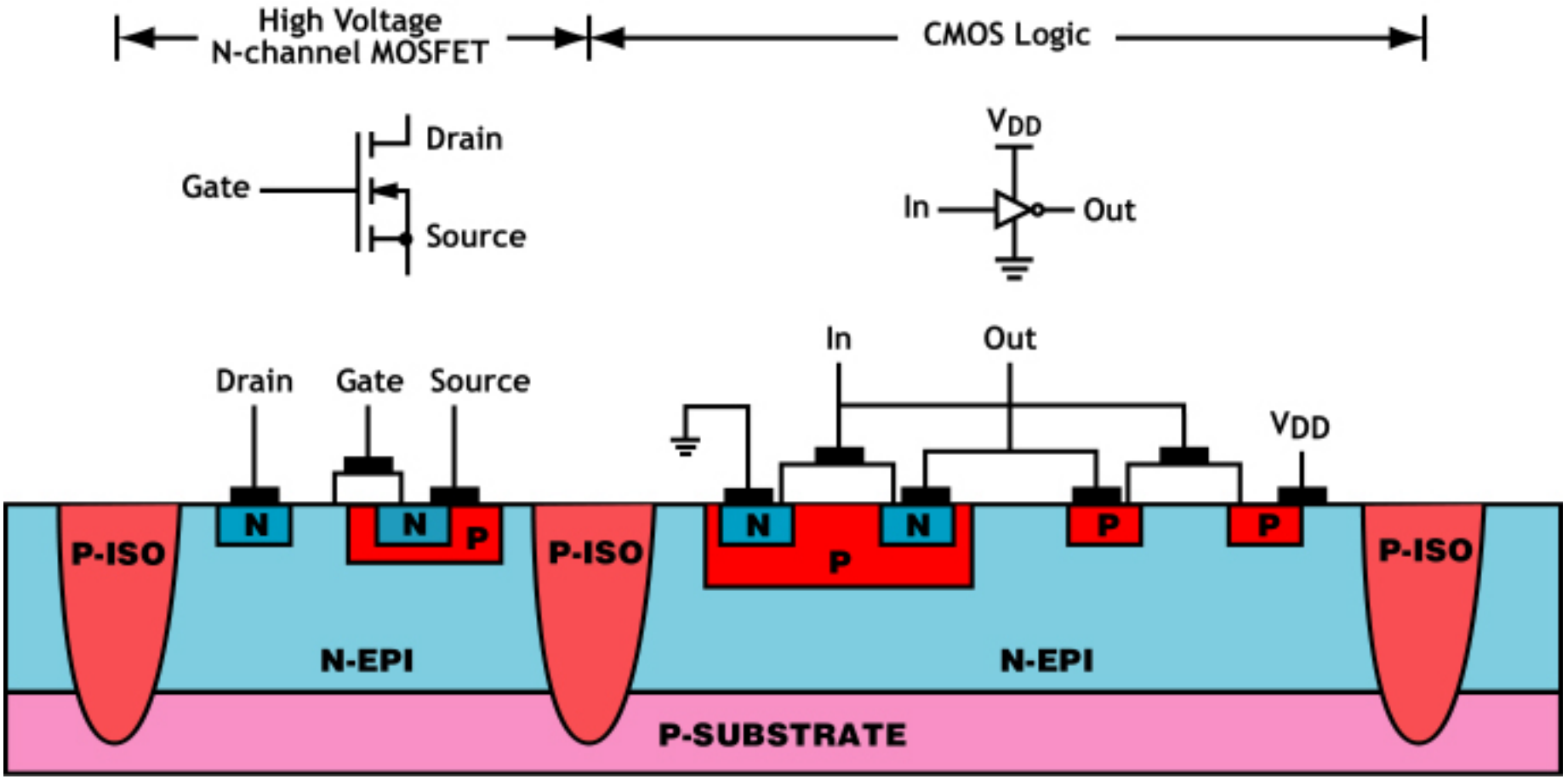
Smart Power >30 Processes

- **BiCMOS**
  - LDMOS to 450V & Depletion Devices Available
  - Integrated 120V Bipolar
  - Variety of Capacitors & Resistors
  - Zeners, Active Diodes, Zap Structures, etc.
- **SiCr Resistors**
  - Low Temperature Variation & Inside Package
- **Packaging & Trimming**
  - A Variety of Packing & Trimming Possibilities
- **Small SO and SOT packages**
- **Available in die or wafer form / Fully Packaged**

Some Low Voltage Companies Think They Can Become HV Overnight - But They're Years Behind !
(It's Not That Easy - Many Have Stumbled Already at 48V !)



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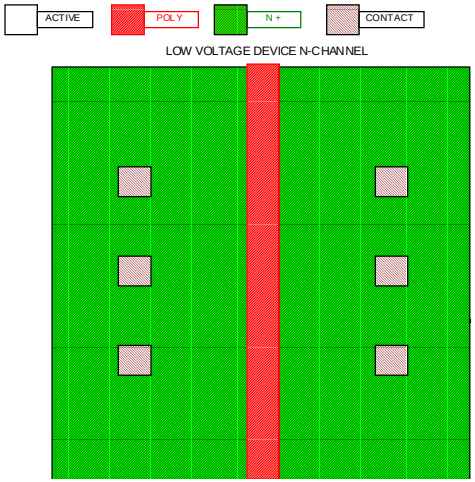
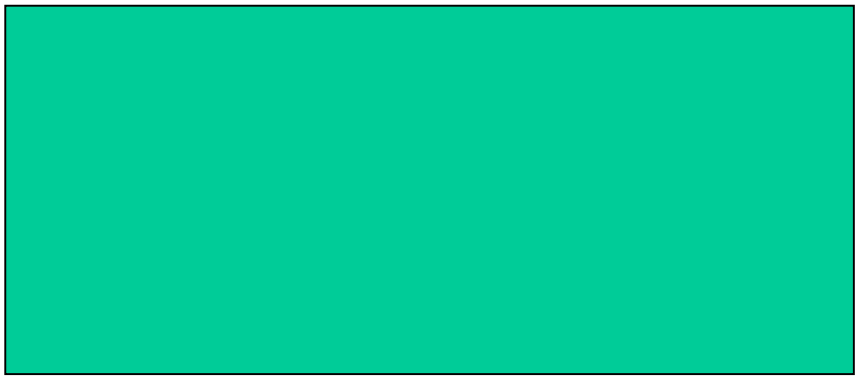
Low Voltage is Easy !



- Simple Devices
- Simple Resistors/Caps
- Latchup Easy to Avoid
- Inexpensive Tools Can Verify
- Few Devices in Library
- Few Layers
- Deep Sub-micron Geometries can Begin to Experience Effects Reminiscent of HV Designs

High Voltage Is Hard !



- Complex Well Structures with Buried Layers
- Many Complex Resistors/Cap/BJT/Diodes
- Proprietary Conductive Field Plate Materials & Knowhow with Custom Refractive Properties
- Proprietary Gate Oxide Geometries
- Many Layers
- Every Trace a Potential Latchup Candidate
- Proprietary Substrate Carrier Injection Protection
- Diffusion & Buried Layer Techniques for Wells & To Prevent Breakdown (Body Corners, etc.)
- Special Threshold Implant Control Techniques
- “Black Magic” Tricks of the Trade for Device Construction, Plate Geometries, and Reliability
- Many Devices in Library
- Very Expensive Equipment (100’s of k’s / seat)

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