DTE power over MDI

Power on the Signal Pairs

Further Testing based on Roger Karam's Results

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Acknowledgments:

Chris Cullen, Karl Nakamura, Roger Karam

intel

Reasons for this presentation

- **Test the Economic feasibility**
- **Test the Technical feasibility**
- **Define our position on Signal Pairs powering of DTE Devices**

Economic feasibility

- **Based on the presentations given by Chris Cullen and Karl Nakamura at our last meeting, as well as our own investigations it seems clear that;**
  - **It is desirable to support both wire pair sets in order to Have Broader Market Appeal**
  - **It is also clear that there is no substantial cost penalty for powering on either wire pair set.**

Technical Feasibility

- **At the last meeting we were treated to a presentation of lab measurements. The intent of the work was to confirm technical feasibility of power over the signal pairs.**

- **In order to verify these results, we agreed to undertake some additional testing in our lab. These results follow.**

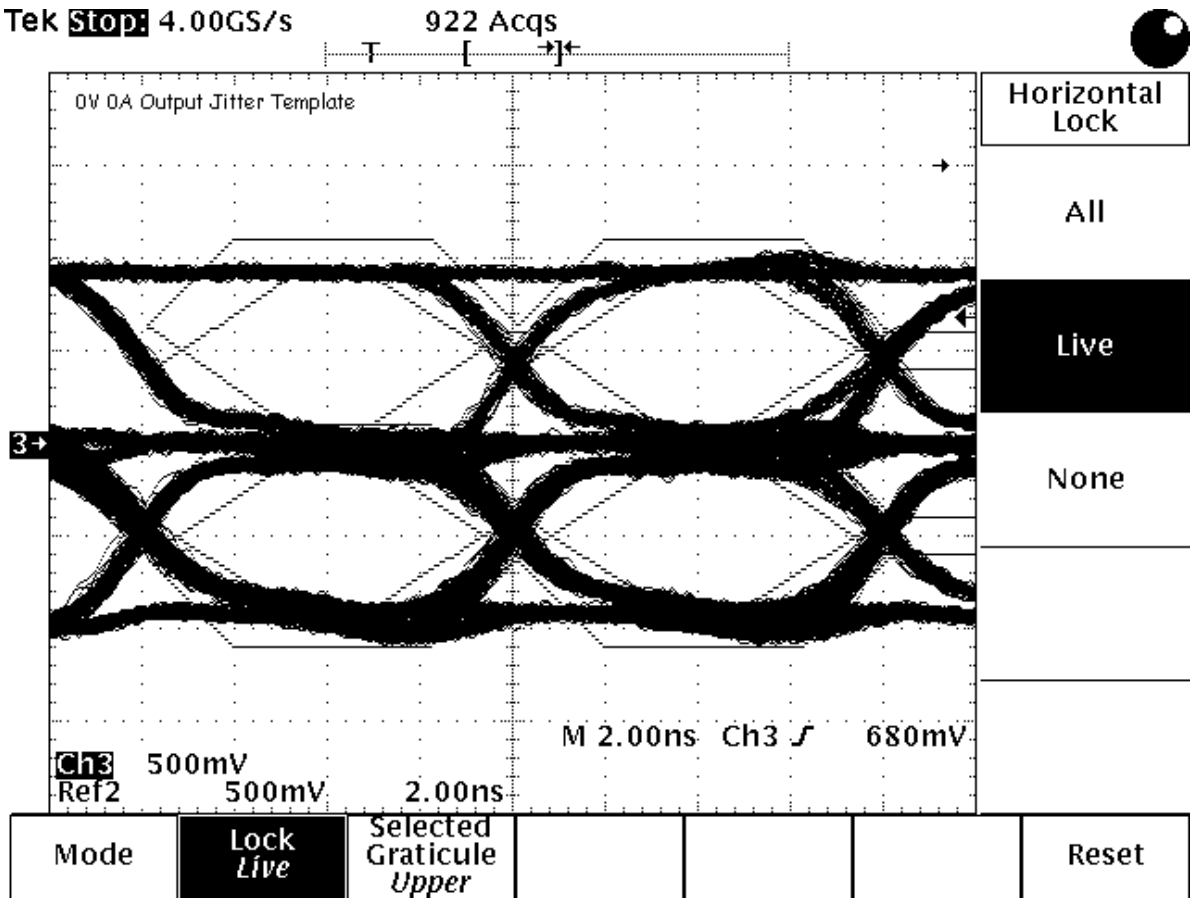
Technical Feasibility

- **A sub-set of the tests carried out by Roger were re-run in our lab.**
  - **8 different PHY devices were tested for general link performance. (Mix of vendors and date codes). The best and worst performers were chosen for the bulk of the testing.**

- **Tests carried out were;**
  - **BER with and without power**
  - **Signal Integrity, 100Mbit/s with and without power**

Differential Signal 0-Pk	**Amplitude Symmetry**
Rise/Fall Time	**Duty Cycle Distortion**
Transmit Jitter	**Overshoot**

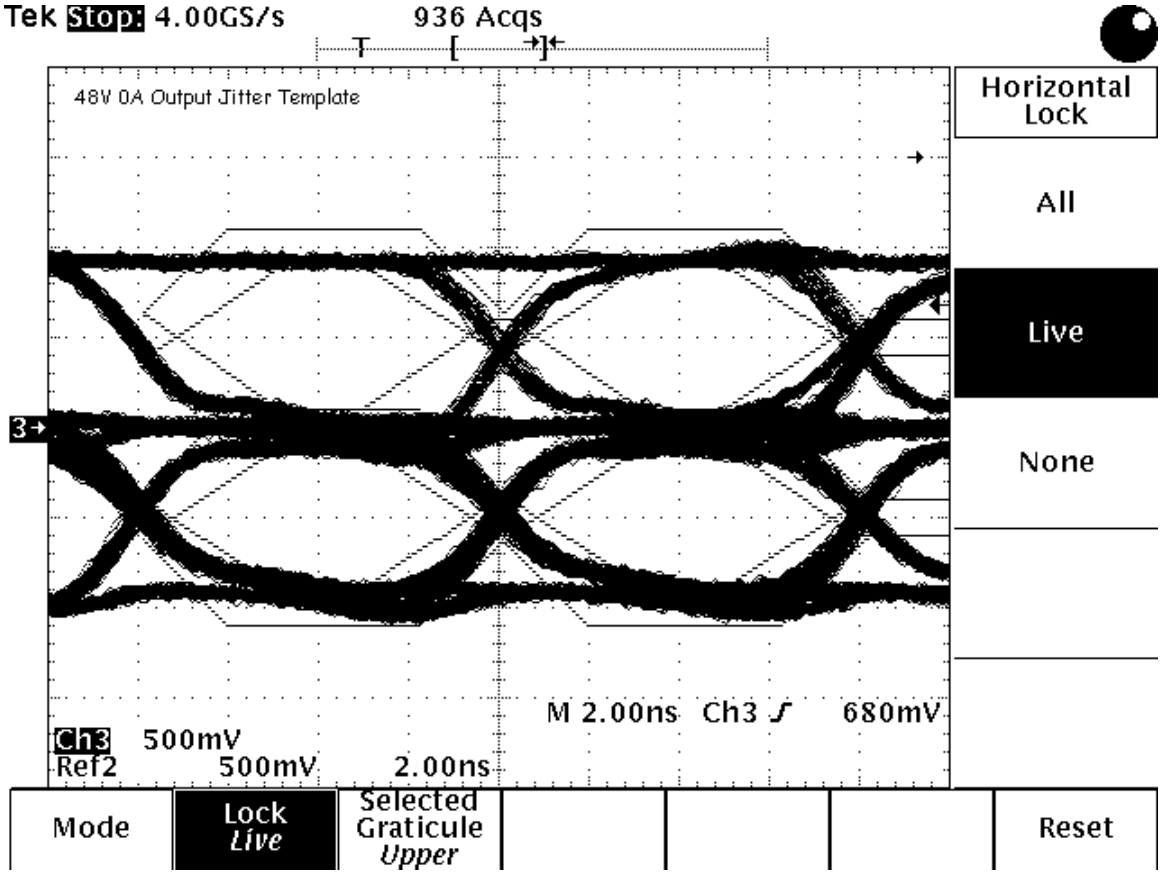
Technical Feasibility



Tx Eye and Jitter, V = 0, I = 0

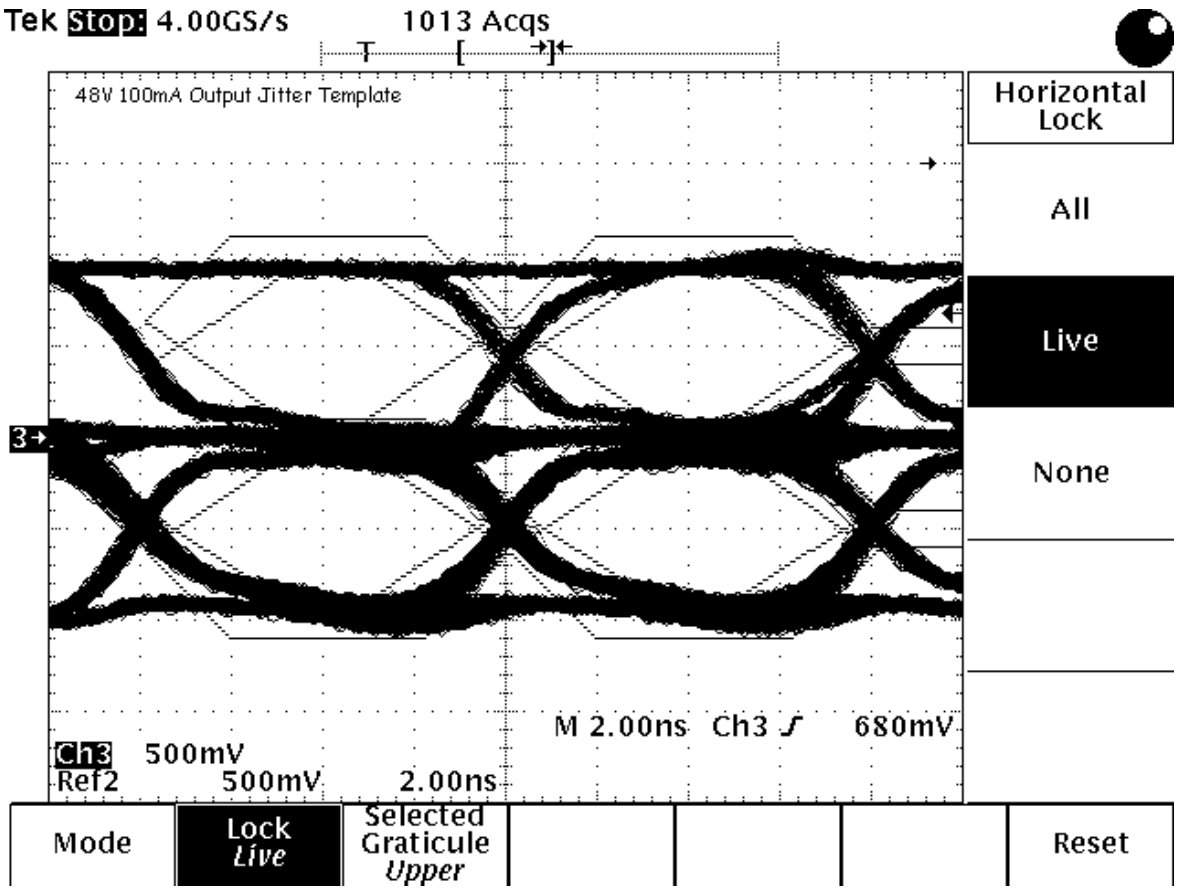
DTE power over MDI

Technical Feasibility



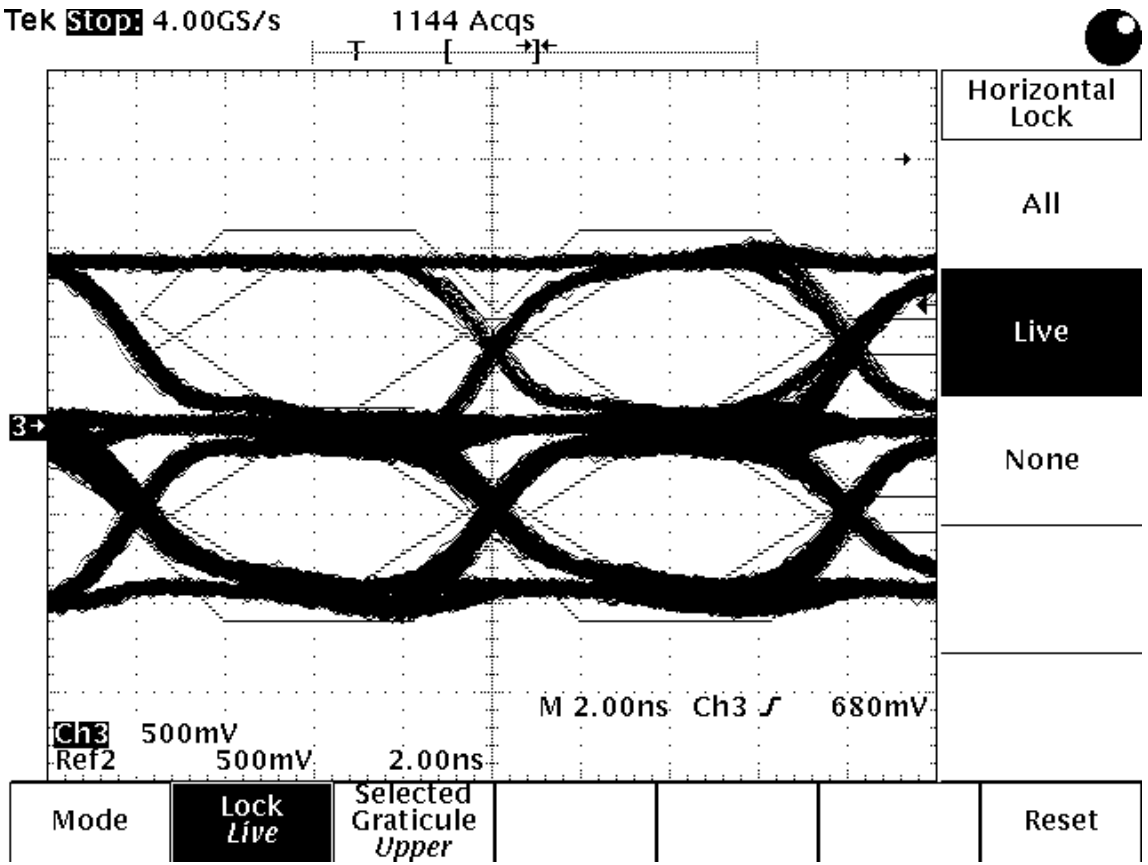
Tx Eye and Jitter, V = 48, I = 0

Technical Feasibility



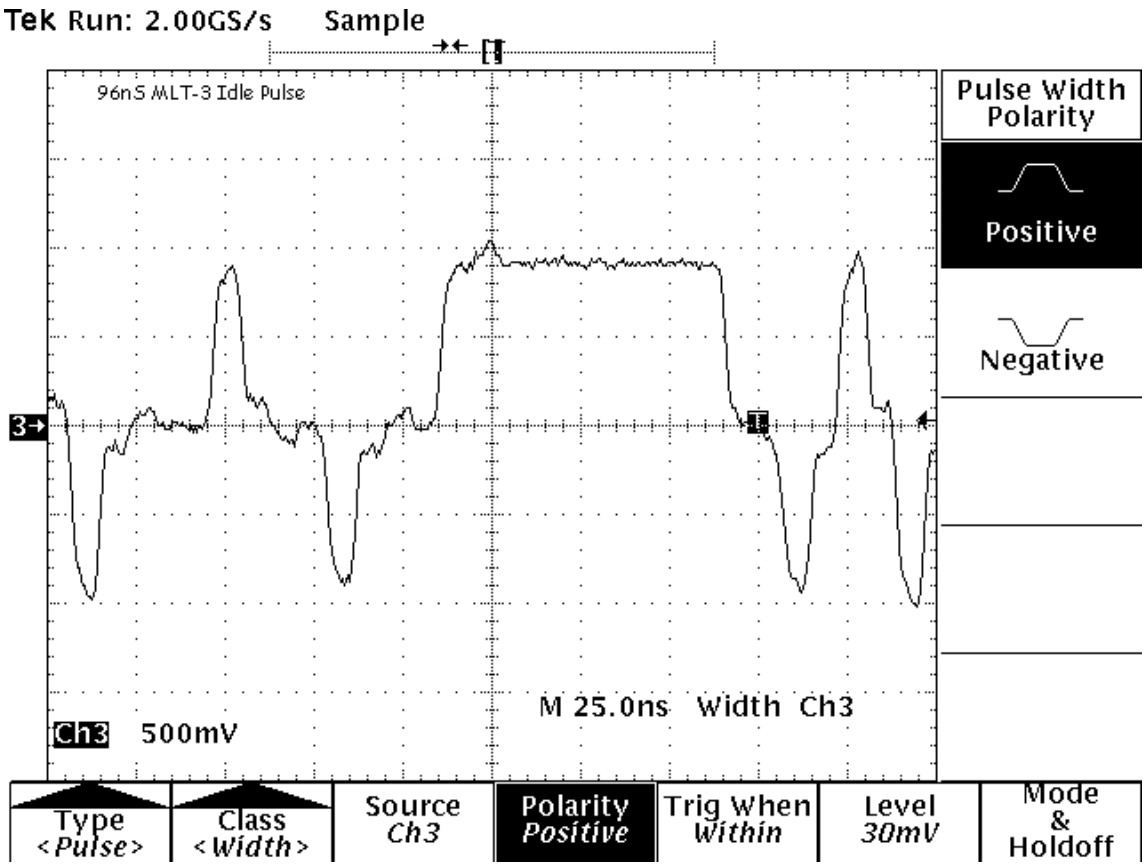
Tx Eye and Jitter, V = 48, I = 100mA

Technical Feasibility



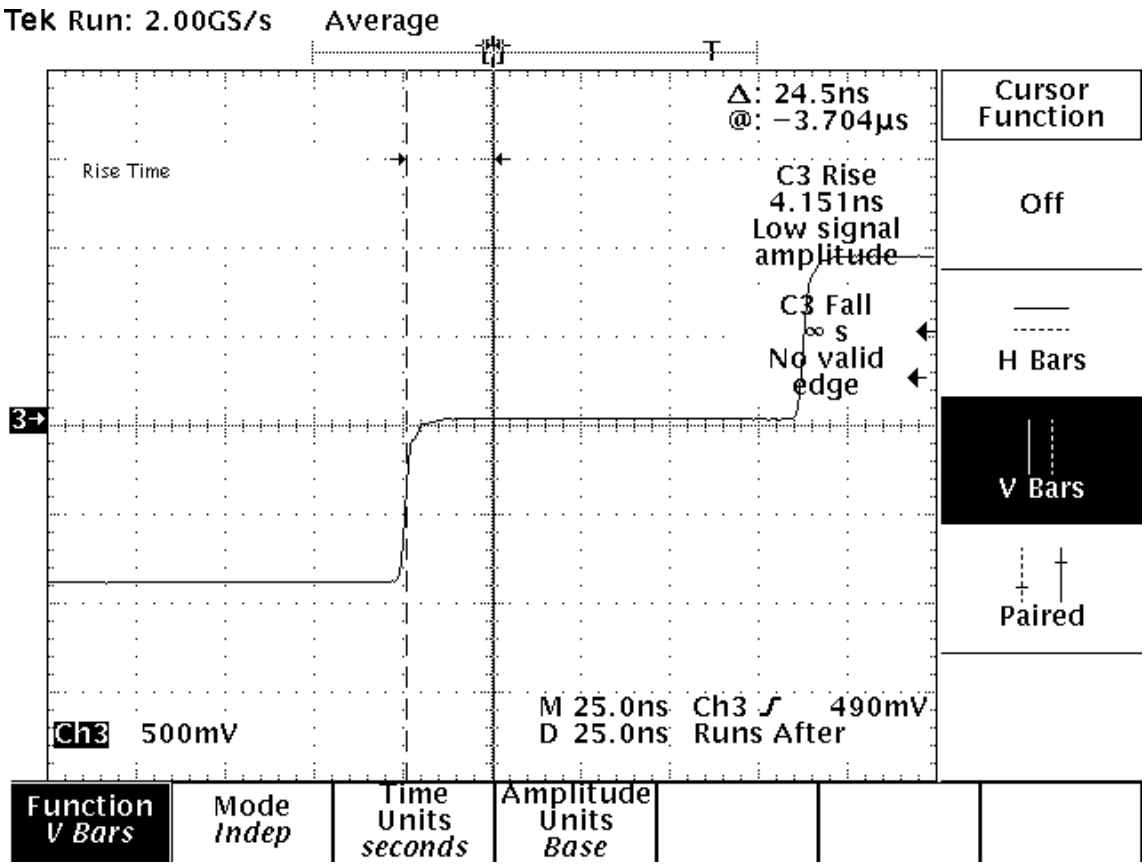
Tx Eye and Jitter, V = 48, I = 300mA

Technical Feasibility



Tx Waveform & Overshoot

Technical Feasibility



Tx Waveform, Rise/Fall Time

Technical Feasibility

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Characteristic	48V,0mA	48V,100mA	48V,300mA
Differential Signal			
Positive Peak	904.3mV	904.3mV	904.05mV
Negative Peak	899.6mV	899.8mV	900.45mV
Rise/Fall Time	2.31/2.26ns	2.29/2.27ns	2.27/2.25ns
Duty Cycle Distortion			
Positive Width	16.078ns	16.031ns	15.998ns
Negative Width	16.043ns	16.122ns	16.035ns
Transmit Jitter	870ps	880ps	870ps

Technical Feasibility

- **Conclusions**
  - **Based on the testing carried out and the data gathered it can clearly be seen that our results are in agreement with those previously presented by Roger.**
  - **Thus we believe that technical feasibility for the signal pair, and as will be shown in later presentations, for the non-signal pair has been proven.**
  - **The limiting factor will be EMI compliance due to switcher supply noise NOT degradation of the Link performance.**

Our Position on DTE Power

- **We supports the powering of PD devices via either Signal or Idle wire pair sets.**

- **This stance is taken based on the data presented or referenced in the previous slides which we believe show a convincing Economic and Technical proof of the viability of either approach.**