Diode Discovery Process Lab Testing Results

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Acknowledgments:
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Agenda

- **Requirement for Testing**
- **Test Method and Device Selection**
- **Operational Effects - BER**
- **Signal Integrity - 100M**
- **Signal Integrity – 10M**
- **Conclusions**

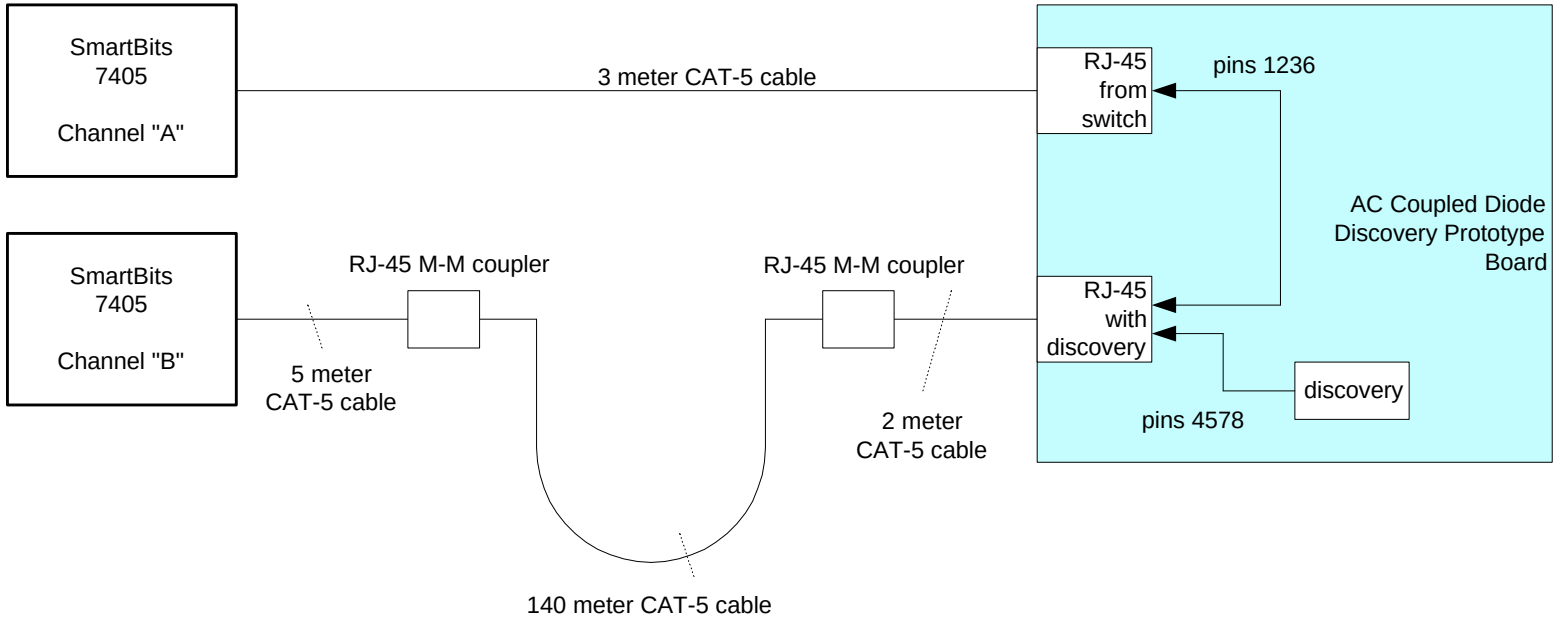
Requirement for this testing

- **The requirement for this series of tests is two fold;**
  - **Having seen the excellent work carried out by Roger Karam on the technical feasibility of power transfer over the signal pairs. The gauntlet was thrown down that someone should do something similar for the “idle pairs”.**
  - **To show that the Diode Discovery Process does not degrade the signal quality of the transmitted data on the MDI link and will therefore not have any detrimental effect on legacy PHYs or equipment already deployed in the field.**

Test Method and Device Selection

- **In order to set a base line for all of the tests to be comparative, BER testing against line length was used.**
  - **8 Different PHY devices were tested. Each was run to the longest line length possible for error free operation.**
  - **The best performing (Good PHY) and the worst performing (Bad PHY) devices were chosen. This is hoped to set the bounds of the majority of PHY products deployed in the field.**
  - **These two PHY devices were used in the testing that follows.**
  - **The schematic for the test bench is shown on the next slide.**

Test Method and Device Selection



- **The block diagram above shows the test set up used for this testing.**
  - **The 2,3,5 meter patch cables are included to ensure a realistic cable structure and maximize the impedance mis-match usually associated with these patch cords.**
  - **The 140m cable is the part of the cable plant that was varied in length during these tests. This cable is made up of various numbers of 25m, 10m and 1m cables connected together with RJ-45 MM couplers. This cable plant includes more sources of impairment than the specified worst case.**

DTE power over MDI

Operational Effects

- **BER Effects**
  - **PHY Devices were tested against line length to indicate degradation in performance.**
  - **The line length was noted at each point when the PHY became error free again. Each PHY was tested under the following conditions;**
    - **No Power, No Discovery**
    - **No Power, Discovery running continuously**
    - **Power On, Discovery On, No Load**
    - **Power On, Discovery On, 100mA Load**
    - **Power On, Discovery On, 300mA Load**
- **The results are shown in the following slides.**

Operational Effects

No Power, No Discovery

- **Shown below is the results captured from SmartBits**
- **The Good PHY is connected on Ports 1 and 5 this shows error at a line length of 163 m**
- **The Bad PHY is connected on Ports 2 and 4 this shows error at a line length of 99 m**

SmartCounters,1	Events	Events	Events	Events
	01 SX-7210	02 SX-7210	04 SX-7210	05 SX-7210
Tx Frames	56,165,714	56,163,463	56,163,463	56,165,714
Rx Frames	56,165,714	56,163,319	56,163,463	56,165,709
Rx Bytes	3,594,605,696	3,594,461,632	3,594,461,632	3,594,605,696
Rx Triggers	0	0	0	0
Collisions	0	0	0	0
CRC Errors	0	144	0	5
Alignment Errors	0	0	0	0
OverSize	0	0	0	0
Frag/UnderSize	0	0	0	0

Operational Effects

No Power, No Discovery

- **The Good PHY is connected on Ports 1 and 5 this shows error free operation at a line length of 161 m**
- **The Bad PHY is connected on Ports 2 and 4 this shows error free operation at a line length of 98 m**

SmartCounters,1	Events	Events	Events	Events
	01 SX-7210	02 SX-7210	04 SX-7210	05 SX-7210
Tx Frames	47,301,749	47,299,843	47,299,843	47,301,749
Rx Frames	47,301,749	47,299,843	47,299,843	47,301,749
Rx Bytes	3,027,311,936	3,027,189,952	3,027,189,952	3,027,311,936
Rx Triggers	0	0	0	0
Collisions	0	0	0	0
CRC Errors	0	0	0	0
Alignment Errors	0	0	0	0
OverSize	0	0	0	0
Frag/UnderSize	0	0	0	0

DTE power over MDI

Operational Effects
Good PHY

DTE power over MDI

- **No Power, No Discovery**
  - **Error free operation was achieved at a line length of 161m**
- **No Power, Discovery running continuously**
  - **Error free operation was achieved at a line length of 161m**
- **Power On, Discovery On, No Load**
  - **Error free operation was achieved at a line length of 139m**
- **Power On, Discovery On, 100mA Load**
  - **Error free operation was achieved at a line length of 155m**
- **Power On, Discovery On, 300mA Load**
  - **Error free operation was achieved at a line length of 152m**

Operational Effects
Bad PHY

- **No Power, No Discovery**
  - **Error free operation was achieved at a line length of 98m**
- **No Power, Discovery running continuously**
  - **Error free operation was achieved at a line length of 98m**
- **Power On, Discovery On, No Load**
  - **Error free operation was achieved at a line length of 91m**
- **Power On, Discovery On, 100mA Load**
  - **Error free operation was achieved at a line length of 96.5m**
- **Power On, Discovery On, 300mA Load**
  - **Error free operation was achieved at a line length of 96m**

Operational Effects
Conclusions

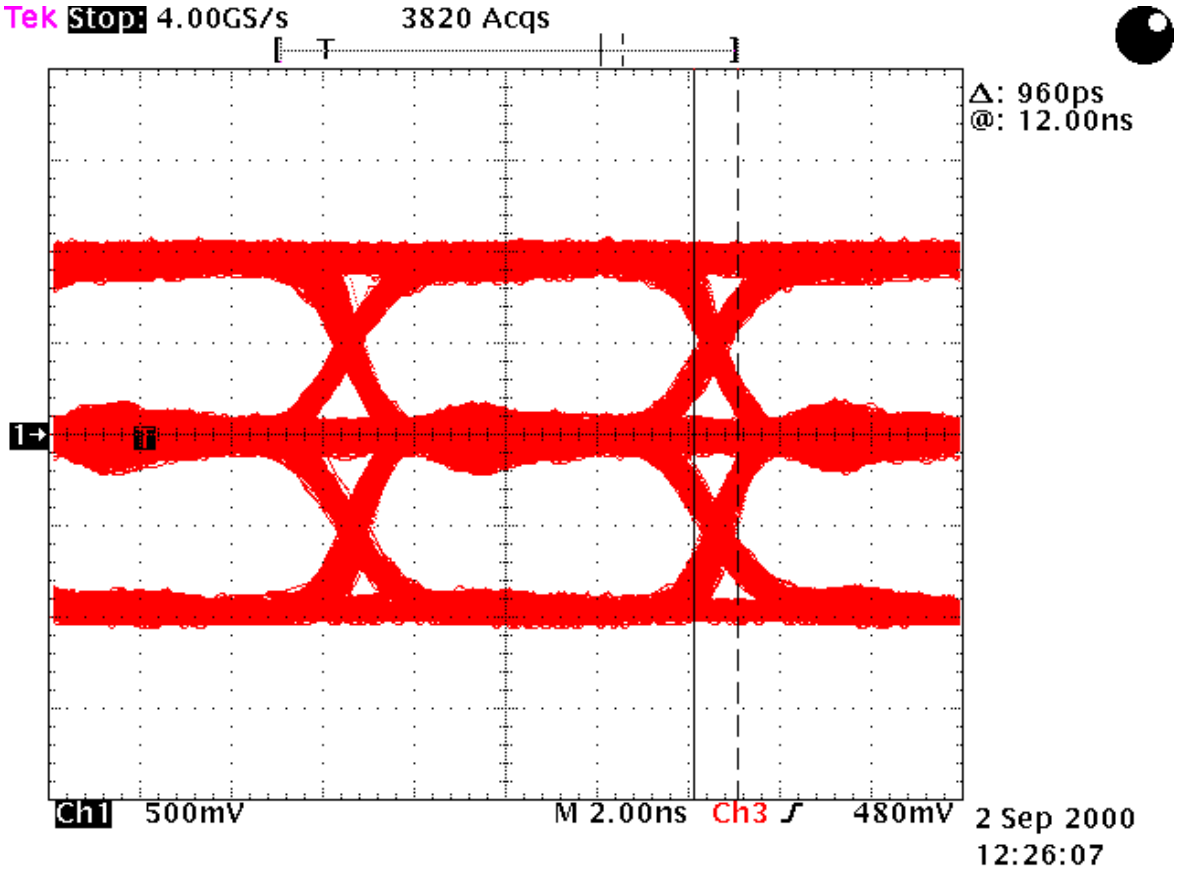
- **These results demonstrate that the Discovery detection process has no effect on the performance of the PHY device and as such does not degrade the existing MDI link.**
- **It can also be clearly seen that the power supply will degrade the MDI link.**
- **This is especially true in a failure mode as shown in “Power On, Discovery On, No Load” test case where the power supply is allowed to cycle on and off continuously.**
- **Full results of these tests are available in a separate word document. These have been posted on the web.**

Signal Integrity - 100M

- **Each PHY device had the following signal integrity tests carried out;**
  - **Differential Signal 0-Pk**
  - **Rise/Fall Time**
  - **Transmit Jitter**
  - **Amplitude Symmetry**
  - **Duty Cycle Distortion**
  - **Overshoot**
- **These tests were carried out under the following conditions**
  - **No Power, No Discovery**
  - **No Power, Discovery running continuously**
  - **Power On, Discovery On, 300mA Load**

Signal Integrity - 100M

Good PHY

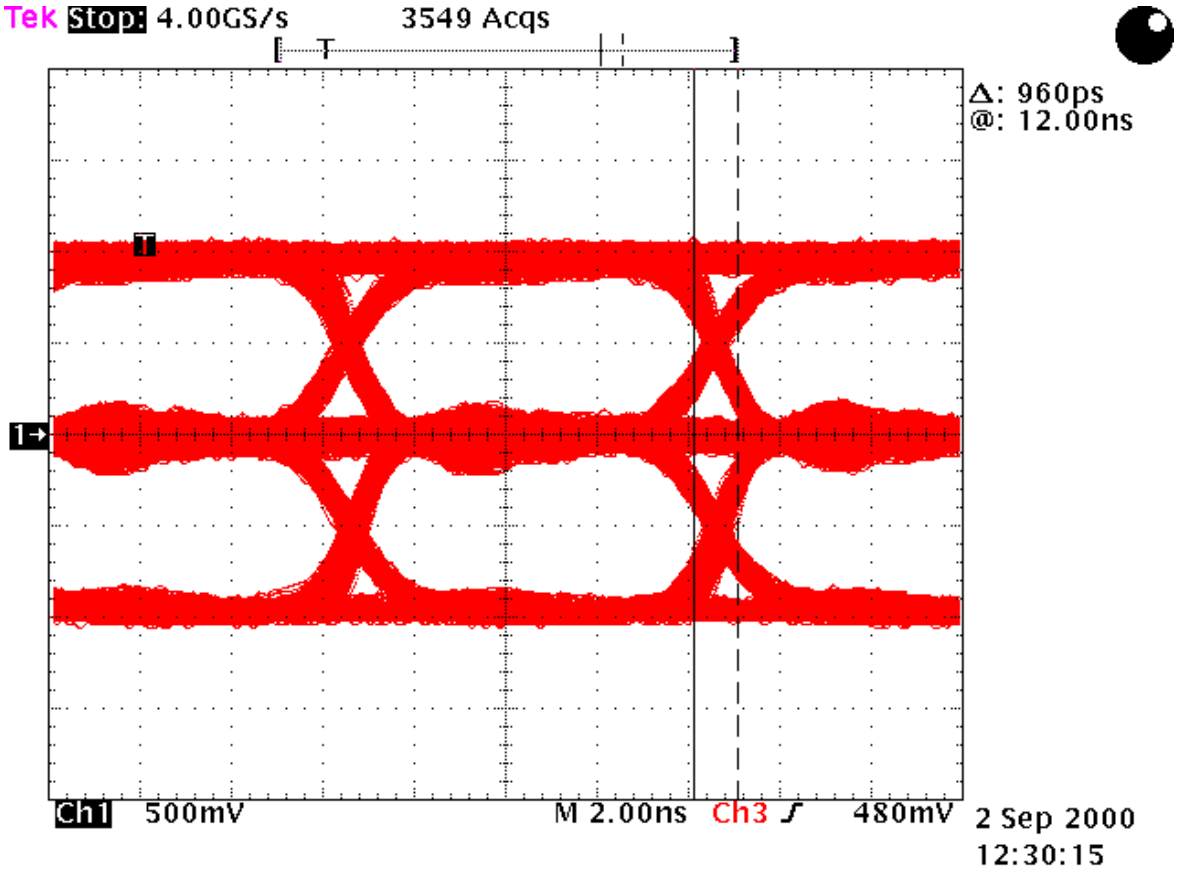


Tx Eye and Jitter, No Discovery, No Power

DTE power over MDI

Signal Integrity - 100M

Good PHY

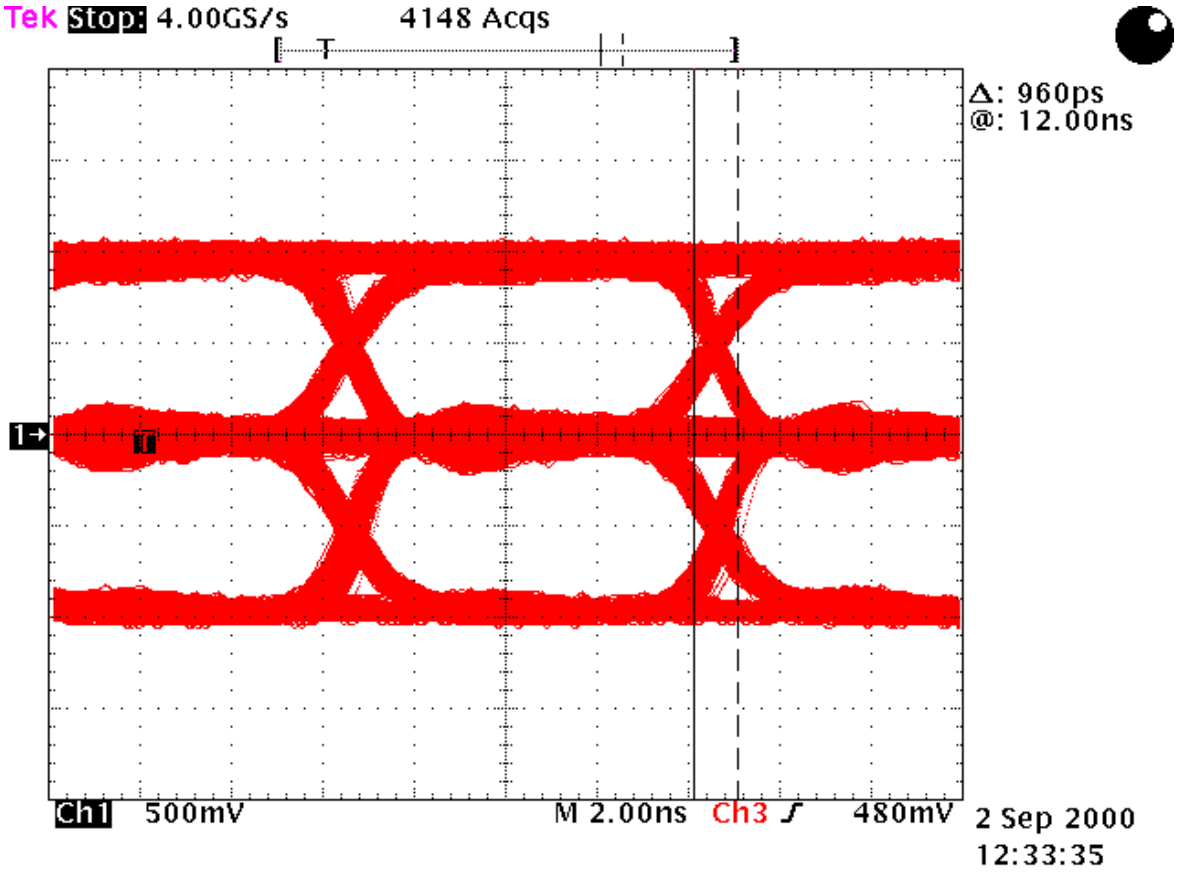


Tx Eye and Jitter, No Power, Discovery On

DTE power over MDI

Signal Integrity - 100M

Good PHY

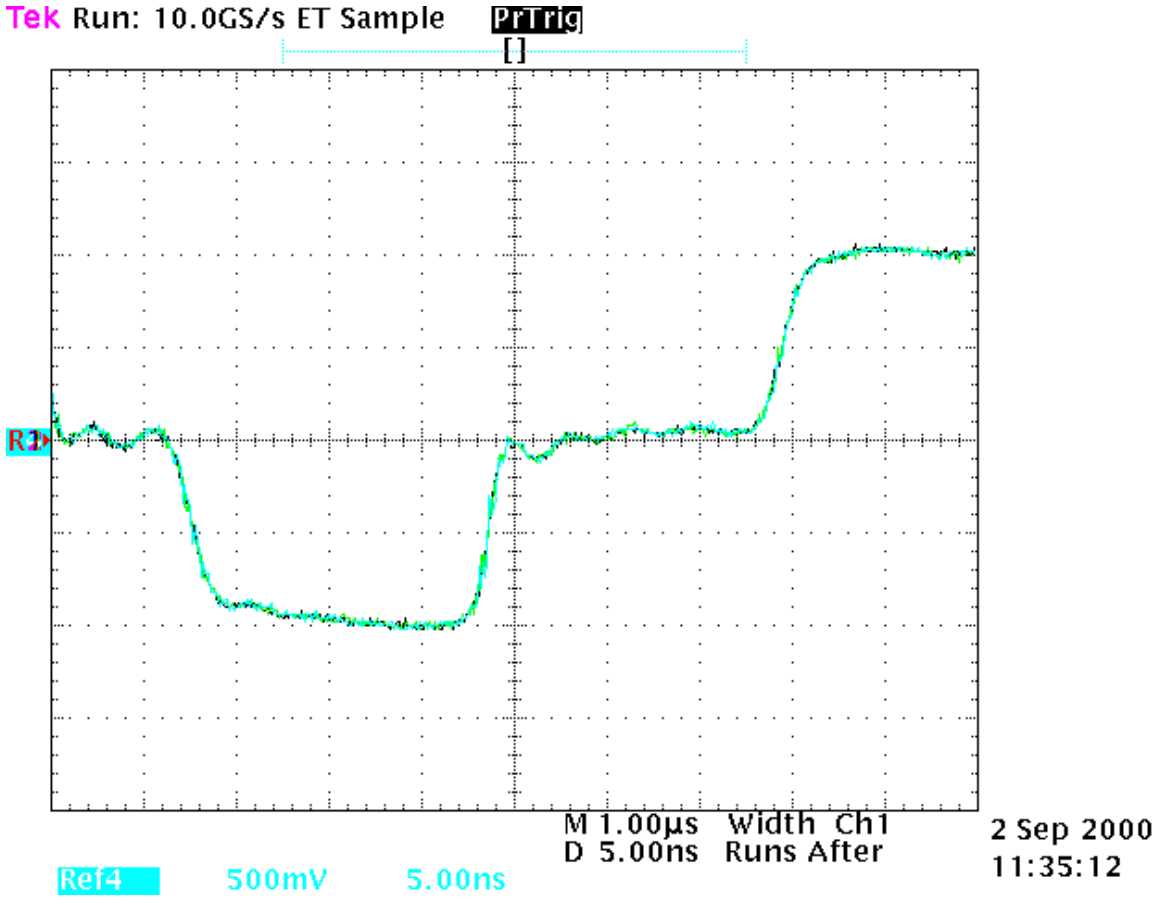


Tx Eye and Jitter, Power On, Discovery On, I = 300mA

DTE power over MDI

Signal Integrity - 100M

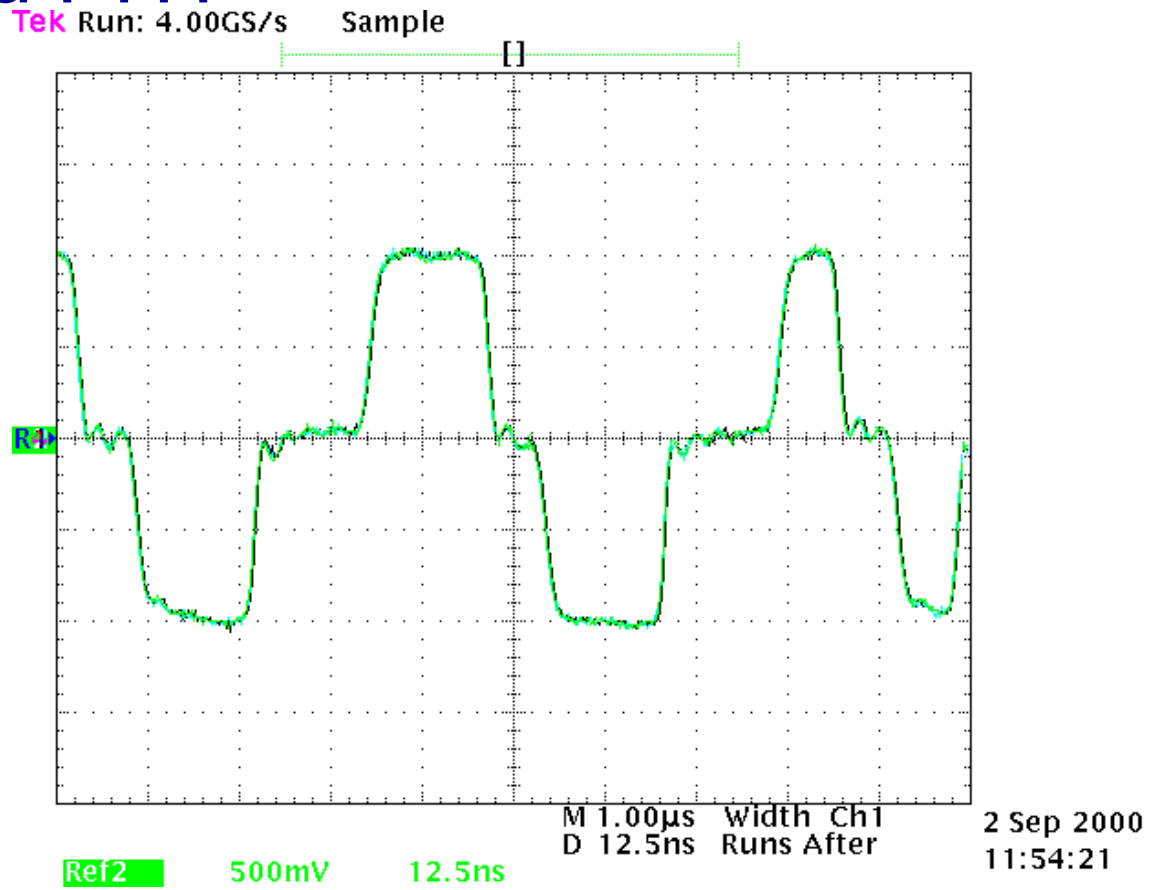
Good PHY



Tx Overshoot, All three conditions

Signal Integrity - 100M

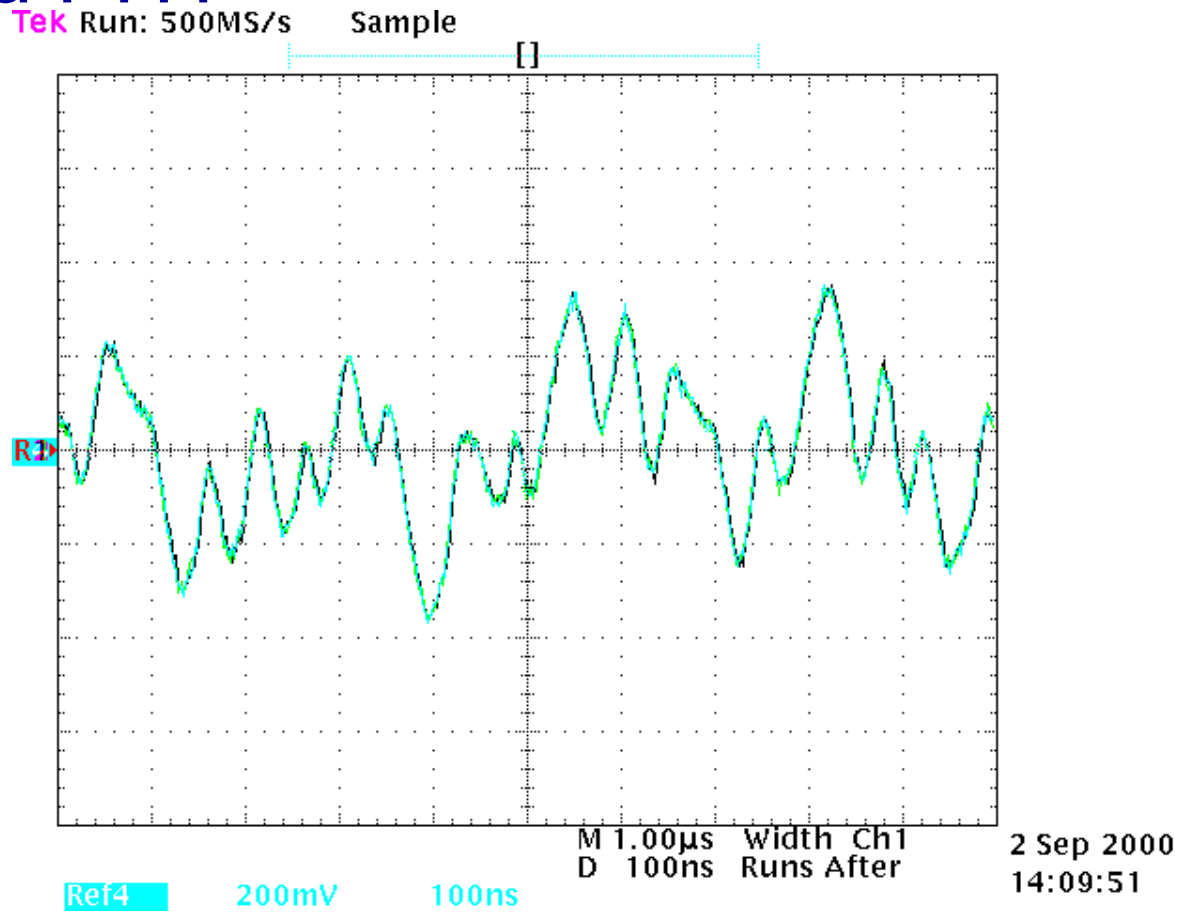
Good PHY



Tx Duty Cycle Distortion, All three conditions

Signal Integrity - 100M

Good PHY



Rx Waveform at 152m

DTE power over MDI

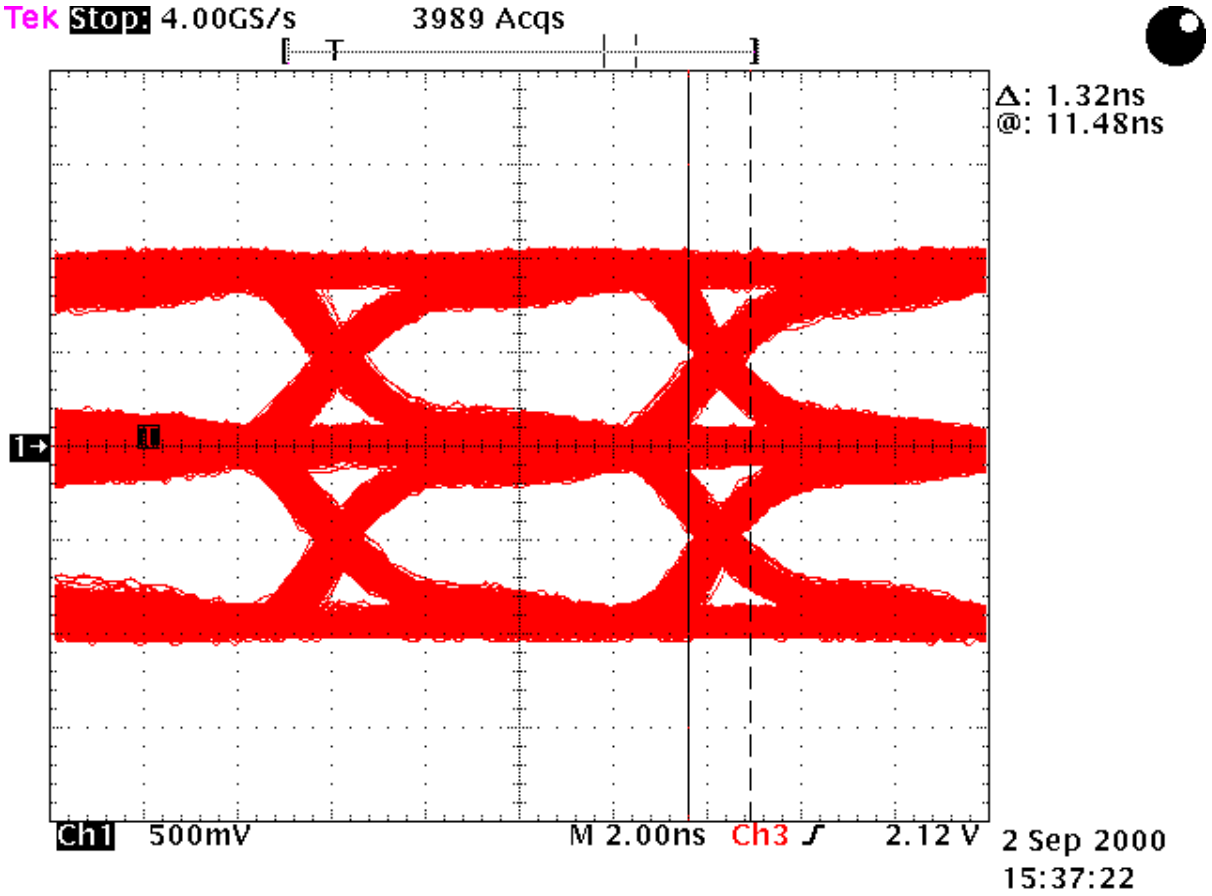
Signal Integrity - 100M
Good PHY – Results Summary

DTE power over MDI

Characteristic	Normal	Discovery	Power
Differential Signal			
Positive Peak	1.03V	1.03V	1.03V
Negative Peak	1.02V	1.02V	1.02V
Rise/Fall Time	2.1/3.6ns	2.1/3.6ns	2.1/3.6ns
Duty Cycle Distortion			
Positive Width	16.2ns	16.2ns	16.2ns
Negative Width	16.2ns	16.2ns	16.2ns
Transmit Jitter	960ps	960ps	960ps

Signal Integrity - 100M

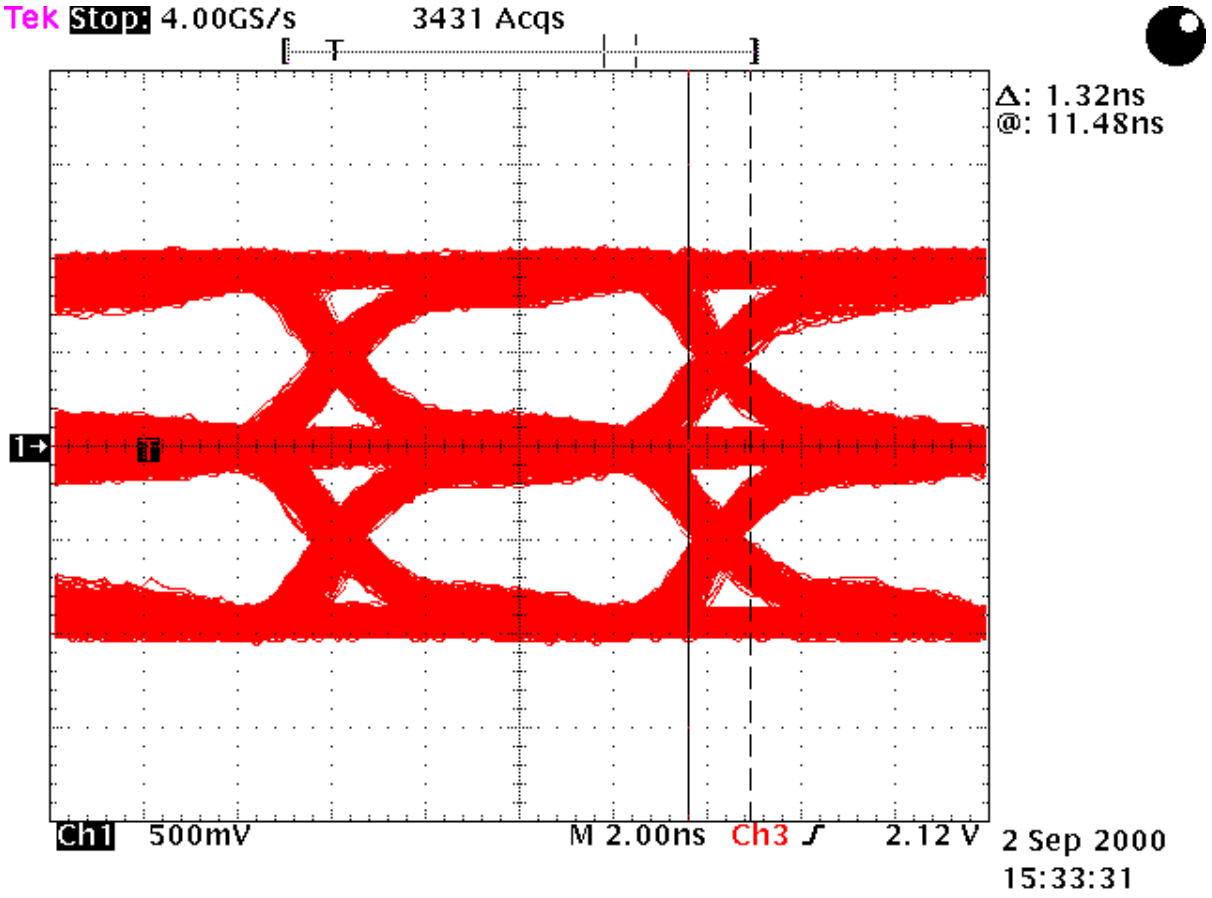
Bad PHY



Tx Eye and Jitter, No Discovery, No Power

Signal Integrity - 100M

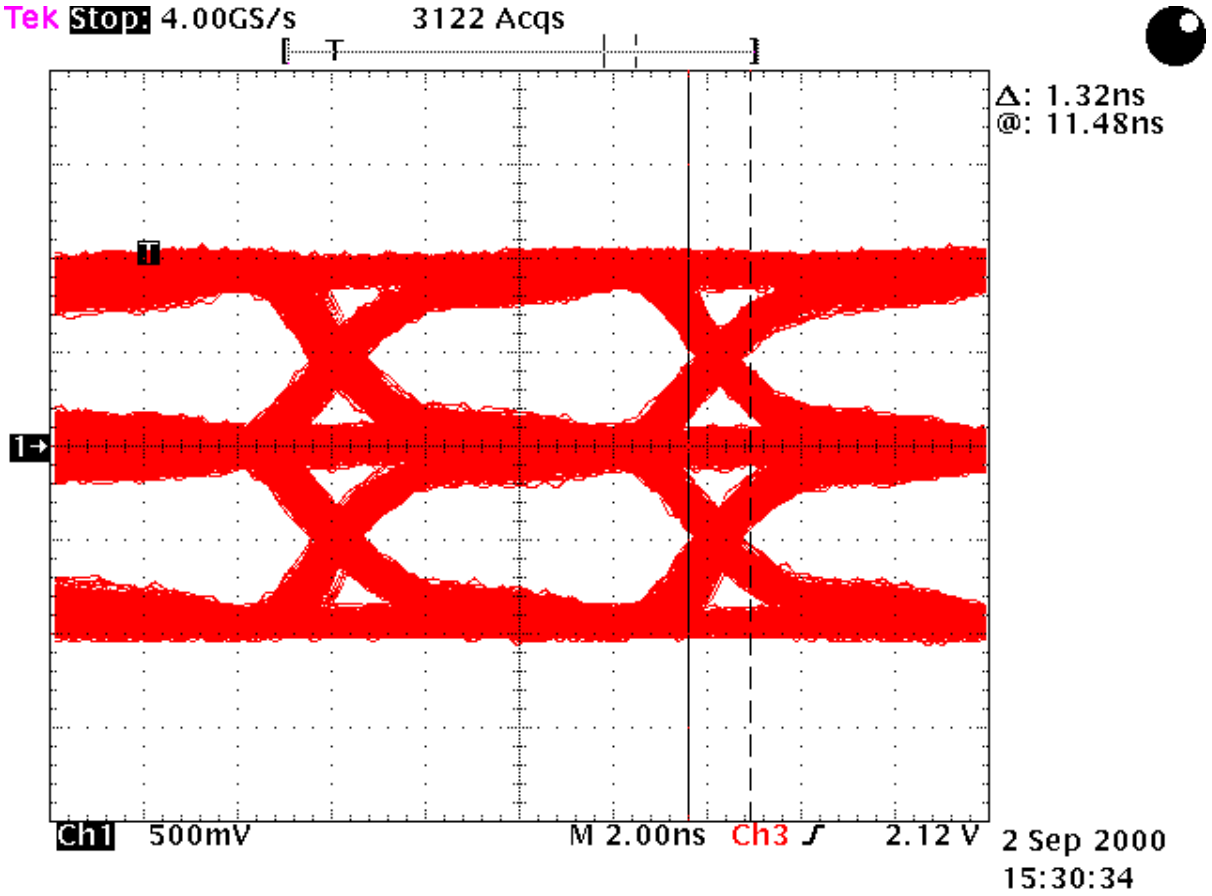
Bad PHY



Tx Eye and Jitter, No Power, Discovery On

Signal Integrity - 100M

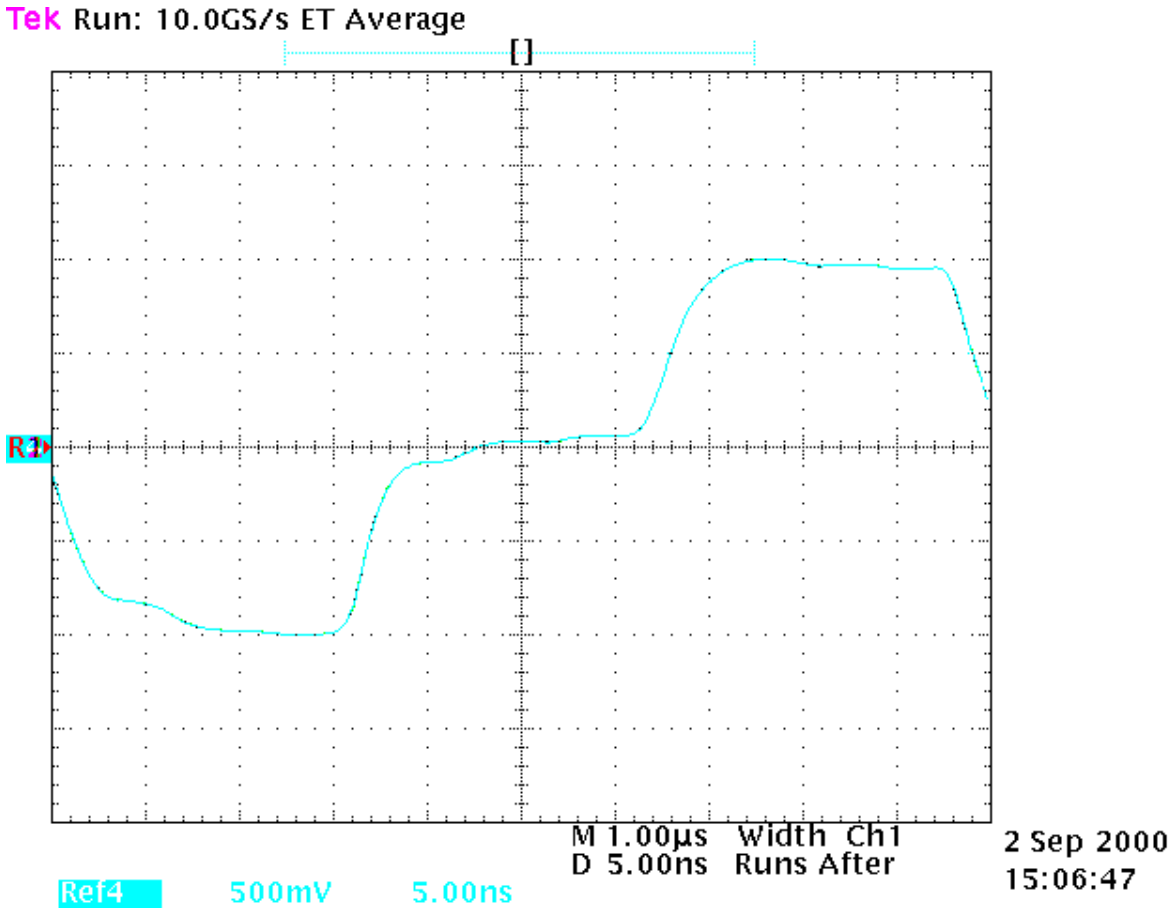
Bad PHY



Tx Eye and Jitter, Power On, Discovery On, I = 300mA

Signal Integrity - 100M

Bad PHY

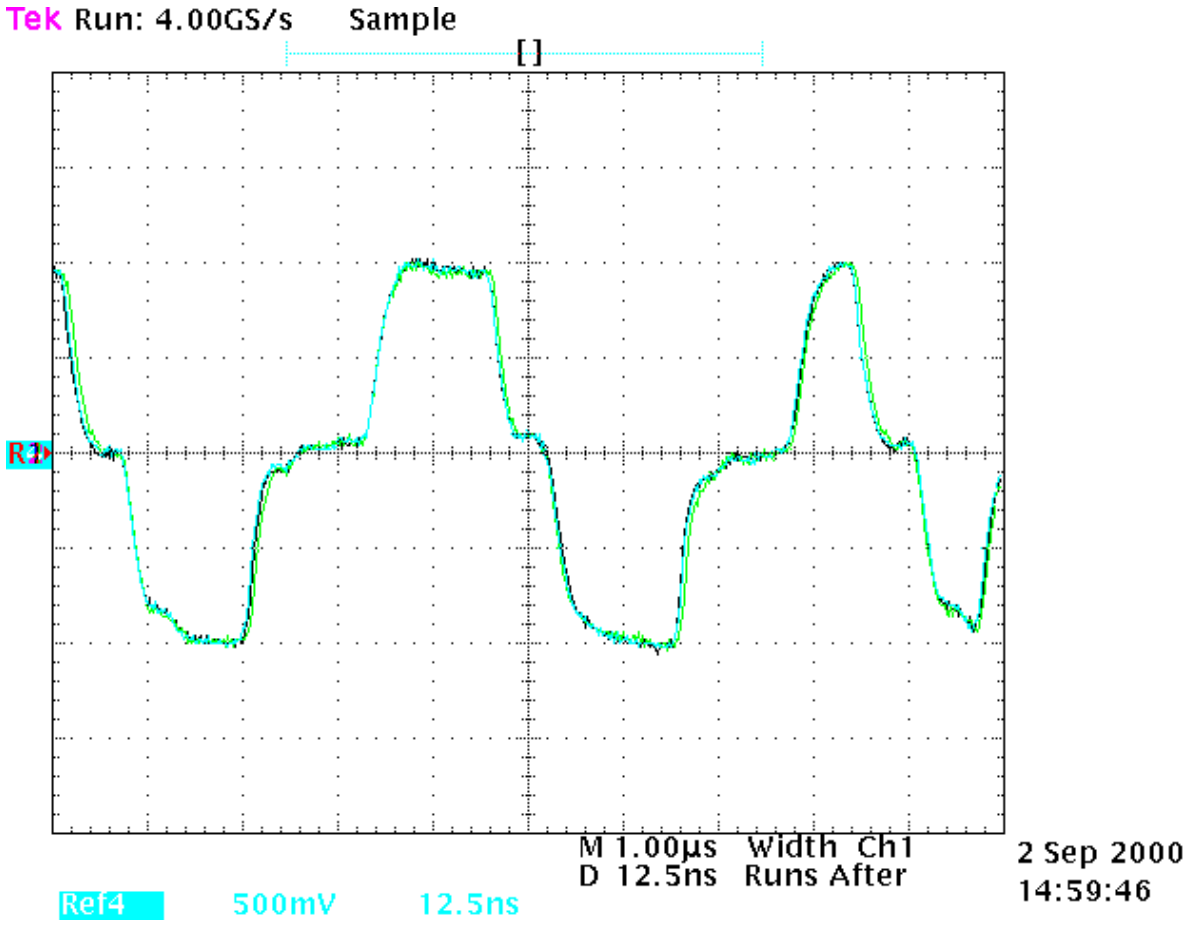


Tx Overshoot, All three conditions

DTE power over MDI

Signal Integrity - 100M

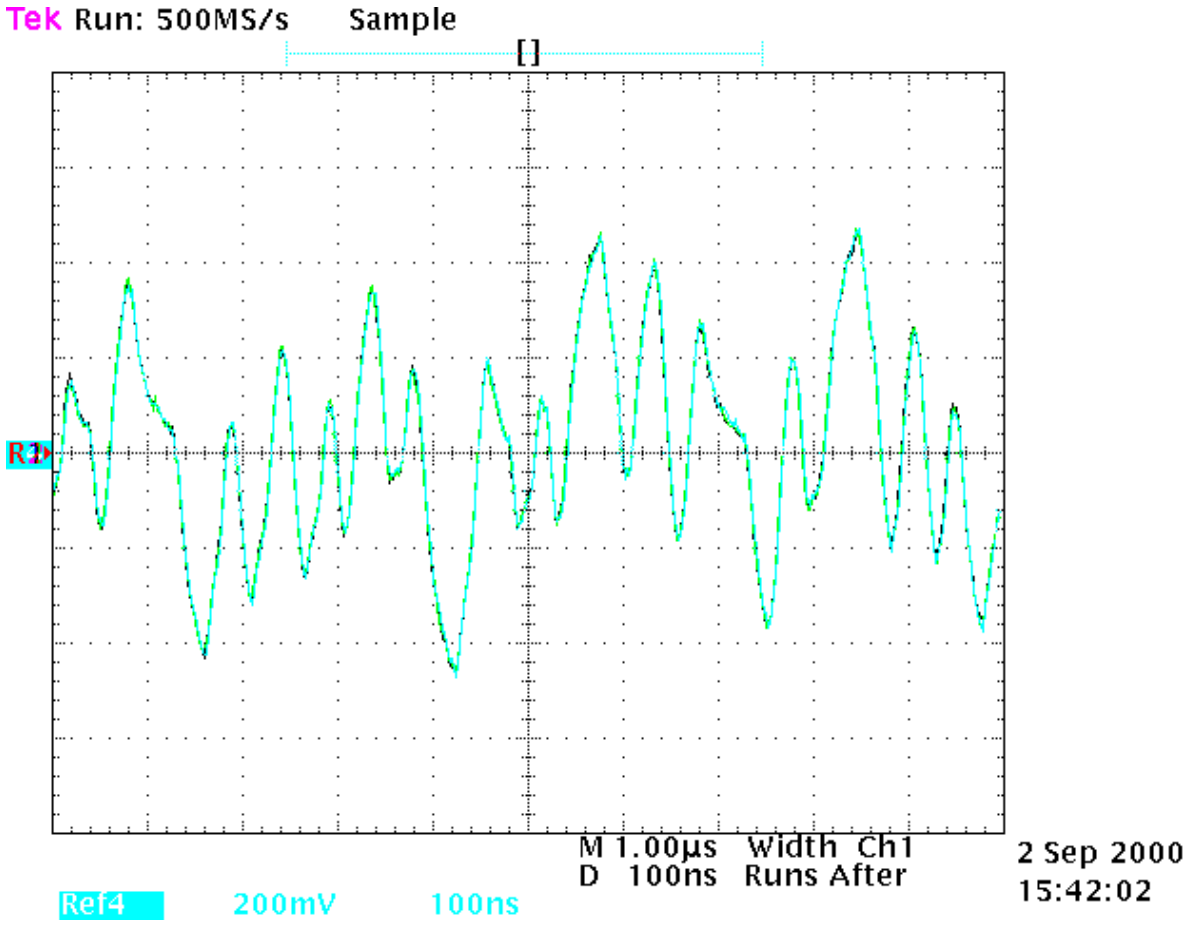
Bad PHY



Tx Duty Cycle Distortion, All three conditions

Signal Integrity - 100M

Bad PHY



Rx Waveform at 96m

DTE power over MDI

Signal Integrity - 100M
Bad PHY – Results Summary

DTE power over MDI

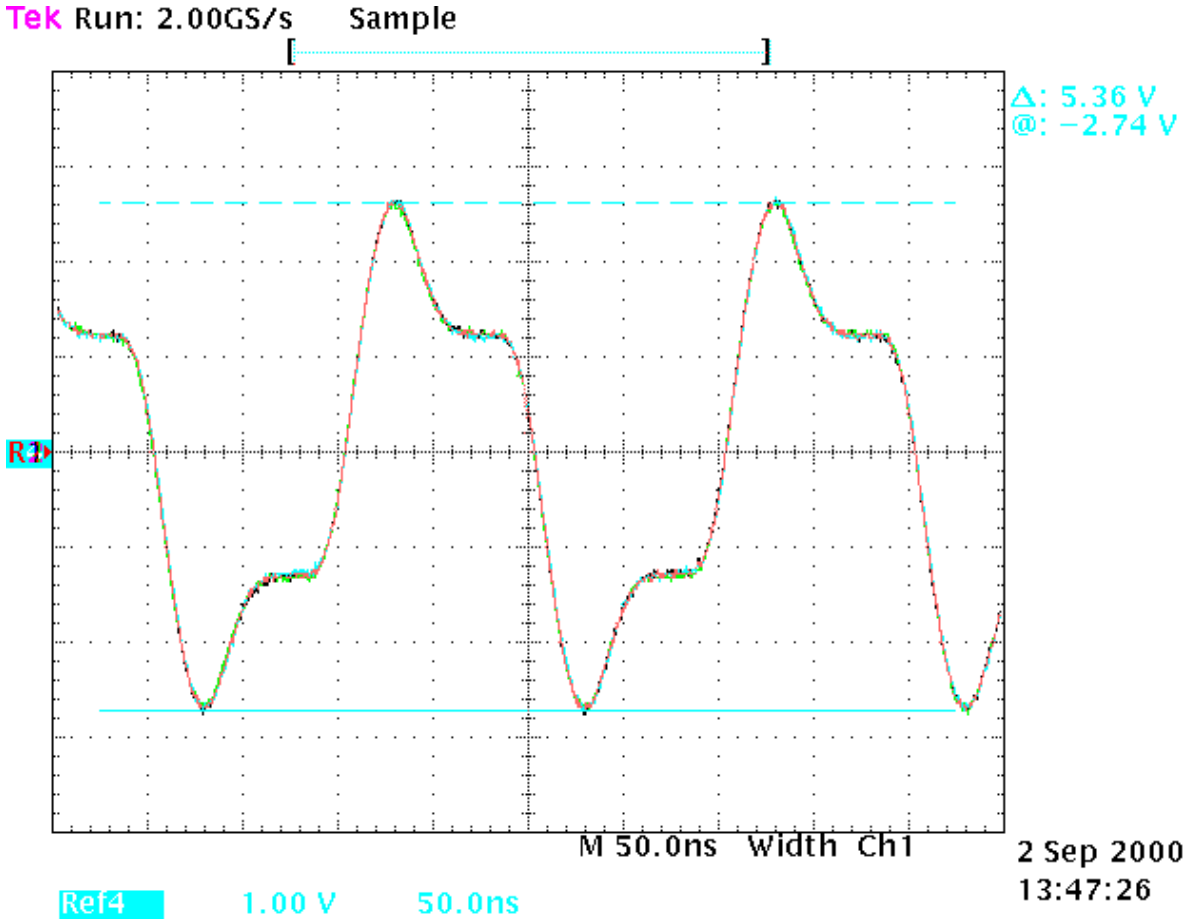
Characteristic	Normal	Discovery	Power
Differential Signal			
Positive Peak	1.00V	1.00V	1.00V
Negative Peak	1.01V	1.01V	1.01V
Rise/Fall Time	3.9/3.6ns	3.9/3.6ns	3.9/3.6ns
Duty Cycle Distortion			
Positive Width	16.5ns	16.5ns	16.5ns
Negative Width	16.3ns	16.3ns	16.3ns
Transmit Jitter	1.32ns	1.32ns	1.32ns

Signal Integrity - 10M

- **Each PHY device had the following signal integrity tests carried out;**
  - **Peak Differential Output Voltage**
  - **Output Waveform vs Template**
  - **Start Of TP_IDL(End of 10Base-T Packet) waveform vs Template**
  - **Link Test Pulse vs Template**
- **These tests were carried out under the following conditions**
  - **No Power, No Discovery**
  - **No Power, Discovery running continuously**
  - **Power On, Discovery On, 300mA Load**

Signal Integrity - 10M

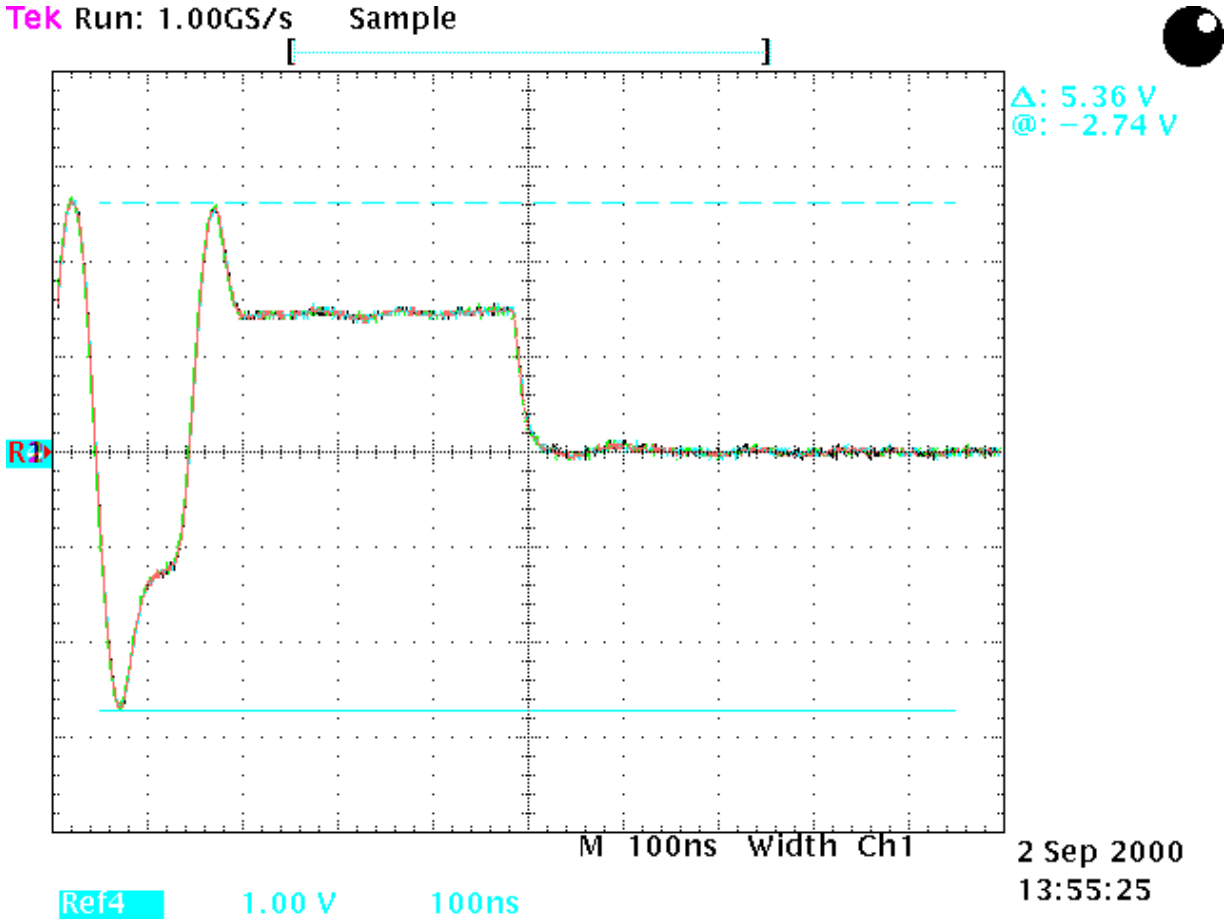
Good PHY



10Mbit/s Signal, All three conditions

Signal Integrity - 10M

Good PHY

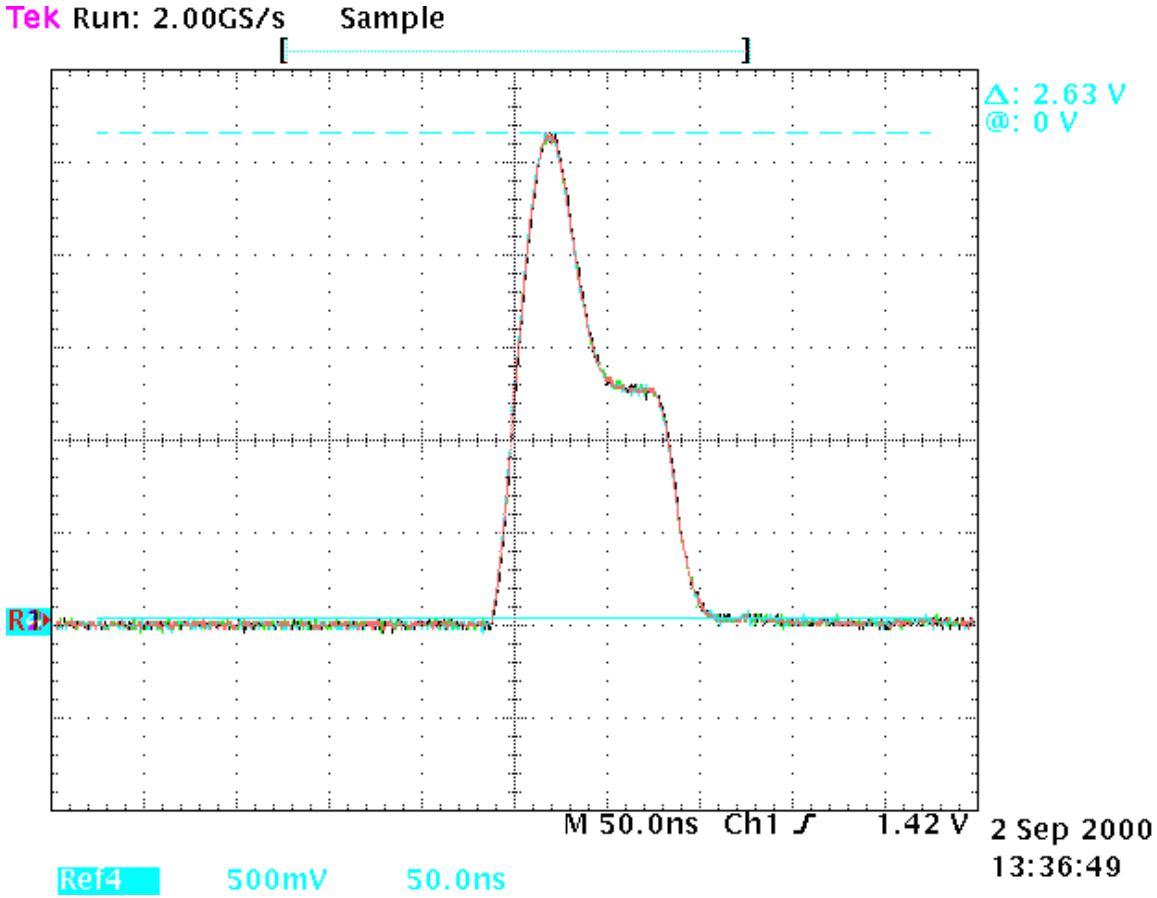


10 Mbit/s Start of TP_IDL, All three conditions

DTE power over MDI

Signal Integrity - 10M

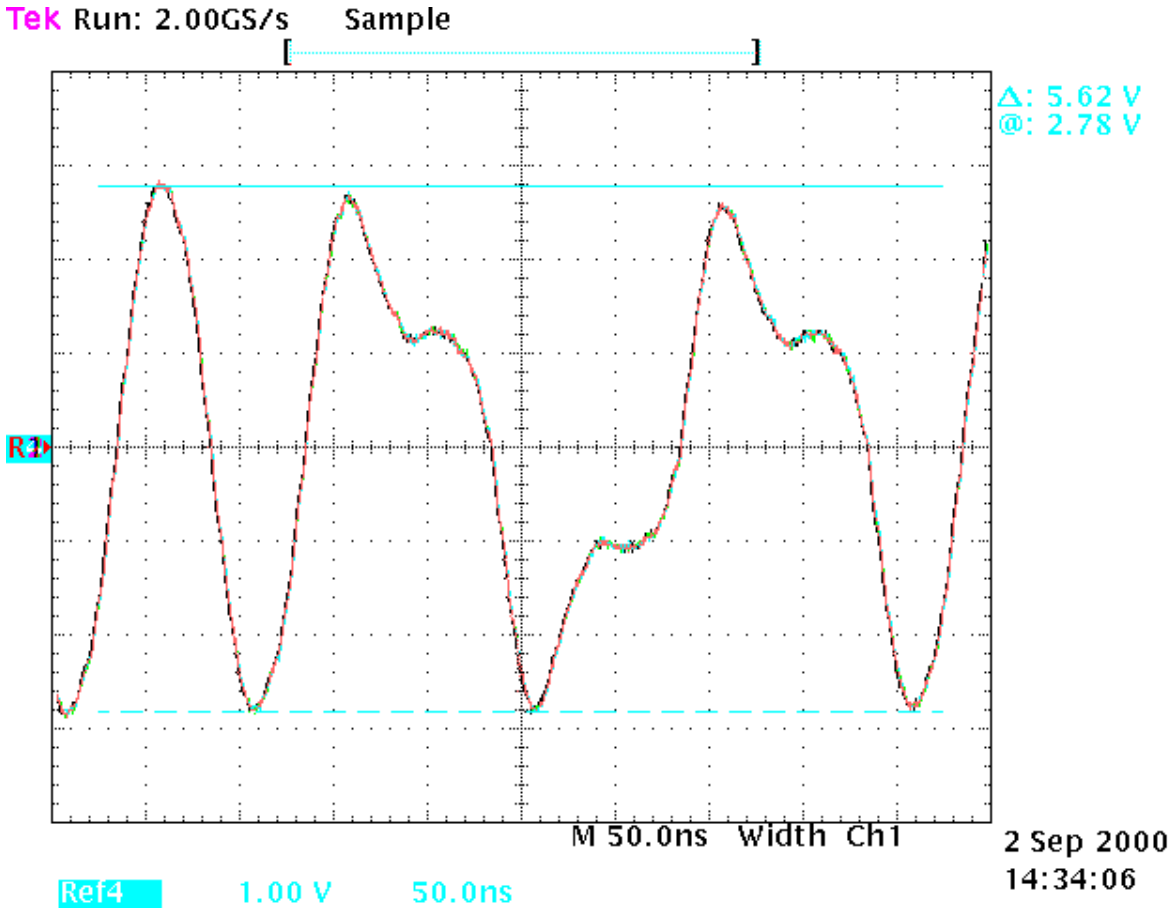
Good PHY



10 Mbit/s Link Pulse, All three conditions

Signal Integrity - 10M

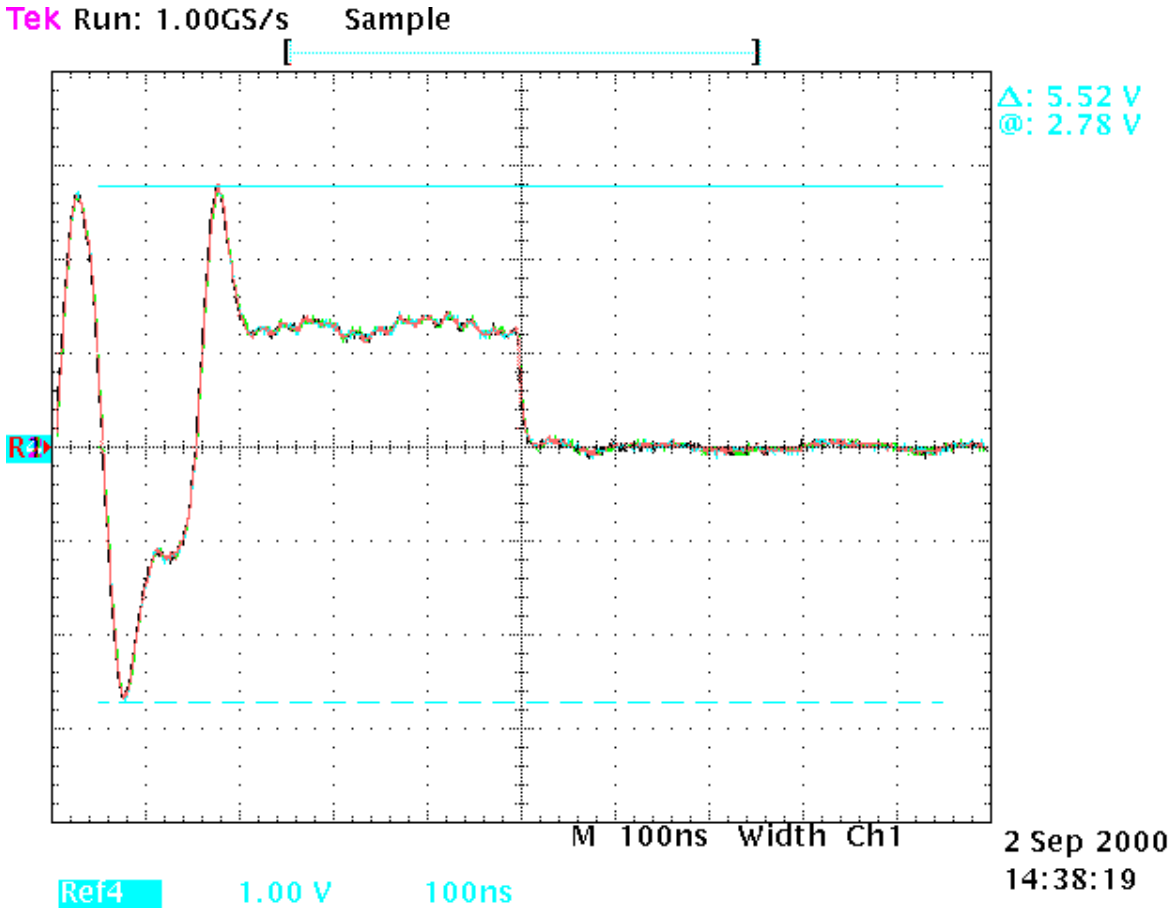
Bad PHY



10Mbit/s Signal, All three conditions

Signal Integrity - 10M

Bad PHY

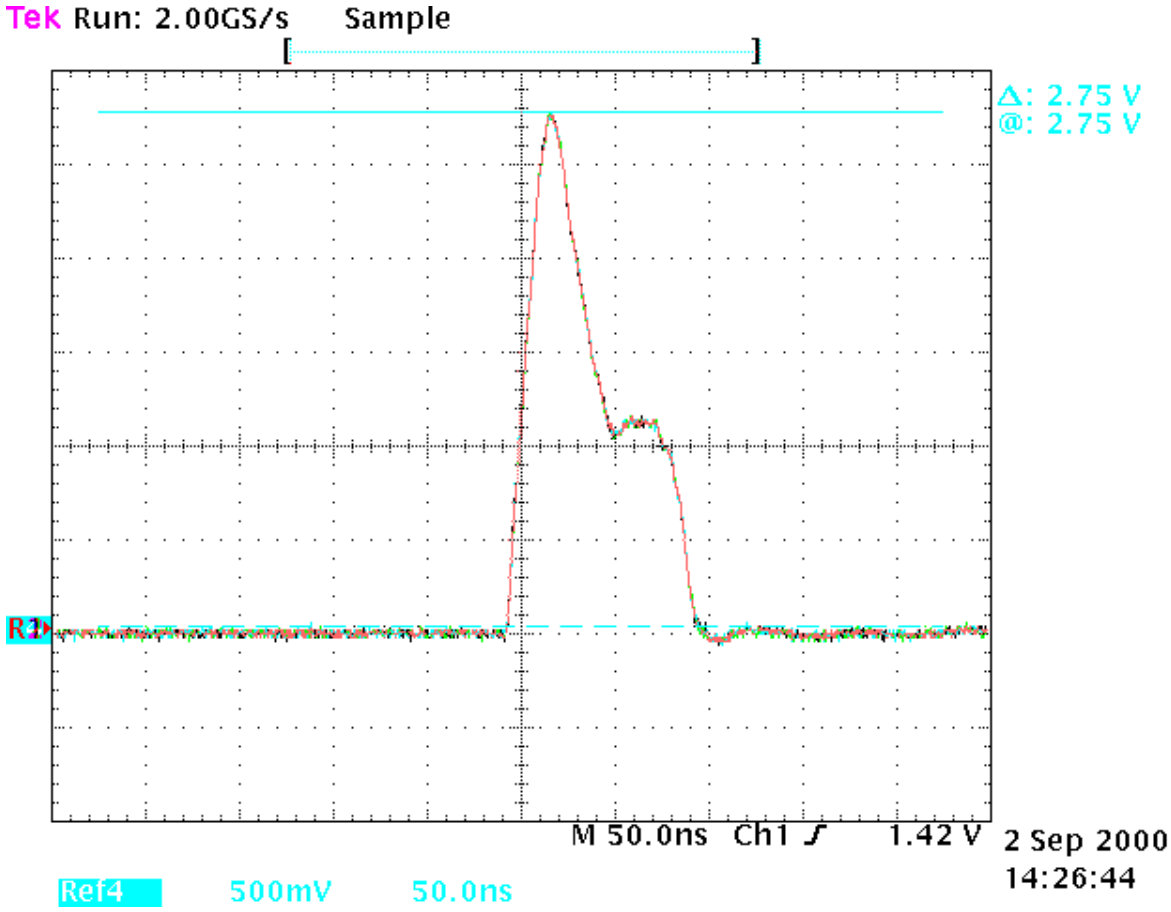


10 Mbit/s Start of TP_IDL, All three conditions

DTE power over MDI

Signal Integrity - 10M

Bad PHY



10 Mbit/s Link Pulse, All three conditions

Conclusions

- **The Diode Discovery Process does not degrade the performance of the MDI link.**
- **No degradation on the Signal pairs as it is not running at the same time as data. Therefore no effect!**
- **No degradation when run on the Idle pairs as shown in the previous data.**
- **As shown by Roger Karam at the last meeting the power supply will have to be filtered to eliminate degradation due to DC power transfer. This is true regardless of the wire pair used.**