IEEE 802.3af DTE Power via MDI
PSE-PD Inter-operate - Stability Analysis

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Objectives

- Specify the requirements to ensure PSE - PD stability at Normal Powering Mode

- Strategy

- Using Impedance Design Criteria
  - Specify PD input impedance without input filter
  - Specify PD input filter output impedance
  - Specify PSE power supply output impedance

System Description at Normal Powering Mode

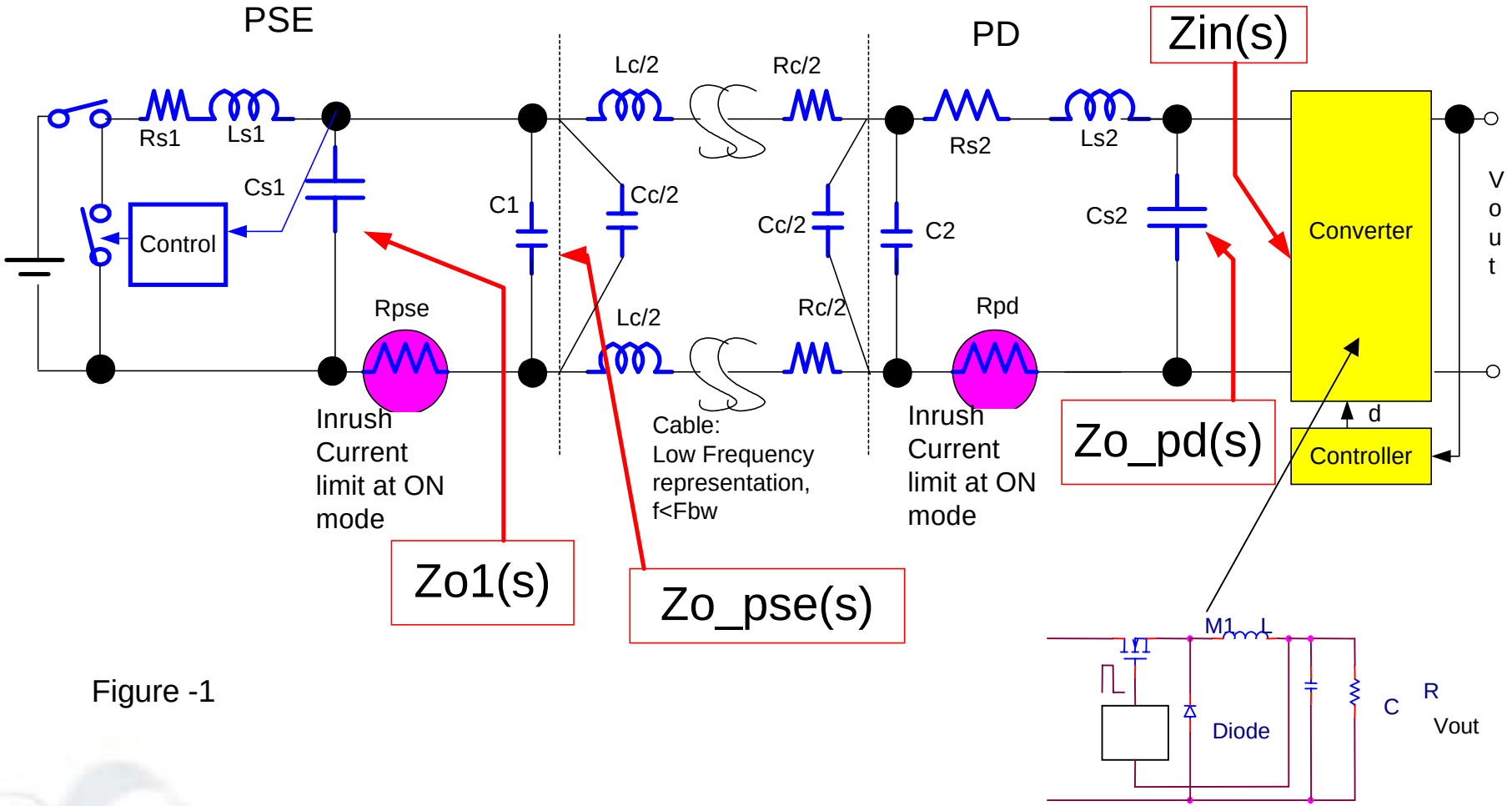
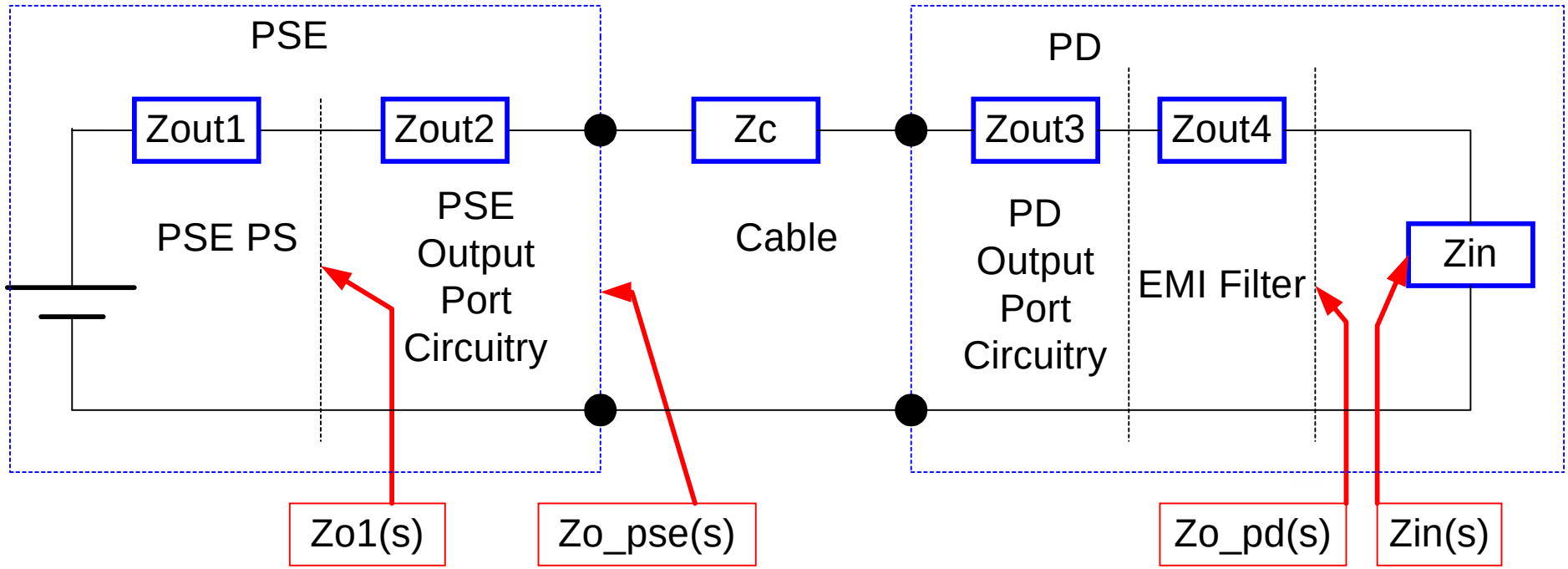


Figure -1

Simplified System at Normal Powering Mode



Problem Definition

- Under Specific Combinations of PSE output impedance and PD input Impedance
  - PSE - PD stability at Normal Powering Mode may be impaired
  - PD Power Supply Dynamic Performance will be changed

The reason:

- PD Power Supply Close Loop Transfer Function

  May be Impaired if Additional Frequency Dependent Elements are Connected From the Power Source (PSE) to the Load (PD's DC/DC converter)

List of Possible Stability Problems

- At specific frequency the source Output Impedance will increase to a level that PD input voltage will drop below UVLO level.
  - Startup Problems
  - Stability Problems during Load Changes
- Due to impairment of the PD PS Open Loop Transfer Function, marginal stability at small signal is expected

Proposed Strategy - Worst Case Analysis

Pros

- Shortest way to get results
- Solves PSE-PD inter-operate problem
- Simple design rules for PD and PSE

Cons

- Required large design margin compared to case when PSE-PD system is designed by the same vendor.

Worst Case Analysis Assumptions

- Cable length = 0 (Cable length =100m effects is discussed in (5))
  - Higher Quality Factor of the LC filters
- Inrush Current Limiter In PSE and PD is ON.
  - Series Switch Resistance =0 (Higher Quality Factor of the LC filters)
- PSE contains LC filter at its output
- PD contains LC filter at its input
- PD DC/DC converter control method is Voltage Mode
  - Current Mode Control is easier case(3,4)

Analysis Information

- Low frequency analysis , f<0.5Fs. Fs=Converter Switching Frequency.
  - Fs=100KHz was used as a typical case.
- Cable is modeled as low frequency device
- System is at Normal Powering Mode
  - PD converter short circuit condition at output is ignored.
- PD:Full Load = 12.95W average at its input
- Min Load = 10mA
- Typical results where simulated by the system model elements presented in July 2001. The control scheme was modified to voltage mode control.

Design Criteria

- To keep PSE-PD system stable, we need to keep PD stable at the following design options (See Figure 1 and Annex A):

- 1. PD with its EMI filter. Meeting |Zo_pd|<<|Zin| (See Annex A for Zin details)
  - Cable length=0, Rpse=0, Rpd=0
  - PSE source without output filter

- 2. PD with PSE PS output filter. |Zo_pse|<<|Zin|
  - Cable length=0, Rpse=0, Rpd=0, C1=0, C2=0.
  - PD converter without input filter

- 3. PD with PSE output filter and PD input filter. |Zo_pd|<<|Zin|
  - Cable length=0, Rpse=0, Rpd=0, C1=0, C2=0.

PSE Power Supply Output Impedance - Zo1

-Connected to resistive load (Min load= 10% of Full Load)

-Control method: Voltage Mode

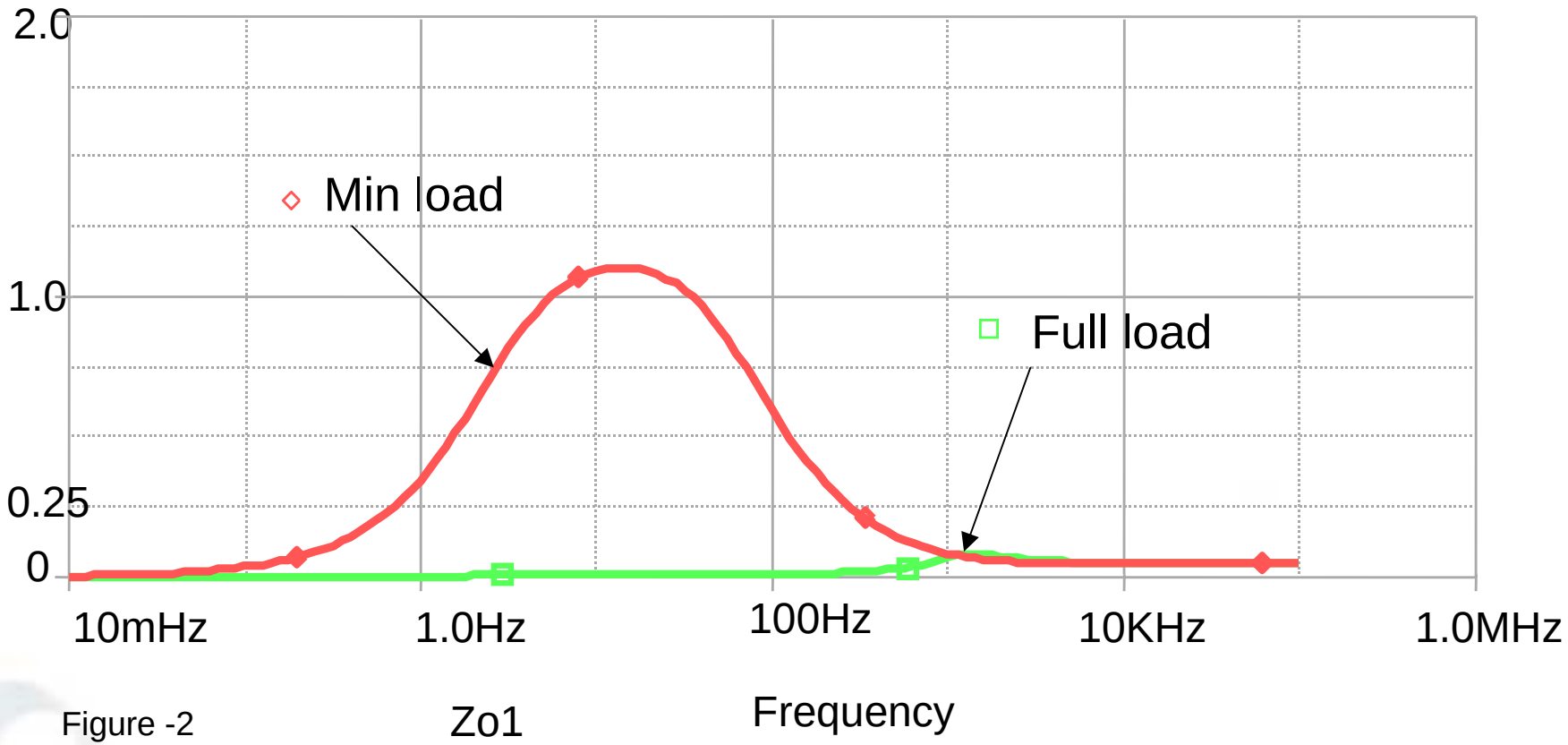


Figure -2

PD Converter Input Impedance - Zi(f) at full load (12.95W,37V)

- Without input filter effect
- With zero output impedance DC source.
- Control method: Voltage Mode,

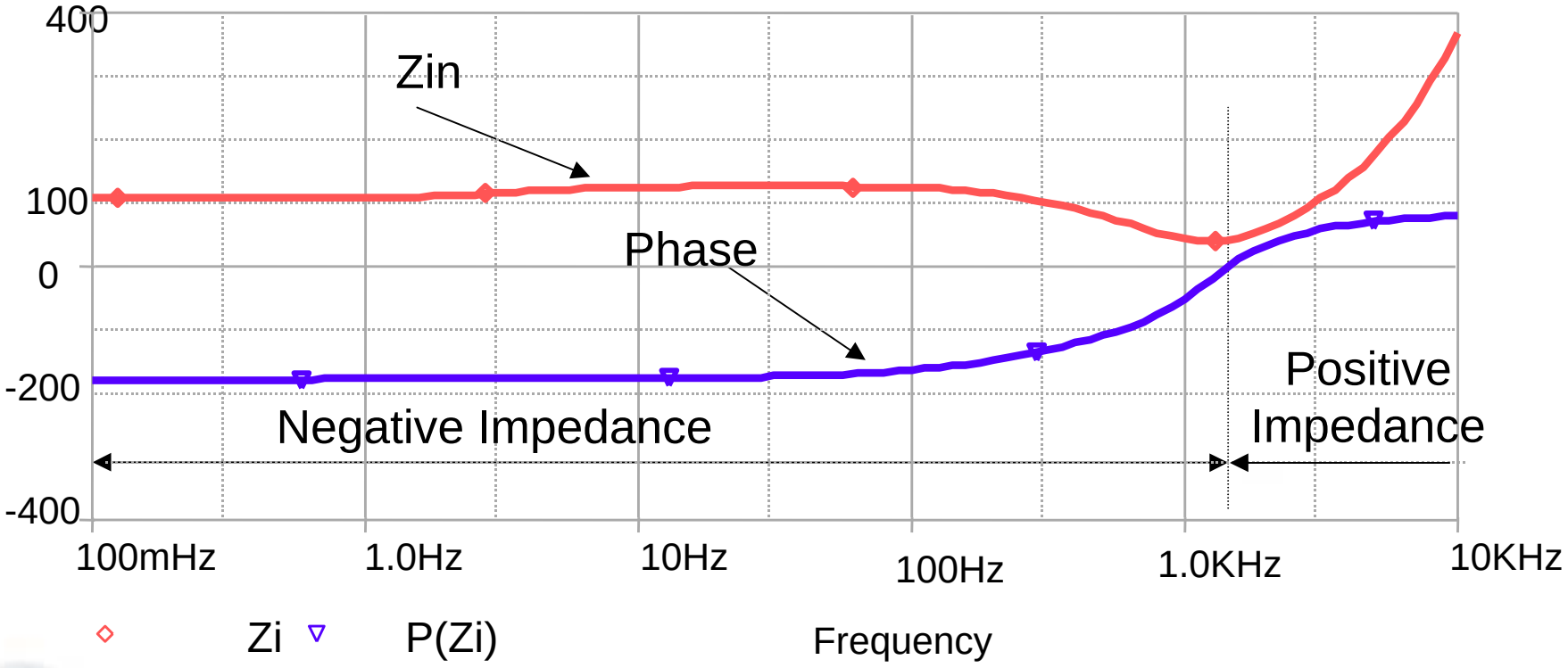
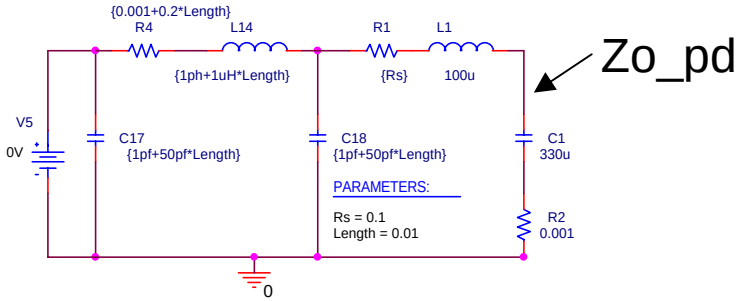
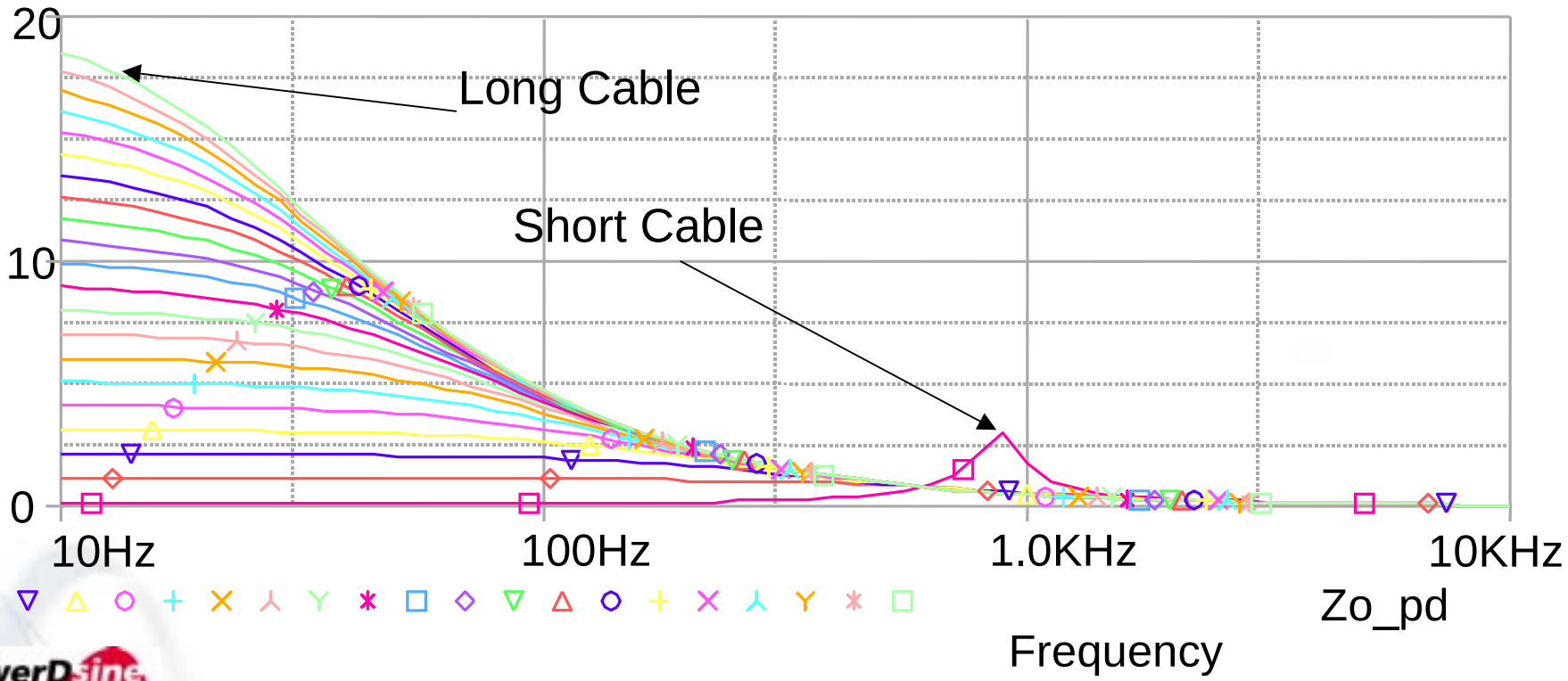


Figure -3

PD EMI Filter output impedance, Zo_pd vs. cable length.

EMI Filter: L=100uH, C=330uH, Rs=0.1 Ohm





PD DC/DC Converter Open Loop Transfer Function

- Without input filter effect

- With zero output impedance DC source.

- Control method: Voltage Mode

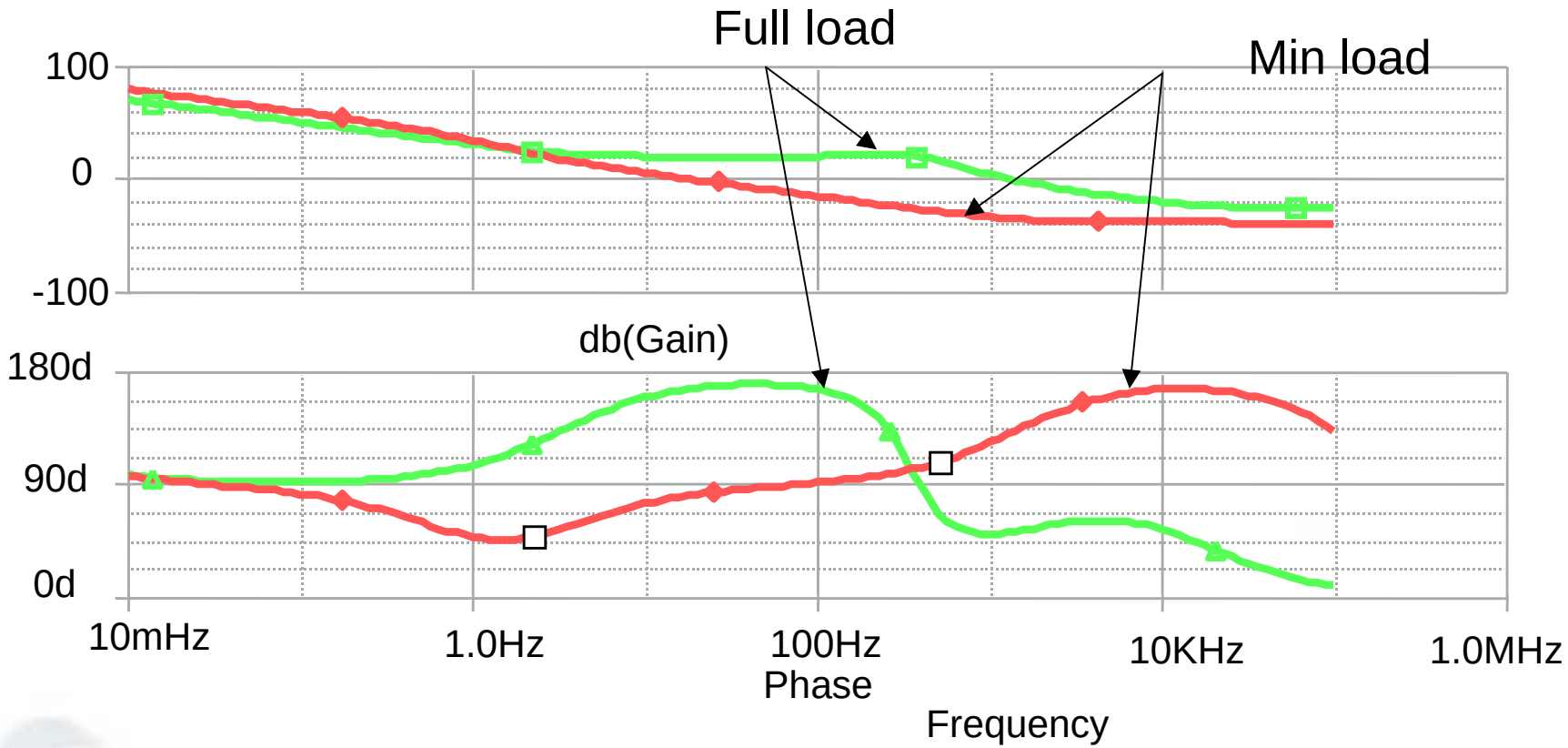
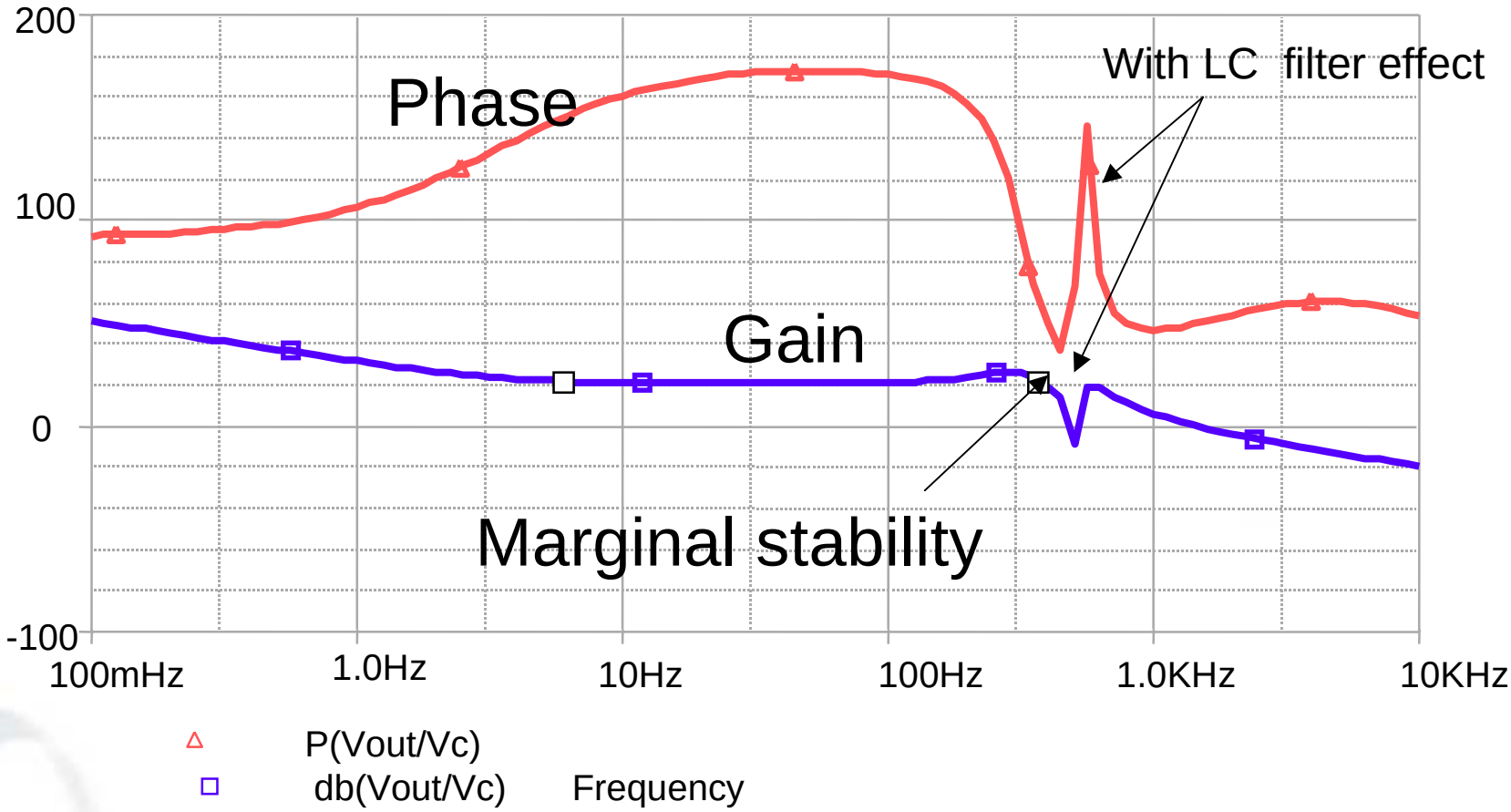


Figure -4

PD DC/DC Converter Open Loop Transfer Function

- With LC filter effect, Full load

- Control method: Voltage Mode



Impedance Allocation Map Measured from PSE PS to PD DC/DC converter input

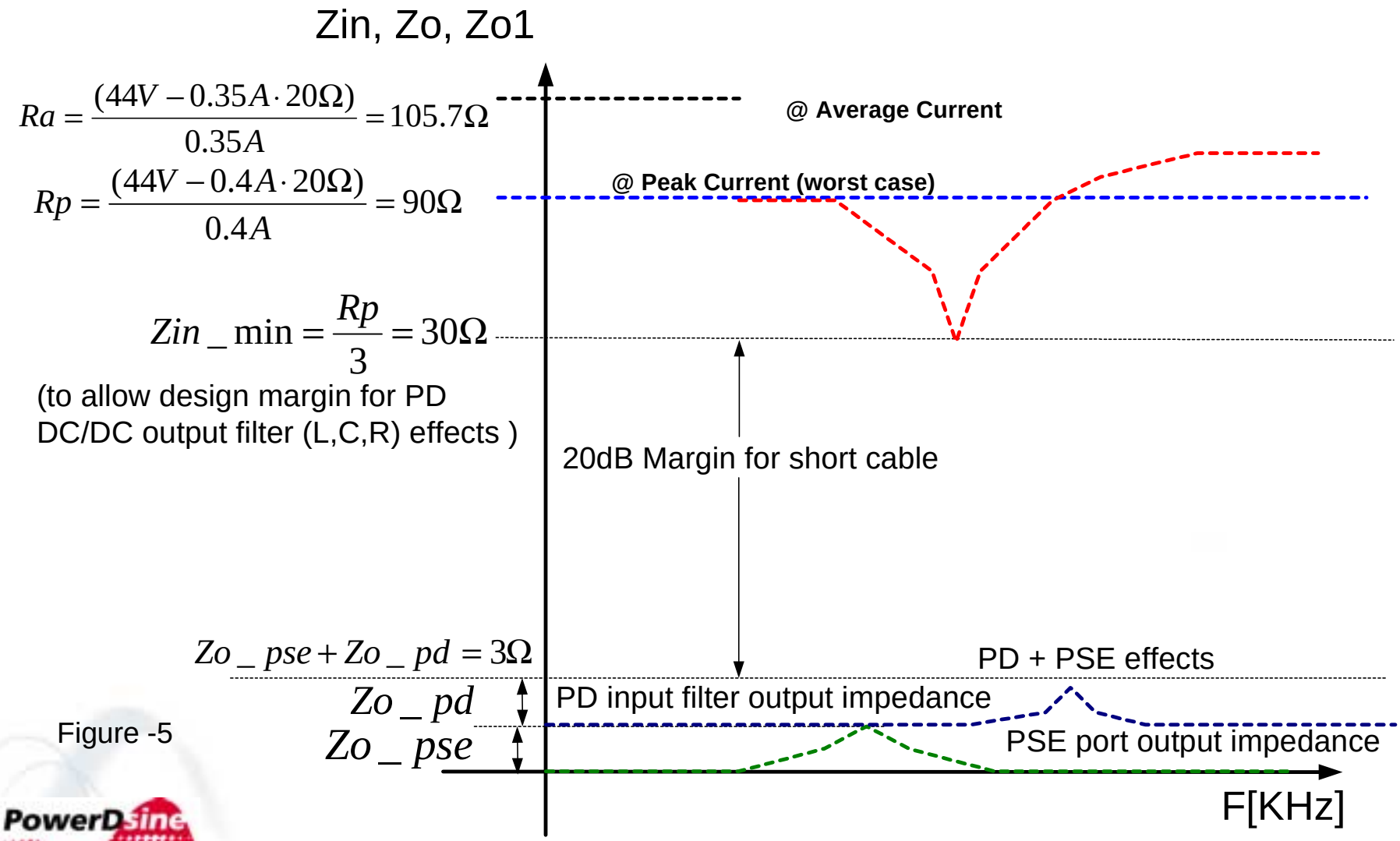


Figure -5

Impedance Allocation Map Measured from PSE Port to PD DC/DC converter input

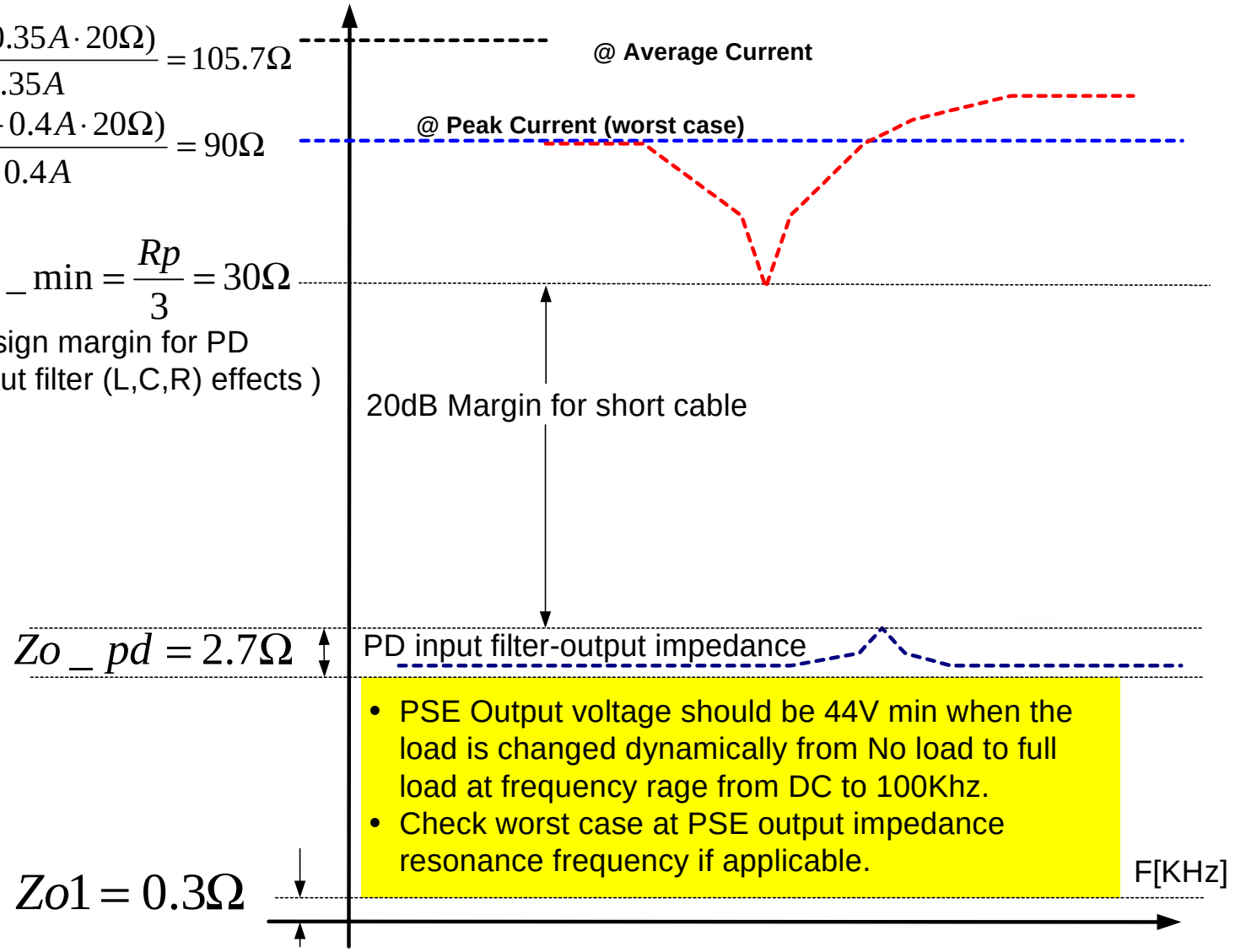
Zin, Zo, Zo1

$$Ra = \frac{(44V - 0.35A \cdot 20\Omega)}{0.35A} = 105.7\Omega$$

$$Rp = \frac{(44V - 0.4A \cdot 20\Omega)}{0.4A} = 90\Omega$$

$$Zin\_\min = \frac{Rp}{3} = 30\Omega$$

(to allow design margin for PD DC/DC output filter (L,C,R) effects)



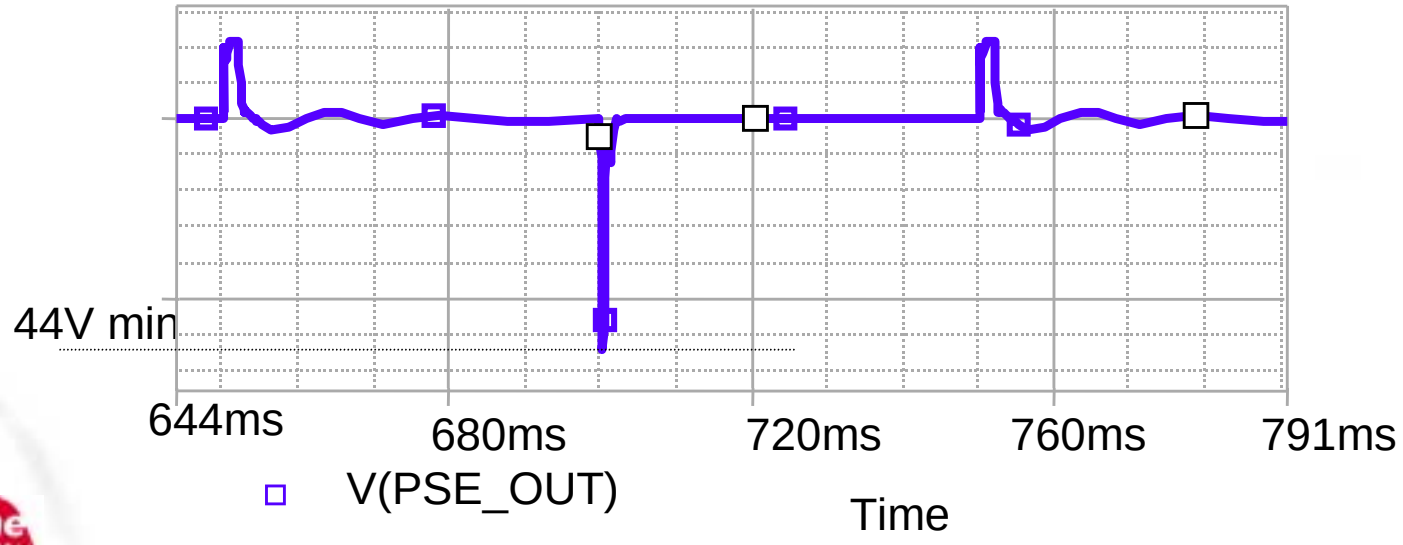
- PSE Output voltage should be 44V min when the load is changed dynamically from No load to full load at frequency rage from DC to 100Khz.
- Check worst case at PSE output impedance resonance frequency if applicable.

Proposed Requirements for PD

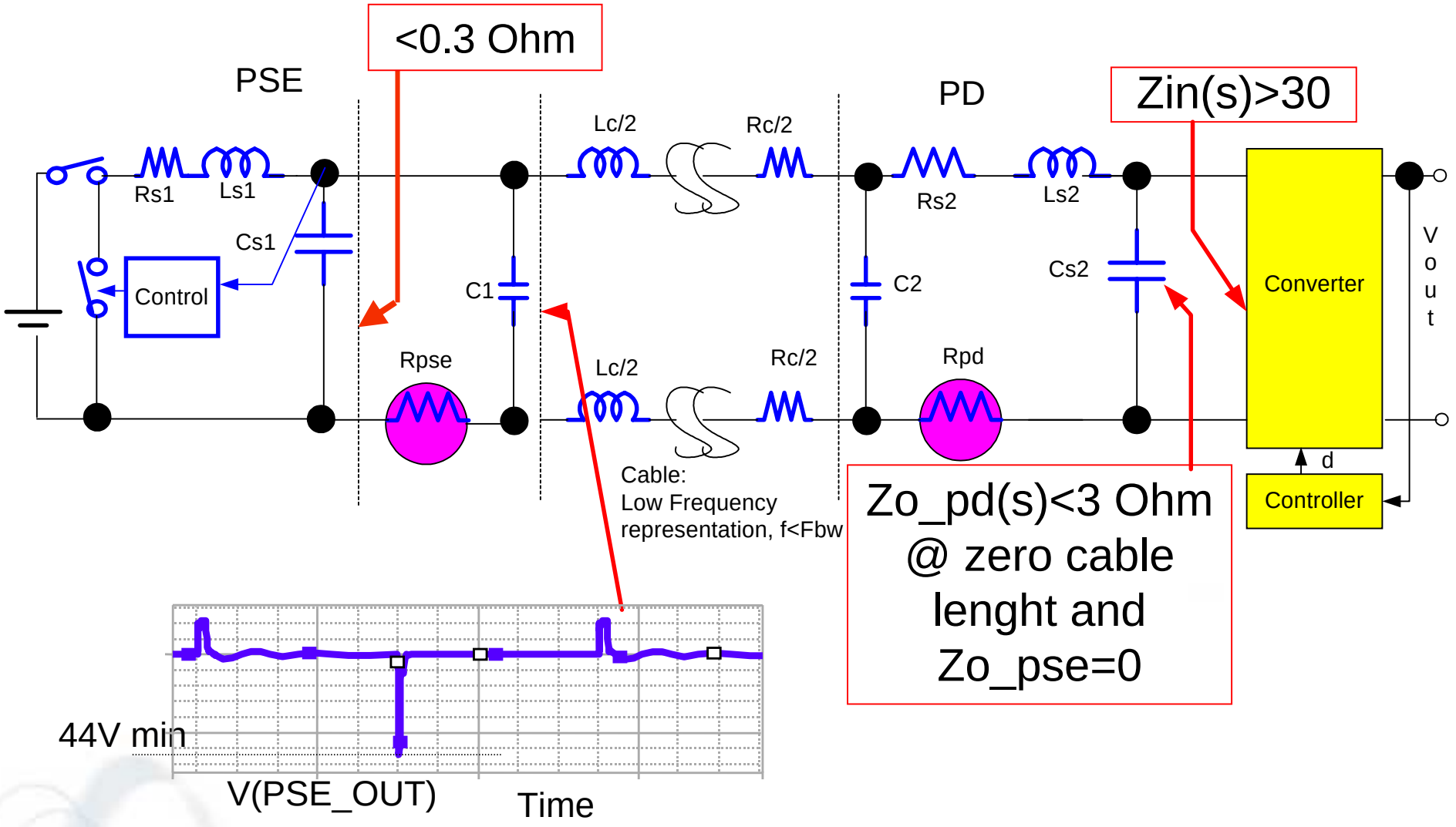
- PD converter input EMI filter or Cable inductance followed by capacitor
  - PD designer will ensure stable operation of its DC/DC converter in a presence of an input filter powered through short cable (<1m) and long cable (>100m).
  - Input filter cutoff frequency << Averaging LC filter cutoff frequency. (See Annex A)
  - The absolute value of the filter output impedance (Zo_pd) will not exceed 2.7Ω with short cable (<1m) for Pmax=12.95W assuming PSE output impedance <0.1Ω.
  - For Pmax< 12.95W, Zo_pd min will be Zo_pd= 2.7Ω*12.95/Pmax.
- PD converter input impedance (without input-filter output impedance effect), Zin
  - PD converter input impedance (Zin) will be 30Ω min at max. load condition, Pmax. (12.95W avg, 14.8W peak)
  - For loads Pmax< 12.95W, Zin_min will be Zin_min= 30Ω*12.95/Pmax.
- All the above requirements should be met well above Fbw.
- Fbw=DC/DC converter closed loop cross over frequency.

Proposed Requirements for PSE Output Port

- PSE PS output impedance (Zo1) shall be 0.3Ω max from DC to 100KHz at full load (Pmax=15.4W).
  - For Pmax<15.4W, Zo1= 0.3Ω*15.4/ Pmax
- PSE Port Output voltage should be 44V min when the load is changed dynamically from No Load to Full Load at frequency range from DC to 100KHz. (Compensating for Rpse)
- Check worst case at PSE output port impedance resonance frequency if applicable.



Proposed Requirements for PSE and PD - Summary



What's next?

Recommendations to IEEE802.3af group:

- PD and PSE requirements should be used as design guidelines.
- If easy test set-up is found to confirm the requirements at PORT level, it can be used as a requirement.
  - To be discussed with the group for the best option.

Annex A - Design Criteria

- Converter operating mode:
  - Continuous Current Conduction mode. Direct duty cycle control (voltage mode control).
- D= PWM controller duty cycle
- Doff = 1 – D
- R= Converter output load
- L= Converter Integrating Inductance
- C= Converter output capacitance
- Gvd(s)= DC/DC converter transfer function from output to control variable, d.
- $Z_N(s)=Zin(s)$ @ $\frac{d(Vout)}{dt}=0$
- $Z_D(s)=Zin(s)$ @ $\frac{d(D)}{dt}=0$
- Ze(s)=Zin(s) @ Converter output is shorted. (Not required to keep stability. It is required to keep converter output impedance unaffected by the presence of an input filter.)

Annex A - Design Criteria cont.

- Worst case analysis
  - Cable length = 0
  - Rpse=0
  - Rpd=0
- To keep PD converter control transfer function unaffected by the input filter and its associated circuits, the following inequalities should be met (2):

$$Gvd(s) = (Gvd(s)\big|Zo\_pd(s) \to 0) \cdot \left(\frac{1 + \frac{Zo\_pd(s)}{Zn(s)}}{1 + \frac{Zo\_pd(s)}{Zd(s)}} \right)$$

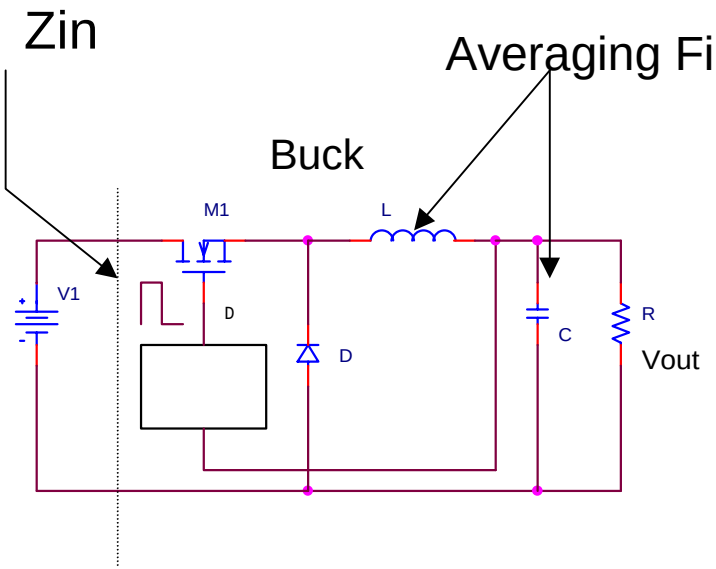
- Hence, the following inequalities should be met:
- $|Zo\_pd(s)| << |Z_N(s)|$
- $|Zo\_pd(s)| << |Z_D(s)|$

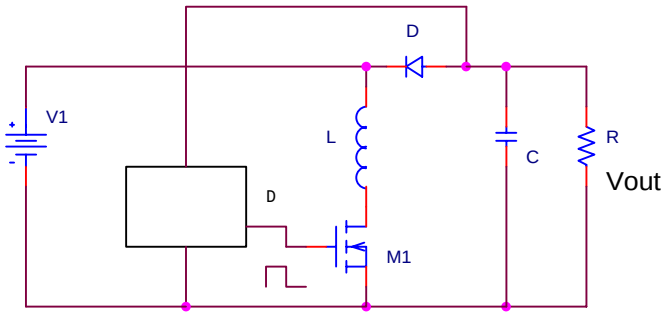
Annex A - Design Criteria cont.

Converter	$Z_N(s)$	$Z_D(s)$	$Z_E(s)$
Buck	$\frac{-R}{D^2}$	$\frac{R\left(1+s\frac{L}{R}+s^2LC\right)}{D^2(1+sRC)}$	$\frac{sL}{D^2}$
Boost	$-Doff^2\cdot R\left(1-s\frac{L}{Doff^2R}\right)$	$\frac{Doff^2R\left(1+s\frac{L}{Doff^2R}+\frac{s^2LC}{Doff^2}\right)}{(1+sRC)}$	sL
Buck-Boost (Flyback)	$-R\frac{Doff^2}{D^2}\left(1-s\frac{D\cdot L}{Doff^2R}\right)$	$\frac{Doff^2R\cdot\left(1+s\frac{L}{Doff^2R}+\frac{s^2LC}{Doff^2}\right)}{D^2(1+sRC)}$	$\frac{sL}{D^2}$

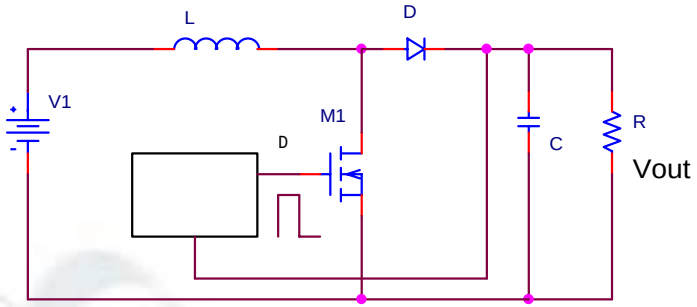
Analytical expressions for Zn, Zd, Ze.
Design Requirement: Plot Zn, Zd, Ze as function of frequency vs. Zo_pd and keep Zo_pd << Zn, Zd, Ze values.

Annex A - Design Criteria cont.





Boost



Buck-Boost (Flyback)

(Can be implemented with coupled inductor to have positive output)

Figure -7

References

- (1) R.D. Middlebrook, Slobodan C'uk , "Input filter considerations in design and application of switching regulator" Advances in Switched-Mode Power Conversion Volumes 1 and 2, Pp. 91-107.
- (2) Robert W. Erickson, Dragan Maksimovic', Fundamentals of Power Electronic 2nd edition pp 377-405, 843-861
- (3) Sandra Y. Erich and William M. Pollvka, "Input Filter Design for Current-Programmed Regulators" IEEE 1990.
- (4) Yungteak Jang and Robert W. Erickson. "Physical Origins of Input Filter Oscillations in Current Programmed Converters" 1991 IEEE Applied Power Electronics Conference.
- (5) Yair Darshan, "IEEE 802.3af Remote Powering Considerations" presented at May 2000 Interim.