CX4 Minimum Transmit Level

Vancouver, BC
Jan 7-8, 2003

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Agenda

- Criteria
- 1.2V Design Limitations
- Summary

What Should Be Criteria for Min Transmit Level?

- Meet CX4 Objectives
- Not exclude any existing XAUI designs
- This means:
  1. Transmit level no higher than XAUI (CX4 Objective)
  2. Compatible with existing and future process (CX4 Objective)
  3. Achievable with existing power supplies
  4. Low power

Let's look at each of the above a little closer

What Does "Transmit level no higher than XAUI" Mean to CX4 Min Transmit Level?

- XAUI requires that transmit level specs be met at *EITHER* near end or far end, but *NOT BOTH*
  - If near end is chosen, level = 800-1600 mV pp dif
  - If far end is chosen, level = 500-1600 mV pp dif
- Per above, if CX4 "transmit level no higher than XAUI", it will have to be spec'd at 500-1600 mV pp dif
  - Since CX4 cable attenuation is ~20db @ 1.5Ghz, a min xmt level of 500mV would result in ~50mv rcv level $\rightarrow$ Too low!
  - Might make sense to let min transmit level be dictated by the other constraints

What Does “Compatible with existing and future process” Mean to CX4 Min Transmit Level?

- Most current XAUI designs on 180 & 130nm process
- Newer XAUI designs on 90nm process
- Power supply voltage limits min transmit level

Process	VDD for core xstors
180nm	1.8V
130nm	1.2V
90nm	1.0-1.2V

cont'd

- Thick oxide transistors could be used instead of core transistors. However, some drawbacks:
  - Slower
  - More ISI
  - Larger area
  - Higher power dissipation
  - Needs higher supply than core transistors
    - Example: Can't use VDD=1.2V in 130nm, would need VDD=1.8
  - May require chips to have two supplies
    - 1.2V for logic
    - Additional higher supply for analog

cont'd

- Single supply very desirable
  - Multiple supplies are negative from system standpoint
  - Single supply XAUI designs already out @ VDD=1.2V
  - Single supply allows easier integration on larger ASIC's
- Lowest supply very desirable
  - Lowest power
  - Lowest area
- End Result:
  - Desireable for min transmit level that is achievable from a single power supply in range of VDD=1.2V-3.3V typ

What Does “Achievable with existing power supplies” Mean to CX4 Min Transmit Level?

- Existing XAUI designs have supplies in range of VDD=1.2V to 3.3V
- Some existing XAUI designs use single supply
- End Result:
  - Desireable for min transmit level that is achievable from a single power supply in range of VDD=1.2V-3.3V typ

What Does “Low power” Mean to CX4 Min Transmit Level?

- Low power important as XAUI gets integrated into digital chips and as systems/modules get smaller
- Low power = single, low voltage power supply
- Lowest supply voltage for current and future process is 1.2V
- End Result:
  - Desireable for min transmit level that is achievable from a single power supply in range of VDD=1.2V

Transmit Level Criteria Summary

- CX4 min transmit level should be spec'd to whatever is achievable with VDD=1.2V to 3.3V
- Since VDD=1.2V is worst case for min transmit level, let's see what is feasible with that supply

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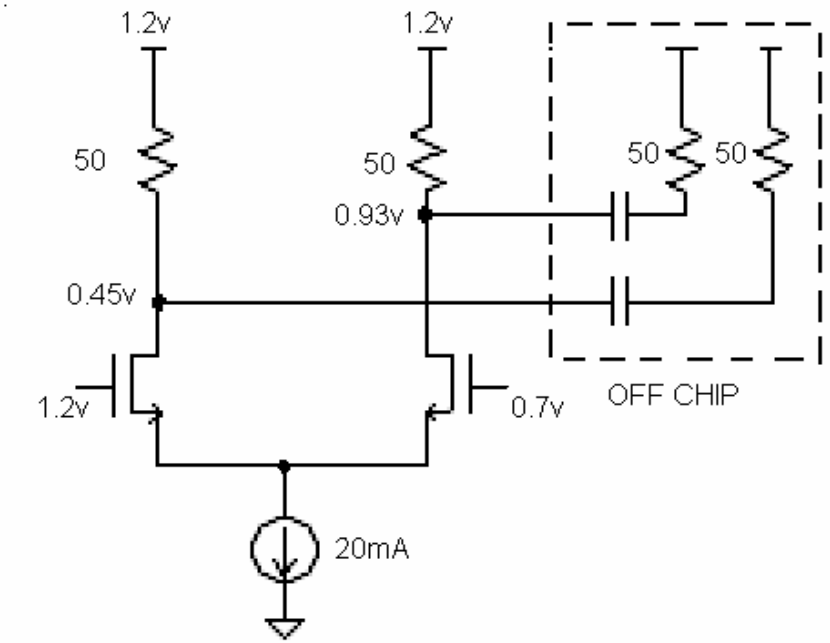
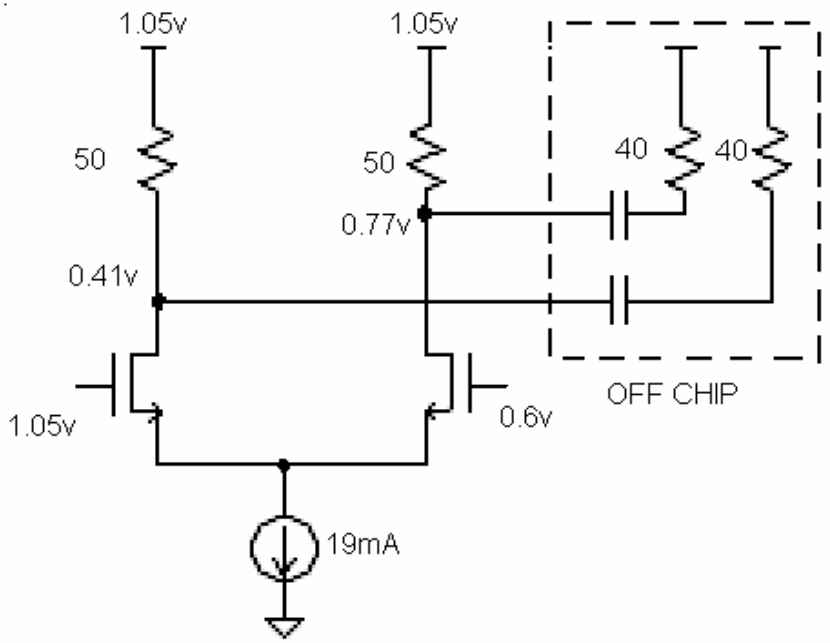
Typical VDD=1.2V Transmit Driver Circuit in 130nm Process



- Standard CML driver
- Because of AC coupling, DC drop is entirely across 50 ohms on chip.
- That pushes low level below ½ supply
- Still get DC xmt level = 960mV pp dif typical

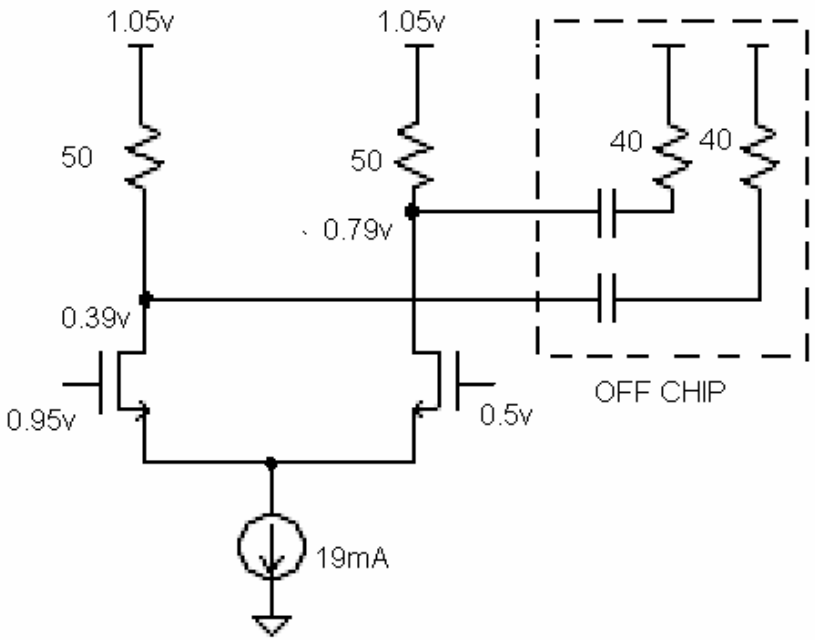
Look at Previous Circuit Under Worst Case Conditions



- Worst case conditions: VDD=1.05, 125C, fast process
- DC Transmit level now reduced to 720 mV pp dif
- Level limited by common source xstors being in triode

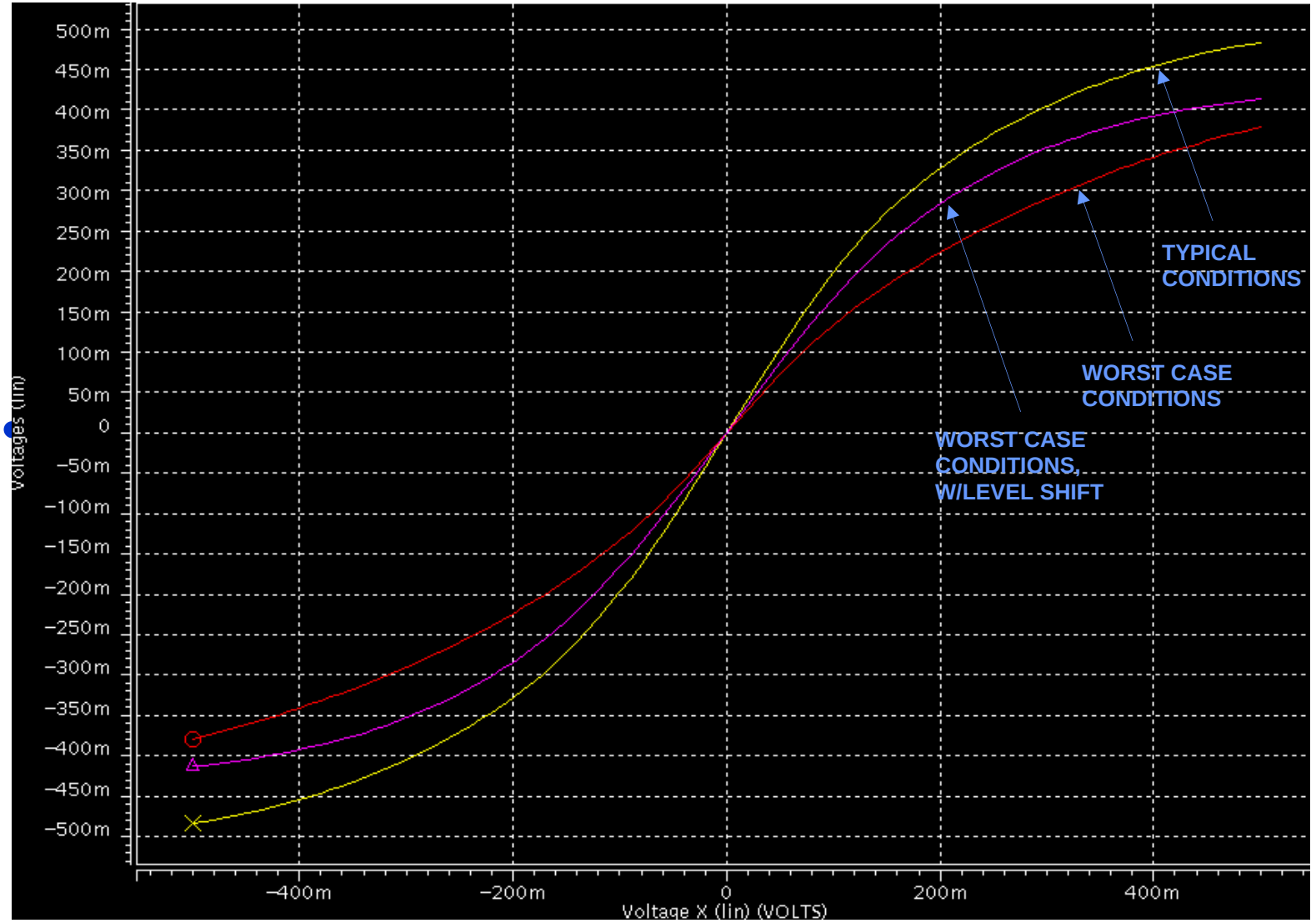
Could Improve Previous Case by Adding Level Shift

- Level shift input voltage from previous stage by 100mV



- DC transmit level improves to 800mV pp dif
- Puts burden on previous stage design, difficult but doable
- Above doesn't factor in worst case external termination resistor value (return loss spec allows ~50% R_{TERM} error)

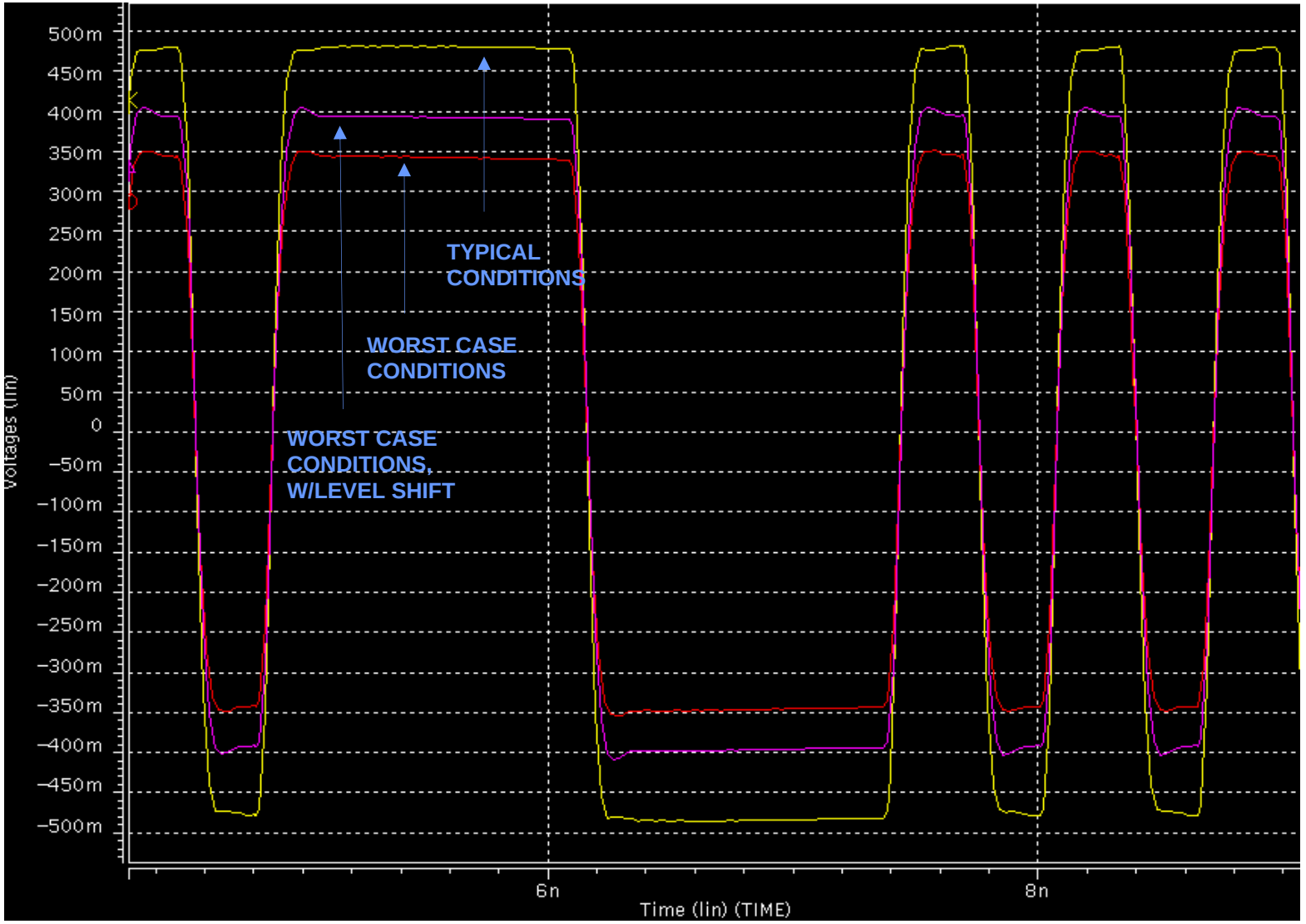
DC Simulation Results for Previous 3 Cases



What About AC Transmit Level?

- The previous slides only showed DC simulation results
- AC levels could be lower due to speed limitations in the circuits
- Let's look at AC level simulation results for previous 3 cases

AC Simulation Results for Previous 3 Cases



AC Simulation Results

- From previous page, AC min transmit level even lower than DC
  - Typ Conditions: 950 mV pp dif
  - Worst Case Conditions: 680 mV pp dif
  - Worst Case Conditions, w/Level Shift: 780 mV pp dif

What About Other Processes?

- Did same simulations in a 90nm process
- Got almost same results, level was ~10mV higher

Achievable Min Transmit Level @ VDD=1.2V

- Simulation Result Summary

Conditions	Min Transmit Level From Simulation (mV pp dif)	
	DC	AC
Typical Conditions	960	950
Worst Case Conditions	720	690
Worst Case Conditions, w/Level Shift	800	780

- Typical driver circuit can support 780mV pp dif min spec in 180nm, 90nm process

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CX4 Transmit Level Summary

- CX4 spec should allow single supply designs
- CX4 spec should allow VDD=1.2V designs
- To accommodate above:
  - Min transmit level spec $\rightarrow$ 750 mV pp dif
    - Min level dictated by process, power supply, low power constraints
  - Max transmit level spec $\rightarrow$ 1600 mV pp dif
    - Max level dictated by existing XAUI spec
- Results have been validated in both 180nm and 90nm process

Backup

Current XAUI Transmit Level Specs

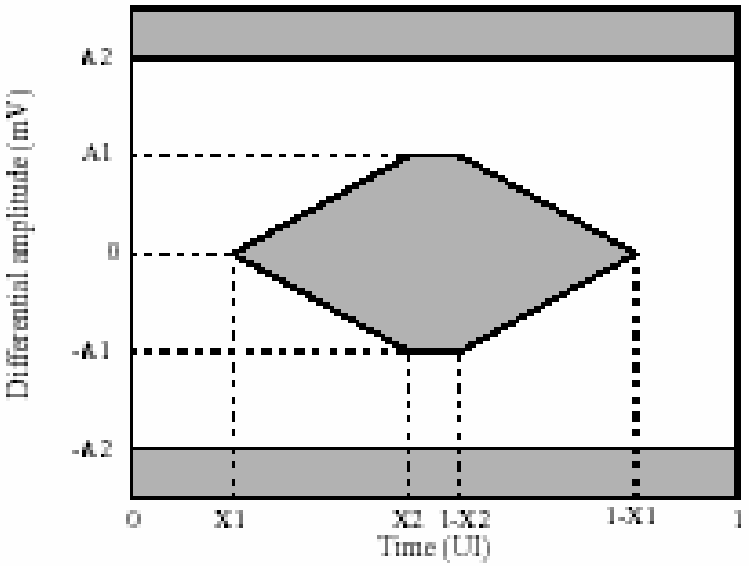

Figure 47–4—Driver template

Table 47–2—Driver template intervals

Symbol	Near-end value	Far-end value	Units
X1	0.175	0.275	UI
X2	0.390	0.400	UI
A1	400	100	mV
A2	800	800	mV