Cl **44** *SC* **1.2** *P* **7** *L* **33** # **324**

Grow, Robert Intel

Comment Type **TR** *Comment Status* **A** *TR058*

New retroactive requirement in item g) that is outside the scope of the 802.3ak PAR.

SuggestedRemedy

Either combine with item f) so Class A operation is limited to the CX4 objective, or move both items f) and g) to clause 54.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Resolved with comment #58

Cl **45** *SC* **2.1.7.6** *P* **11** *L* **21** # **331**

Grow, Robert Intel

Comment Type **TR** *Comment Status* **A** *TR001*

Incorrect reference to the bit number in the text.

SuggestedRemedy

Change ""1.8.4"" to 1.8.9"" two occurences.

Proposed Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

See comment #1

Cl **54** *SC* **1.1** *P* **16** *L* **31** # **287**

Frazier, Howard SW

Comment Type **TR** *Comment Status* **A** *TR287*

Since 54.1.1 through 54.1.4.3 are identical to 53.1.1 through 53.1.4.3, there is no point in reproducing them. Rather, you can simply refer to them. Saves pages, avoids confusion, less to maintain. (it's all informative, anyway)

SuggestedRemedy

Replace 54.4.1 through 54.1.4.3 with the following 54.4.1 Physical Medium Dependent (PMD) service interface The service interface provided by the 10GBASE-CX4 PMD is identical in all respects to the service interface provided by the 10GBASE-LX4 PMD, as described in 53.4.1.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #335

Cl **54** *SC* **10** *P* **39** *L* **40** # **124**

Jonathan Thatcher WWP

Comment Type **TR** *Comment Status* **A** *TR124*

The specific requirements for testing jitter are not clear. All we have is that it SHALL be performed with an unspecified test procedure that results in a BER bathtub curve such as that which is described in the Informative Annex 48B.

SuggestedRemedy

Highly recommend including a more complete jitter test methodology. One that you would be proud to put in the PICs.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

The jitter test method specified in 54.10.1 is consistent with the jitter test method specified in 47.4.3. Annex 48B, paragraph 1, will be changed to "... XAUI described in Clause 47, the 10GBASE-LX4 PMD described in Clause 53 and the 10GBASE-CX4 PMD described in Clause 54."

Cl **54** *SC* **4** *P* **18** *L* **36** # **290**

Frazier, Howard SW

Comment Type **TR** *Comment Status* **A** *TR290*

It seems needlessly complicated to specify the delay for the 10GBASE-CX4 PMD as including the delay associated with 1 meter of cable, and then making the user add in the delay for the other 13 meters of cable. For optical media, the complication is worth it, since the cable delay is such a large component of the end to end to delay, and can vary greatly since the cables can be either very short, or very looooooong. For CX4, we should simply account for the worst case cable delay in the PMD delay. Given the fact that the worst possible delay associated with a CX4 link will be very small compared to the worst case delay associated with an optical link, this change should make absolutely no difference to system implementers, but it should make a user's life a little easier.

SuggestedRemedy

On line 44, change 1 meter of cable to 15 meters of cable. Also change 512 to 1024 BT, or 2 pause quanta. Table 44-2 should be changed accordingly. If the committee thinks they should allow for more delay and specify 1536, or even 2048 BT, I would have no objection whatsoever. It's all tiny compared to fiber.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

All PHYs have this delay specified at the MDI, see 31B.3.7. In the case of 10Gbps fiber PHYS the MDI is at the end of 1m of fiber.

Will remove the words "(including 1m of cable)". Also Table 44-2 CX4-PMD note to be changed to "See 54.4".

Cl **54** *SC* **6.4** *P* **21** *L* **17** # **116**

Jonathan Thatcher WWP

Comment Type **TR** *Comment Status* **R** *TR116*

Technically speaking, if a 101010... pattern exists "on the wire," there won't be a 1 UI interval where the MDI has exceeded 175 mVppd (that would require infinite rise/fall times, which is won't meet spec).

SuggestedRemedy

It might be better to specify SD using energy (e.g. AC power). This would decouple (no pur intended) this specification from the DC blocking CAP and its inherent impact (e.g. filter time) on the detection times. This can be done without specifying the implementation.

Proposed Response *Response Status* **U**

REJECT.

An indefinate 101010... pattern cannot exist on the wire. The minimum IPG contains sufficient low frequency content to cause SIGNAL_DETECT to be asserted. As long as a minimum IPG is received at an interval that is less than or equal to the minimum SIGNAL_DETECT deassertion time SIGNAL_DETECT will remain asserted.

Will add "absolute differential voltage" to clarify.

Cl **54** *SC* **6.4** *P* **21** *L* **24** # **357**

Grow, Robert Intel

Comment Type **TR** *Comment Status* **A** *TR357*

The sentence doesn't properly describe that 500us is the maximum time for assertion of SIGNAL_DETECT.

SuggestedRemedy

Change to read: ""... has dropped below and remained below 50mVppd within 500us.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Change text to "The PMD shall have asserted SIGNAL_DETECT ...."

Cl **54** *SC* **6.4** *P* **21** *L* **43** # **295**

Frazier, Howard SW

Comment Type **TR** *Comment Status* **A** *TR295*

Why does the specification assume that the signal detect assertion time (or any signal detect response time) is measured using MDIO/MDC? There is no need to assume this if the signal can be directly measured with a 'scope. The fact that there is no electrical spec for signal detect makes the timing parameters meaningless, and there is no way to bound the sampling time or response time at the MDIO/MDC. If you want to put timing parameters in for signal detect, you should add in the essential components of an electrical spec.

SuggestedRemedy

Remove the note at line 43, and set the assertion time at whatever you feel is both technically and economically feasible, assuming that the parameter can be measured by directly observing the signals with a 'scope, and that things like the rise/fall times of the signals are tiny in comparison to the measurement interval. To get around the need for an electrical spec, you could state that ""The signal detect assertion and deassertion times are measured at the logic thresholds indentified in the PMD manufacturer's specification."" This would permit a wide range of implementations, tighten up the times, circumvent the need for an electrical spec, and avoid the ambiguity and complexity associated with sampling the intervals via MDIO/MDC.

Proposed Response *Response Status* **U**

ACCEPT.

Note removed. All other suggested remedy criteria met.

Cl **54** *SC* **6.7** *P* **22** *L* **12** # **341**

Grow, Robert Intel

Comment Type **TR** *Comment Status* **A** *TR341*

The term ""absolute output voltage limits"" is not defined in Table 54-6.

SuggestedRemedy

Change to read ""... and does not exceed the maximum differential peak amplitude in Table 54-6."" Fix similar problem on line 24.

Proposed Response *Response Status* **U**

ACCEPT.

Cl **54** *SC* **7** *P* **23** *L* **11** # **388**

Brown, Kevin — Broadcom Corp

Comment Type **TR** *Comment Status* **A** *TR388*

The complete link budget of: transmiter level (54.7.3.4), return loss (54.7.3.5), template (54.7.3.6), jitter (54.7.3.8), cable assembly insertion loss (54.8.2), return loss (54.8.3), NEXT (54.8.4), FEXT (54.8.5), Receiver amplitude (54.7.4.4), return loss (54.7.4.5), jitter tollerance (54.7.4.6) when taken all together produces a non working link. The amount of allowable noise in the system from return losses, NEXT, FEXT and jitter is higher than what is required to obtain error free opperation, for a BER of 10^-12, with the given insertion loss, transmit level, transmit template and a reasonable simple receiver equalization (at the minimum ould need next & fext cancilation).

SuggestedRemedy

A presentation is to be given by Howard Baumer for a suggested link budget at the May interim in Portsmouth, NH.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Based upon presentations given in Portsmouth, N.H. that address this comment, the following changes will be made:

1) Clause 54.8.3 change equuations 54.4a, 54.4b, 54.4c to:
Return Loss(f) >= 22.35 - 17.17 x log10(f/100) for 100MHz < f <= 400MHz
Return Loss(f) >= 12 for 400MHz < f <= 2000Mz

2) Clause 54.7.3.4 change the first sentence in the first paragraph to: 'Driver differential output amplitude shall be less than 1200 mVp-p."

3) Clause 54.7.3.4 after the third sentence of the first paragraph add the following sentenc
The difference between any two lanes' differential peak-to-peak output amplitude shall be less than or equal to 150mVpp.
differential peak-to-peak output amplitude difference will be added to Table 54-6.

4) Clause 54.8.4.2 change equation 54.6 to:
MDNext(f) >= 27 - 17 x log10(f/2000)

5) Change the transmit template and table to the one presented in Ottawa by Dimitry Taich, dt_ottawa.pdf. Change the 54.7.3.1 item 6 to "... Normalized Waveform = (Original Waveform - Voff) * (0.69 / Vnorm).".

6) All related figures, tables and other references will be updated accordingly.

Cl **54** *SC* **7.3.2** *P* **25** *L* **24** # **469**

Bill Quackenbush — Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **A** *TR469*

Impedance is a complex quantity (R+jX). I infer that the specification of the impedance as 50 Ohms really means 50+j0 Ohms (50 Ohms resistive). What is unclear to me is how the specified tolerance of +/- 0.5% is to be applied a complex quantity. For instance, is the tolerance applied individually to the resistive and reactive components of the specified impedance resulting in a permitted impedance range of 49.5+j0 to 50.5+j0 Ohms? If so, this is a specification that no physical resistor can meet over the specified frequency range due to parasitic inductance and capacitance. I suspect that some other meaning was intended, but such meaning is not evident in the text. In particular, I suspect that the intent was to specify an impedance whose resistive component is 50 Ohms +/- 1% and whose reactive component is assumed to be small and is ignored.

SuggestedRemedy

Change the specification to an "impedance whose resistive component is 50 Ohms +/- 1%". If the reactive component is of concern, then a more complex specification is required.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Change Clause 54.7.3.2 to:
"The nominal differential impedance of the transmit test fixture depicted in Figure 54-3 shall be 100 ohms with a return loss greater than 20dB from 100MHz to 2.0GHz."

Cl **54** *SC* **7.3.2** *P* **25** *L* **24-24** # **467**

Bill Quackenbush — Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **A** *TR467*

The specification is not clear and does no agree with Figure 54-3 which shows no clear connection to the signal shield. The impedance being specified is not clearly stated.

SuggestedRemedy

Change the text to something like "The test fixture shall terminate each signal of a differential pair with an impedance of 50 Ohms +/- 1% to the signal shield. The impedance specification shall be met over the frequency range of 100 MHz to 2.0 GHz."

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Will revise figure 54-3 to improve clarity.
Will expand figure so signal lines are not so crowded.

Proposed text change is adddresed in response to comment #469

Cl **54** *SC* **7.3.6** *P* **27-28** *L* **23-50 on 2** # **464**

Naresh Raman Independent

Comment Type **TR** *Comment Status* **A** *TR487*

There were simulation results presented at the MARCH Plenary that showed that some changes had to be made to the template in the draft. The presentations were CX4_Mar03_Mysticom.ppt and cx4_tx_template_update_03_10_03.pdf

SuggestedRemedy

Replace Fig. 54-6 and Table 54-7 with the figure and Table in the attached document.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #487

Cl **54** *SC* **7.3.8** *P* **28** *L* **51-53** # **465**

Naresh Raman Independent

Comment Type **TR** *Comment Status* **A** *TR465*

The total jitter for XAUI and CX4 are the same. The DJ limit is also the same but the RJ limits have been specified differently in the CX4 Standard. There has been no presentation made to the Study group to warrant this change. The study group has only changed the limits from XAUI if there was a technical requirement. If there is no clear justification for this change to the RJ limit then it should also be the same as the XAUI limits.

SuggestedRemedy

Change text under 54.7.3.8 to The transmitter shall satisfy the jitter requirements with a maximum total jitter of ± 0.175 UI peak from the mean and a maximum deterministic component of ± 0.085 UI peak from the mean. Note that these values assume symmetrical jitter distributions about the mean. If a distribution is not symmetrical, its peak to peak total jitter value must be less than these total jitter values to claim compliance. Jitter specifications include all but 10E-12 of the jitter population. The maximum random jitter is equal to the maximum total jitter minus the actual deterministic jitter. Jitter measurement requirements are described in 54.10.1.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Change Clause 54.7.3.8. To '... and a maximum random component of ± 0.135 UI peak"

Cl **54** *SC* **7.3.8** *P* **28** *L* **54** # **461**

van Doorn, Schelto Intel

Comment Type **TR** *Comment Status* **A** *TR465*

Because new technologies use lower voltage levels, the random jitter is expected to increase due to a lower signal to noise ratio. Putting a cap on the RJ this low might hinder future technologies. Our objectives state to use the XAUI ""as is"" and adding the RJ cap is not needed and contradicts to the objective. No presentation has been made to prove that the original XAUI will not work.

SuggestedRemedy

Remove the RJ cap to be compliant with in XAUI or justify and a max value that we can live with.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #465

Cl **54** *SC* **7.3.8** *P* **29** *L* **4** # **298**

Frazier, Howard SW

Comment Type **TR** *Comment Status* **A** *TR298*

The editor's note at the top of the page is inappropriate for inclusion in a WG ballot draft, especially since the March, 2003 plenary was history at the time the ballot was launched.

SuggestedRemedy

Remove the note prior to offering the draft for sale. If the transmit jitter allocation is still subject to analysis, then it was inappropriate to launch a WG ballot on this draft, and the ballot should be halted and voided.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Note is a typo and was indaverdently left in. It will be removed.

Cl **54** *SC* **7.3.8** *P* **29** *L* **4** # **458**

Thaler, Pat Agilent Technologies

Comment Type **TR** *Comment Status* **A** *TR298*

The note seems to indicate some uncertainty in the correctness of the current transmit jitter spec (which seems to be drawn directly from the XAUI jitter spec). Also, receiver jitter is inadequately specified (see my other comment on the subject). Therefore, it is not clear that jitter allocation is sufficiently understood.

SuggestedRemedy

Establish a jitter budget allocation and correct transmit jitter to correspond to that.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #298

Cl **54** *SC* **7.3.8** *P* **29** *L* **4-5** # **463**

Don Alderrou Intel Corporation

Comment Type **TR** *Comment Status* **A** *TR465*

The Jitter budget for CX4 is critical. Any difference from the XAUIbudget may cause interoperability issues. I can't vote to Approve thisdraft with an Editor's note stating that the jitter budget will bereconsidered.

SuggestedRemedy

Specify the XAUI jitter budget for CX4 and remove the Editor's note.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #465

Cl **54** *SC* **7.4** *P* **29** *L* **24** # **119**

Jonathan Thatcher WWP

Comment Type **TR** *Comment Status* **A** *TR119*

It seems absolutely unreasonable to define the minimum input amplitude based on a non-existent and unspecified golden transmitter, a non-existent worst case cable assembly, etc Related text in 54.7.4.4 on page 30, line 6.

SuggestedRemedy

Spec it.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

The following text will be deleted from the first paragraph of Clause 54.7.4.4:

"The minimum input amplitude is defined by the transmit driver, the channel and the actual receiver input impedance. Note that the transmit driver is defined using a well controlled load impedance. The minimum signal amplitude into an actual receiver may vary from the minimum height due to the actual receiver input impedance."

Cl **54** *SC* **7.4.4** *P* **30** *L* **3** # **113**

Gaither, Justin Xilinx, Inc

Comment Type **TR** *Comment Status* **A** *TR113*

Input sensitivity is not properly specified. This would require me to qualify my part against every other vendor out their through maximum cable length in order to verify compliance.

SuggestedRemedy

Please specify the worst case output amplitude against the worst possible mismatch case of output transmitter impedance, cable and input impedance.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Input sensitivity for a system that uses receive side equalization is an inappropriate parameter.

Cl **54** *SC* **7.4.6** *P* **31** *L* **30** # **457**

Thaler, Pat Agilent Technologies

Comment Type **TR** *Comment Status* **A** *TR457*

This appears to leave determination of the required receiver jitter tolerance as an exercise for the implementor. This is complicated to determine and should be specified by the standard.

SuggestedRemedy

Specify the quantity of jitter that the receiver must tolerate.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #374

Cl **54** *SC* **7.4.6** *P* **31** *L* **33-34 and** # **477**

Bill Quackenbush Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **A** *TR457*

The specification of the allowable sinusoidal jitter component is unclear. There is no indication whether the allowable sinusoidal component must be above or below the line on Figure 54-8.

SuggestedRemedy

Shade the portion of Figure 54-8 above the upper bound line or label the line with "upper bound". Change the sentence beginning on line 33 to "The receiver shall tolerate an additional sinusoidal jitter with any combination of frequency and amplitude in the unshaded portion of Figure 54-8."

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #457

Cl **54** *SC* **8** *P* **32** *L* **17** # **120**

Jonathan Thatcher WWP

Comment Type **TR** *Comment Status* **A** *TR386*

It seems completely unreasonable to define cross talk characteristics on a limited rise / fall time signal and have a zero random jitter component.

SuggestedRemedy

Yes, this is hard. But it is reasonable to have specifications for the RJ contribution for PCB, Cable, and "Other."

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #386, Informative table has been removed

Cl **54** *SC* **8.1** *P* **32** *L* **54** # **484**

Bill Quackenbush Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **R** *TR484*

Impedance is a complex quantity (R+jX). I infer that specification of the impedance as 100 Ohms really means 100+j0 Ohms (100 Ohms resistive). What is unclear to me is how the specified tolerance of +/- 10% is to be applied a complex quantity. For instance, is the tolerance applied individually to the resistive and reactive components of the specified impedance resulting in a permitted impedance range of 90+j0 to 110+j0 Ohms? If so, this is a specification that no lossy transmission line can meet over the specified frequency range due to its losses. I suspect that some other meaning was intended, but such meaning is not evident in the text. In particular, I suspect that the intent was to specify an impedance whose resistive component is 100 Ohms +/- 10% and whose reactive component is assumed to be small and is ignored.

SuggestedRemedy

Change the specification to an "impedance whose resistive component is 100 Ohms +/- 10%". If the reactive component is of concern, then a more complex specification is required. CommentEnd SuggestedRemedy

Proposed Response *Response Status* **U**

REJECT.

The specification is defining "Characteristic" impedance for a differential transmission line which is defined nominally as sqrt(L/C) and therefore the suggested remedy is inappropriate.

Cl **54** *SC* **8.2** *P* **33** *L* **10-11** # **481**

Bill Quackenbush Cisco Systems, Inc.

Comment Type **TR** *Comment Status* **A** *TR432*

The measurement points for the cable assembly insertion loss are not clearly stated. Reference to a diagram or figure would be useful such as Figure 54-2. Are TP1 and TP4 o Figure 54-2 the correct measurement points for this measurement?

SuggestedRemedy

Clarify the measurement points for the cable assembly insertion loss.

Proposed Response *Response Status* **U**

ACCEPT.

See comment #432

Cl **54** *SC* **8.6** *P* **38** *L* **30** # **299**

Frazier, Howard SW

Comment Type **TR** *Comment Status* **A** *TR299*

I don't see a specification for shield transfer impedance within Clause 54. Is shield transfe impedance for an end to end link specified in the referenced documents?

SuggestedRemedy

Specify shield transfer impedance. If it is not adequately specified in the referenced documents for the cable and the connectors, consider adopting material like that found in 22.6.2, which describes Shielding effectiveness and transfer impedance for the MII.

Proposed Response *Response Status* **U**

ACCEPT.

Shield transfer impedance is specified in the referenced documents.

Cl **54** *SC* **Figure 54-6** *P* **27** *L* **24** # **346**

Grow, Robert Intel

Comment Type **TR** *Comment Status* **A** *TR487*

The agreement of the Task Force was to review and adjust the transmit template with the results of simulations, yet that hasn't been done.

SuggestedRemedy

Replace Figure 54-6 and Table 54-7 with a template representative of simulation results. Steve Dreyer has submitted replacements that I believe accurately reflect simulation results.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #487

Cl **54** *SC* **Table 54-9** *P* **32** *L* **23** # **291**

Frazier, Howard SW

Comment Type **TR** *Comment Status* **A** *TR386*

in note b to Table 54-9: 5.08cm of FR4? Does the 0.08 cm make a difference? I can barely see 0.08 cm of PCB, let alone measure it.

SuggestedRemedy

Please round it off to 5 cm of FR4.

Proposed Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See comment #386, Informative table has been removed