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Proposal for Transmitter Electrical Specifications

IEEE P803.2an Task Force

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Objectives

- **Establish Transmitter Electrical Specifications**
  - **Peak differential output voltage (paragraph 55.5.3.1)**
  - **Maximum output droop (paragraph 55.5.3.2)**
  - **Transmitter linearity (paragraph 55.5.4)**
  - **Transmitter PSD and power level (paragraph 55.5.6)**
  - **Transmitter clock frequency (paragraph 55.5.7)**
- **Specifications Based on Interoperability Requirements**
  - **Electrical specifications that affect interoperability are normative**
    - **Primary requirement is > 37 dB transmit SNR**
    - **Corresponds to < 0.2 dB implementation loss at receiver**
  - **Electrical specifications that go beyond interoperability restrict ability of manufacturers to optimize performance**

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Objectives

- **Specifications Tied to Objective Measurements**
  - **Measurements should be possible with commerical lab equipment**
  - **Errors due to lab equipment accuracy must be negligible**
  - **Measurement procedures must be unambiguous**
  - **Elaborate custom test fixtures should not be required**

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Basis for Output Voltage Specification

- **Output Voltage Range of 2.25 Vpp ± 10%**
  - **Corresponds to output power range of 4.0 dBm to 5.7 dBm (with transformer loss)**

- **Required Specification**

55.5.3.1 Peak differential output voltage

When transmitting the Test 1 waveform (i.e., repeating pattern of ten +16 symbols followed by ten -16 symbols) into a 100Ω differential resistive load, the peak-to-peak differential voltage at the MDI output shall be 2.25 V ± 10% at a point 10 nsec after the zero crossing.

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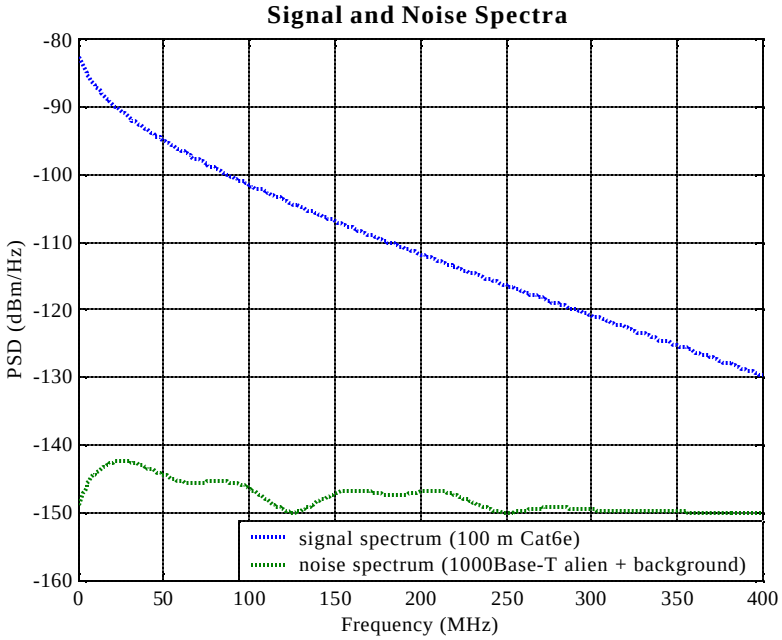
Basis for Output Voltage Specification

- **Compatible with Required Output Power Levels**
  - **Power > 4 dBm needed for > 37 dB SNR on 100m Cat6e**
    - **Based on optimal DFE calculation with 1000BASE-T ANEXT and –150 dBm/Hz background noise**
    - **Class E, 100 m ANEXT limit line applied to 1000BASE-T output PSD (1.5 Vpp before filtering)**



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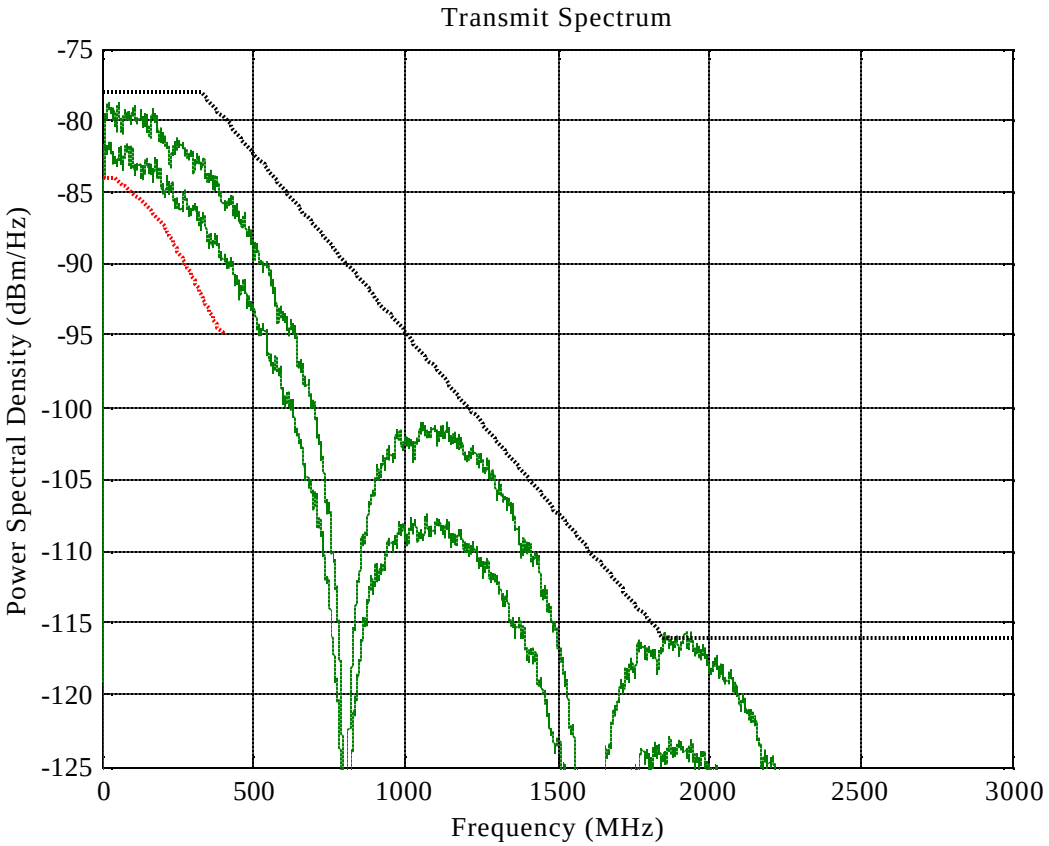
Basis for Output Voltage Specification

- **Compatible with EMI Compliant PSD Masks**



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Transmitter Droop Specification

- **Required Specification**

  55.5.3.2 Maximum output droop

  When transmitting the Test 2 waveform (i.e., repeating pattern of sixty-four +16 symbols followed by sixty-four -16 symbols) into a 100Ω differential resistive load, the magnitude of both the positive and negative droop shall be less than 10% over a period of 0.08 μsec beginning at a point 10 nsec after the zero crossing.

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Basis for Droop Specification

- **Requirement Based on 200 kHz Line Transformer HighPass Response**
  - **At least one transformer manufacturer has demonstrated lower corner frequency of 100 KHz on prototype design**
  - **Provides margin for manufacturing tolerances**
  - **800 nsec effective time constant**

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Transmitter Linearity Specification

- **Required Specification**

  55.5.4 Transmitter linearity

  When in Test mode 4 and transmitting on a single pair into a 100Ω differential resistive load, the signal to noise plus distortion ratio of the differential signal at the MDI output shall be greater than the values given in the following table. For two-tone sinusoids, signal power shall be defined as the total (sum) power of both tones. Signal to noise plus distortion ratio measurements shall be made over an effective integration time interval of not less than 10 msec and not more than 100 msec.

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Transmitter Linearity Specification

- **Required Specification (cont.)**

Signal to Noise Plus Distortion Requirements

Output Waveform Frequencies	SNDR Specification (dB)
Single tone:	
(101/1024)*800 MHz	38
(167/1024)*800 MHz	38
Two tone:	
(179/1024)*800 MHz, (181/1024)*800MHz	40
(277/1024)*800 MHz, (281/1024)*800MHz	39
(397/1024)*800 MHz, (401/1024)*800MHz	36

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Basis for Linearity Specification

- **Combine Linearity and Timing Jitter Requirements into Specification for Signal to Noise Plus Distortion**
  - **Allows transmitter implementation losses to be optimally allocated by PHY manufacturers**
  - **Test equipment limitations make accurate clock jitter measurements difficult at 10GBASE-T baud rates and jitter levels**
  - **Jitter measured on test clocks can be very different (better or worse) from jitter on MDI output due to buffering and test point accessibility**

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Basis for Linearity Specification

- **Signal to Noise plus Distortion Ratio Required for Interoperability is > 37 dB**
  - **Corresponds to < 0.3 dB link implementation loss on long lines**
- **Distortion and Noise is Frequency Dependent**
- **Sufficient Requirement for Signal to Noise Plus Distortion is**

$$\mathrm{SNDR}(f_{\mathrm{MHz}}) = \begin{cases} 40\ \mathrm{dB}, & f_{\mathrm{MHz}} \le 200 \\ 58 - 20 \cdot \log_{10}\left(f_{\mathrm{MHz}}/25\right)\ \mathrm{dB}, & 200 < f_{\mathrm{MHz}} \le 500 \end{cases}$$

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Basis for Linearity Specification

- **Signal to Noise plus Distortion Ratio Specification Based on Sinusoidal Test Signals**
  - **Sinusoidal measurements provide an accurate estimate of distortion for Tomlinson-Harishima Precoded DSQ signals**
  - **Sinusoidal measurements can be made in the frequency domain or time domain using basic lab equipment**
    - **signal averaging is not needed to achieve necessary accuracy, allowing reliable noise measurements**
  - **Sinusoidal measurements do not require special test access or complicated waveform acquisition and processing procedures**

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PSD and Power Specification

- **Required Specification**

55.5.6 Transmitter power spectral density (PSD) and power

In test mode 5 (normal operation with no power back-off), the transmit power shall be in the range 4.0 dBm to 6.0 dBm and the power spectral density of the transmitter, measured into a 100Ω differential resistive load, shall be below the upper mask and above the lower mask specified in Figure 55-26, which corresponds to:

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PSD and Power Specification

- **Required Specification (cont.)**

$$\text{Upper PSD Mask}\,(f_{\text{MHz}}) = \begin{cases} -78\ \text{dBm/Hz}, & 1 \le f_{\text{MHz}} \le 330 \\ -78 - \left(\dfrac{f_{\text{MHz}} - 330}{40}\right)\text{dBm/Hz}, & 330 < f_{\text{MHz}} \le 1850 \\ -116\ \text{dBm/Hz}, & 1850 < f \le 3000 \end{cases}$$

$$\text{Lower PSD Mask}\,(f_{\text{MHz}}) = \begin{cases} -84\ \text{dBm/Hz}, & 1 \le f_{\text{MHz}} \le 50 \\ -84 - \left(\dfrac{f_{\text{MHz}} - 50}{50}\right)\text{dBm/Hz}, & 50 < f_{\text{MHz}} \le 200 \\ -87 - \left(\dfrac{f_{\text{MHz}} - 200}{25}\right)\text{dBm/Hz}, & 200 < f \le 400 \end{cases}$$

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Basis for PSD and Power Specification

- **Upper Mask Provides EMI-Based Bound for TH Precoded DSQ Signals (see pagnanelli_2_1104)**
  - **Specified noise floor ensures > 37 dB transmit SNR**
- **Lower Mask Ensures Output Spectrum is Compatible with Expected Equalizer Capabilities**
- **PSD Masks Accommodate Reasonable Filter Design Variation and Manufacturing Tolerance**
- **Output Power Range of 4 dBm to 6 dBm Ensures > 37 dB SNR on 100m Cat6e in the Presence of 1000BASE-T ANEXT and –150 dBm/Hz Background Noise.**

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Transmitter Clock Frequency

- **Required Specification**

  55.5.7 Transmitter clock frequency

  The symbol transmission rate on each pair of the Master PHY shall be 800 Mbaud ± 50 ppm.

- **Frequency References with ± 50 ppm Tolerance are Readily Available**

- **Tighter Tolerance Eases Tracking Requirements of Low-Jitter Loop Timing Recovery Circuits**

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Conclusion

- **Specific Transmitter Electrical Specifications have been Established Based on Interoperability Requirements**

- **Specifications are Tied to Objective Measurements that can be Made Accurately with Basic Lab Test Equipment and Simple Procedures**