55.X Management interface

10GBASE-T makes extensive use of the management functions provided by the MII Management Interface (see 22.2.4), and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28.)

55.X.1 Support for Auto-Negotiation
All 10GBASE-T PHYs shall provide support for Auto-Negotiation (Clause 28) and shall be capable of operating as MASTER or SLAVE.

Auto-Negotiation is performed as part of the initial set-up of the link, and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-negotiation signaling is used for the following two primary purposes for 10GBASE-T:

a) To negotiate that the PHY is capable of supporting 10GBASE-T transmission.

b) To determine the MASTER-SLAVE relationship between the PHYs at each end of the link. This relationship is necessary for establishing the timing control of each PHY. The 10GBASE-T MASTER PHY is clocked from a local source. The SLAVE PHY uses loop timing where the clock is recovered from the received data stream.

40.5.1.1 10GBASE-T use of registers during Auto-Negotiation
A 10GBASE-T PHY shall use the management register definitions and values specified in Table 55–X1.

Table 55–X1—10GBASE-T Registers

Register	Bit	Name	Description	Type
0	0.15:0	MII control register	Defined in 28.2.4.1.1	RO
1	1.15:0	MII status register	Defined in 28.2.4.1.2	RO
4	4.15:0	Auto-Negotiation advertisement register	The Selector Field (4:4:0) is set to the appropriate code as specified in Annex 28A. The Technology Ability Field bits 4.12:5 are set to the appropriate code as specified in Annexes 28B and 28D. Bit 4.1.15 is set to logical one to indicate the desired exchange of Next Pages describing the 10 gigabit extended capabilities.	R/W
5	5.15:0	Auto-Negotiation link partner ability register.	Defined in 28.2.4.1.4. 10BASE-T implementations do not use this register to store Auto-Negotiation Link Partner Next Page data.	RO
6	6.15:0	Auto-Negotiation expansion register	Defined in 28.2.4.1.5	RO
7	7.15:0	Auto-Negotiation Next Page transmit register	Defined in 28.2.4.1.6	R/W
8	8.15:0	Auto-Negotiation link partner Next Page register	Defined in 28.2.4.1.8	RO
X	X.15:13	Test mode bits	Transmitter test mode operations are defined by bits X.15:13 as described in 55.XXX and Table 55-XXX. The default values for bits X.15:13 are all zero.	R/W
X	X.12	MASTER-SLAVE Manual Config Enable	1 = Enable MASTER-SLAVE Manual configuration value 0= Disable MASTER-SLAVE Manual configuration value. Default bit value is 0.	R/W
X	X.11	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when X.12 is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when X.12 is set to logical one. Default bit value is 0.	R/W

X	X.10	Port Type	Bit X.10 is to be used to indicate the preference to operate as MASTER (multiport device) or as SLAVE (single-port device) if the MASTER-SLAVE Manual Configuration Enable bit, X.12, is not set. Usage of this bit is described in 55.XX. 1=Multiport device 0=single-port device	R/W
X	X.9	10GBASE-T Full Duplex	1 = Advertise PHY is 1000BASE-T full duplex capable. 0 = Advertise PHY is not 1000BASE-T full duplex capable.	R/W
X	X.8:0	Reserved	Write as 0, ignore on read.	R/W
Y	Y.15	MASTER-SLAVE configuration fault.	Configuration fault, as well as the criteria and method of fault detection, is PHY specific. The MASTER-SLAVE Configuration Fault bit will be cleared each time register Y is read via the management interface and will be cleared by a 10GBASE-T PMA reset. This bit will self clear on Auto-Negotiation enable or Auto-Negotiation complete. This bit will be set if the number of failed MASTER-SLAVE resolutions reaches 7. For l0GBASE-T, the fault condition will occur when both PHYs are forced to be MASTERs or SLAVEs at the same time using bits X.12 and X.11. Bit Y.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 55.XXX. 1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration faultdetected	RO/LH/SC
Y	Y.14	MASTER-SLAVE configuration resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	RO
Y	Y.13	Local Receiver Status	1 = Local Receiver OK (loc_rcvr_status=OK) 0 = Local Receiver not OK (loc_rcvr_status=NOT_OK) Defined by the value of loc_rcvr_status as per 55.XXX.	RO
Y	Y.12	Remote Receiver Status	1 = Remote Receiver OK (rem_rcvr_status=OK) 0 = Remote Receiver not OK (rem_rcvr_status=NOT_OK) Defined by the value of rem_rcvr_status as per 55.XXX.	RO
Y	Y.11	LP 10GBASE-T FD	1 = Link Partner is capable of 10GASE-T full duplex 0 = Link Partner is not capable of 10GBASE-T full duplex This bit is guaranteed to be valid only when the Page received bit (6.1) has been set to 1.	RO
Y	Y.9:8	Reserved	Reserved	RO
Y	Y.7:0	Idle Error Count	Idle Error Count Bits Y.7:0 indicate the Idle Error count, where Y.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rxerror_status is equal to ERROR. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and are to be held at all ones in case of overflow (see 30.5.1.1.11).	RO/SC
15	15.15:12	Extended status register	See 22.2.4.4	RO

55.X.1.2 10GBASE-T Auto-Negotiation page use

10GBASE-T PHYs shall exchange a 10GBASE-T formatted Next Page, and two 10GBASE-T unformatted Next Pages in sequence, without interruption, as specified in Table 55-XX. In the event that the DTE also wishes to advertise 1000BASE-T abilities, the 10GBASE-T pages will follow the 1000BASE-T pages. Additional Next Pages can be exchanged as described in Annex 40C.

Note that the Acknowledge 2 bit is not utilized and has no meaning when used for the 10GBASE-T message page exchange.

Table 55–X2—10GBASE-T Base and Next Pages bit assignments

Bit	Bit definition	Register location
BASE PAGE		
D15	1 (to indicate that Next Pages follow)	
D14:D1	As specified in 28.2.1.2	Management Register 4
Page 0 (Message Next Page)		
M10:M0	9	
Page 1 (Unformatted Next Page)		
U10:U4	Reserved transmit as 0	
U3	10GBASE-T full duplex	Register X.9 MASTER-SLAVE Control register
U2	10GBASE-T port type bit (1 = multiport device and 0 = single-port device)	Register X.10 MASTER-SLAVE Control register
U1	10GBASE-T MASTER-SLAVE Manual Configuration value (1 = MASTER and 0 = SLAVE). This bit is ignored if 9.12 = 0.	Register X.11 MASTER-SLAVE Control register
U0	10GBASE-T MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable.) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 9.11.	Register X.12 MASTER-SLAVE Control register
Page 2 (Unformatted Next Page)		
U10:U0	10GBASE-T MASTER-SLAVE Seed bits 10:0. Bit U10 contains the MSB and bit U0 contains the LSB.	MASTER-SLAVE Seed Value (10:0)

55.X.1.3 Sending Next Pages

Implementors who do not wish to send additional Next Pages (i.e., Next Pages in addition to those required to perform PHY configuration as defined in this clause) can use Auto-Negotiation as defined in Clause 28 and the Next Pages defined in 55.X.1.2. Implementors who wish to send additional Next Pages are advised to consult Annex 40C.

55.X.2 MASTER-SLAVE configuration resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 55–XX with the 10GBASE-T Technology Ability Next Page bit values specified in Table 55–XX and information received from the link partner. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown in the Arbitration state diagram (Figure 28–13.)

The following four equations are used to determine these relationships:

manual_MASTER = U0 * U1
manual_SLAVE = U0 * !U1
single-port device = !U0 * !U2,
multiport device = !U0 * U2

where

U0 is bit 0 of unformatted page 1,
U1 is bit 1 of unformatted page 1, and
U2 is bit 2 of unformatted page 1 (see Table 40–4).

A 10GBASE-T PHY is capable of operating either as the MASTER or SLAVE. In the scenario of a link between a single-port device and a multiport device, the preferred relationship is for the multiport device to be the MASTER PHY and the single-port device to be the SLAVE. However, other topologies may result in contention. The resolution function of Table 55–X3 is defined to handle any relationship conflicts.

Table 55–X3—10GBASE-T MASTER-SLAVE configuration resolution table

Local device type	Remote device type	Local device resolution	Remote device resolution
single-port device	multiport device	SLAVE	MASTER
single-port device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	manual_MASTER	SLAVE	MASTER
manual_SLAVE	multiport device	SLAVE	MASTER
multiport device	manual_MASTER	SLAVE	MASTER
manual_SLAVE	single-port device	SLAVE	MASTER
multiport device	single-port device	MASTER	SLAVE
multiport device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	manual_SLAVE	MASTER	SLAVE
manual_MASTER	single-port device	MASTER	SLAVE
single-port device	manual_SLAVE	MASTER	SLAVE
manual_MASTER	multiport device	MASTER	SLAVE
multiport device	multiport device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
single-port device	single-port device	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.	The device with the higher SEED value is configured as MASTER, otherwise SLAVE.
manual_SLAVE	manual_SLAVE	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault
manual_MASTER	manual_MASTER	MASTER-SLAVE configuration fault	MASTER-SLAVE configuration fault

The rationale for the hierarchy illustrated in Table 40–5 is straightforward. A 1000BASE-T multiport device has higher priority than a single-port device to become the MASTER. In the case where both devices are of the same type, e.g., both devices are multiport devices, the device with the higher MASTER-SLAVE seed bits (SB0...SB10), where SB10 is the MSB, shall become the MASTER and the device with the lower seed value shall become the SLAVE. In case both devices have the same seed value, both should assert link_status_10GigT=FAIL (as defined in XXX) to force a new cycle through Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete.

The method of generating a random or pseudorandom seed is left to the implementor. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 2^{11}– 2. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. When MASTER-SLAVE resolution is complete, the seed counter shall be reset to 0 and bit Y.15 shall be set to logical zero. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit X.12) and the MASTERSLAVE Config Value bit (control register bit X.11) are used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Configuration fault condition, thus the MASTER-SLAVE Configuration fault bit (status register bit Y.15) shall be set to logical one. The MASTER-SLAVE Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and link_status_10GigT shall be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force a new cycle through Auto-Negotiation after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occurs on the entrance to

the FLP LINK GOOD CHECK state (Figure 28–16) when the highest common denominator (HCD) technology is 1000BASE-T. The resulting MASTER-SLAVE value is used by the 1000BASE-T PHY control (55.XXX).

If MASTER-SLAVE Manual Configuration is disabled (bit X.12 is set to 0) and the local device detects that both the local device and the remote device are of the same type (either multiport device or single-port device) and that both have generated the same random seed, it generates and transmits a new random seed for MASTER-SLAVE negotiation by setting link_status to FAIL and cycling through the Auto-Negotiation process again.

The MASTER-SLAVE configuration process returns one of the three following outcomes:

a) *Successful:* Bit Y.15 of the 1000BASE-T Status Register is set to logical zero and bit Y.14 is set to logical one for MASTER resolution or for logical zero for SLAVE resolution. 1000BASE-T returns control to Auto_Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–16) and passes the value MASTER or SLAVE to PMA_CONFIG.indicate (see 55.XXX.)
b) *Unsuccessful:* link_status_10GigT is set to FAIL and Auto-Negotiation restarts (see Figure 28–16.)
c) *Fault detected:* (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit Y.15 of the 1000BASE-T Status Register is set to logical one to indicate that a configuration fault has been detected. This bit also is set when seven attempts to configure the MASTER SLAVE relationship via the seed method have failed. When a fault is detected, link_status_1GigT is set to FAIL, causing Auto-Negotiation to cycle through again.

NOTE—MASTER-SLAVE arbitration only occurs if 10GBASE-T is selected as the highest common denominator; otherwise, it is assumed to have passed this condition.

Modifications to Annex 28B

Modify 28B.3

a) 10GBASE-T full duplex

will need to bump each other technology down one

Modifications to Annex 28C.

Add to table 28C-1

Message Code #	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
9	0	0	0	0	0	0	0	1	0	0	1	10GBASE-T Technology Message Code. Two 10GBASE-T Ability Pages to follow using Unformatted Next Pages.
10...	0	0	0	0	0	0	0	1	0	1	0	Reserved for future Auto-Negotiation use

Add 28C.11 Message Code #9 – 10GBASE-T technology message code

Clause 55 (10GBASE-T) uses Next Page Message Code 9 to indicate that 10GBASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two unformatted Next Pages that contain information defined in 55.X.X.X.

Modifications to Annex 28D

Will need to add section 28D.6 Extensions required for Clause 55 (10GBASE-T)
Recommend to use 28D.5 as a starting point.