



THE LDPC 4D-PAM8 Proposal for 10GBASE-T

IEEE 802.3an Task Force

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Agenda

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Outline



ref: rao_1_1103.pdf, November 2003, slide 10

Four main ingredients of the LDPC 4D-PAM8 proposal:

- 1 Gs/s 8-Level Pulse Amplitude Modulation (PAM) signaling.
- 12dB Co-set Partitioning.
- (2048, 1723) RS-LDPC block encoding using 320bytes of XGMII data over 80 cycles of XGMII clock.
- Tomlinson-Harashima pre-coding with transmit shaping.



Co-set Partitioning

from: rao_1_1103.pdf, November 2003, slide 11

12dB Co-set Partitioning

○ +2

● +1

○ 0

● -1

○ -2

6dB co-set partitioning
in 4DPAM-5 1000BASE-T
(transmit 5 levels, but achieve
noise immunity of 3 level
transmission)

○ +7

● +5

● +3

● +1

○ -1

● -3

● -5

● -7

12dB co-set partitioning
in 4DPAM-8 10GBASE-T
(transmit 8 levels, but achieve
noise immunity of 2 level
transmission)

(2048,1723) RS-LDPC Block Encoding



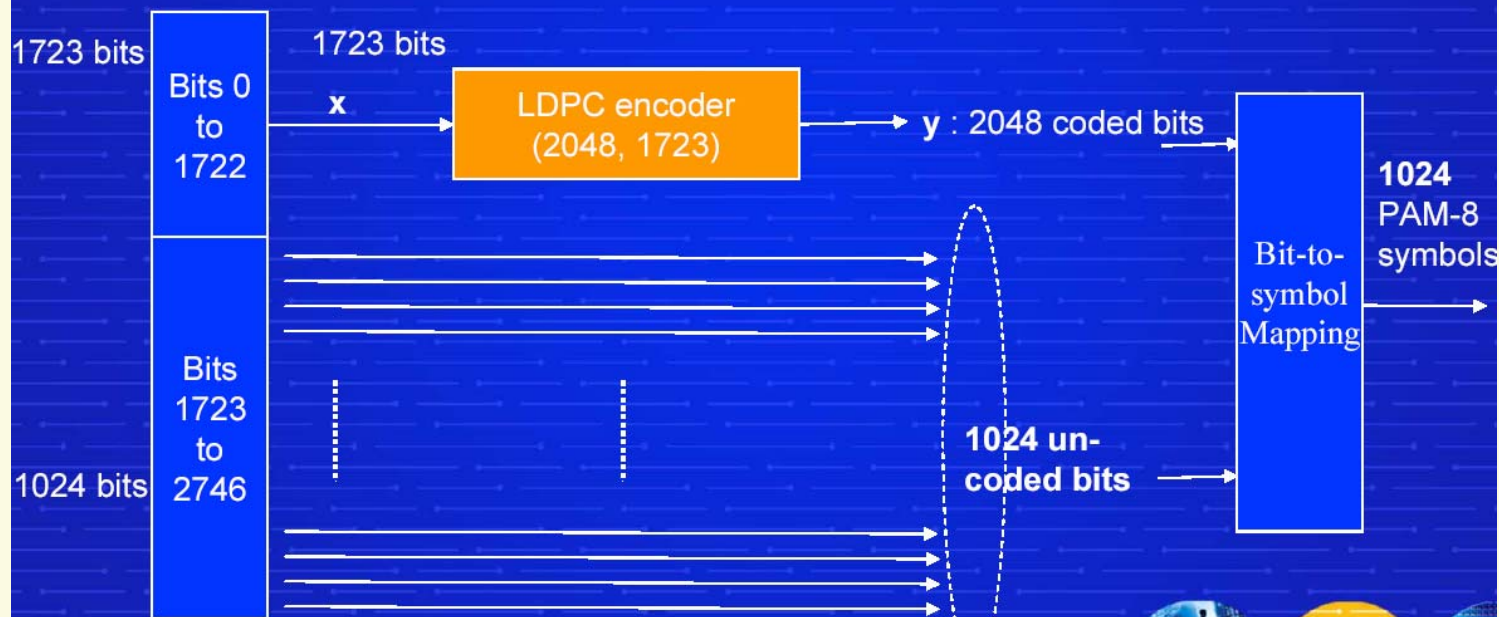
from: rao_1_1103.pdf, November 2003, slide 12

LDPC Co-set Encoding

Data block size = 2560 bits over 256 symbols

Control block size = 187 bits

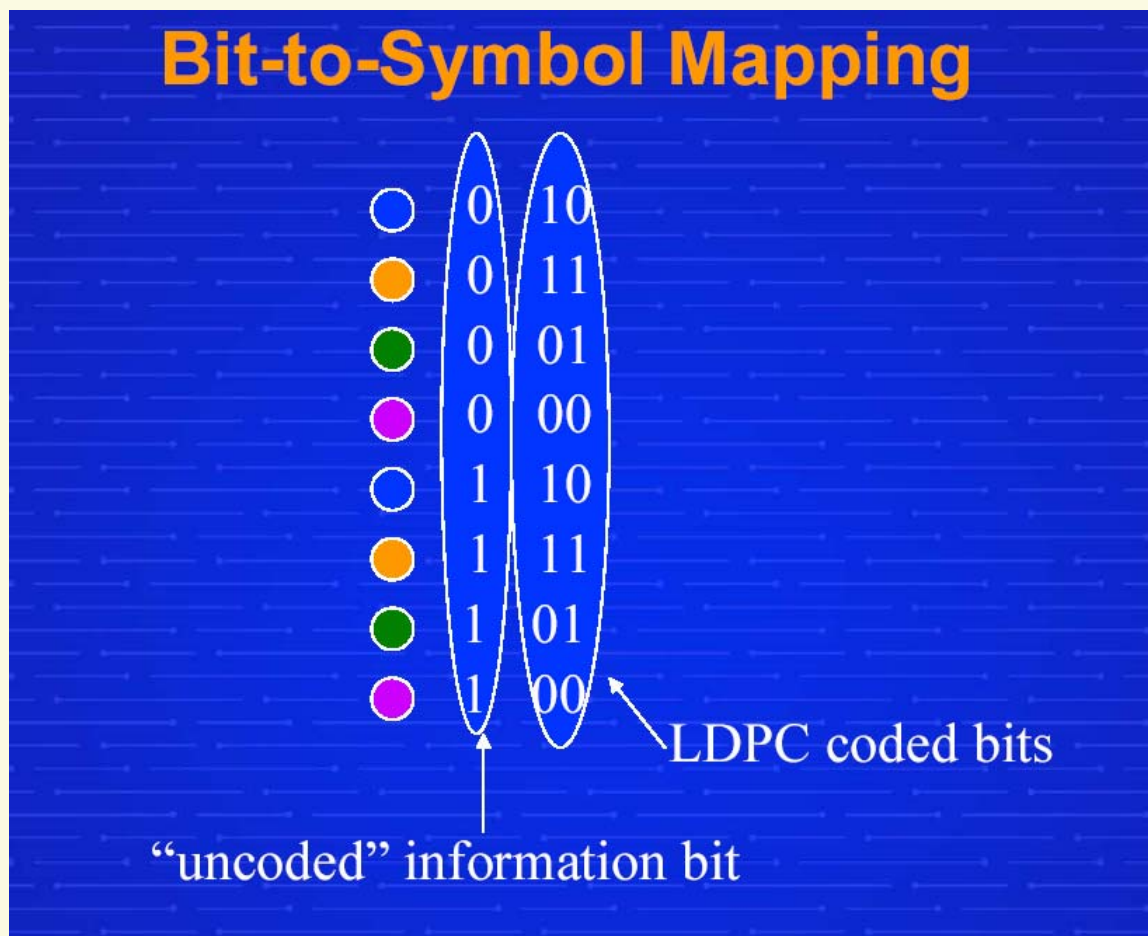
Information block size = 2747 bits = 1723+1024 bits





Bit-to-Symbol Mapping

from: rao_1_1103.pdf, November 2003, slide 13

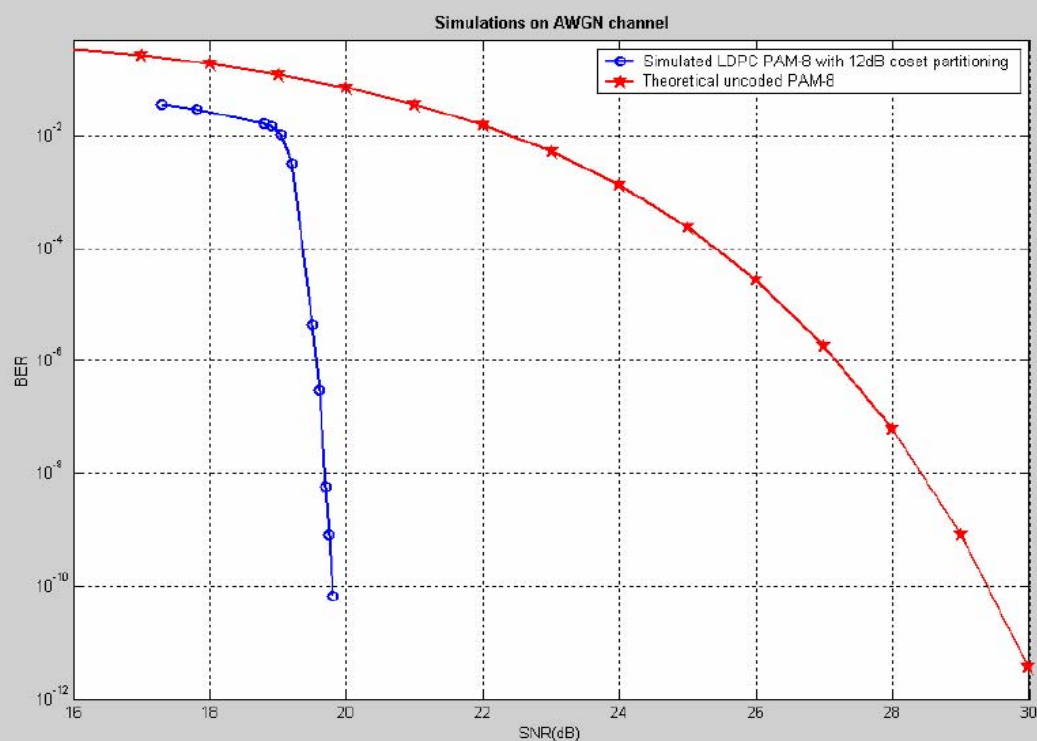


Simulation Results

from: rao_1_1103.pdf, November 2003, slide 15



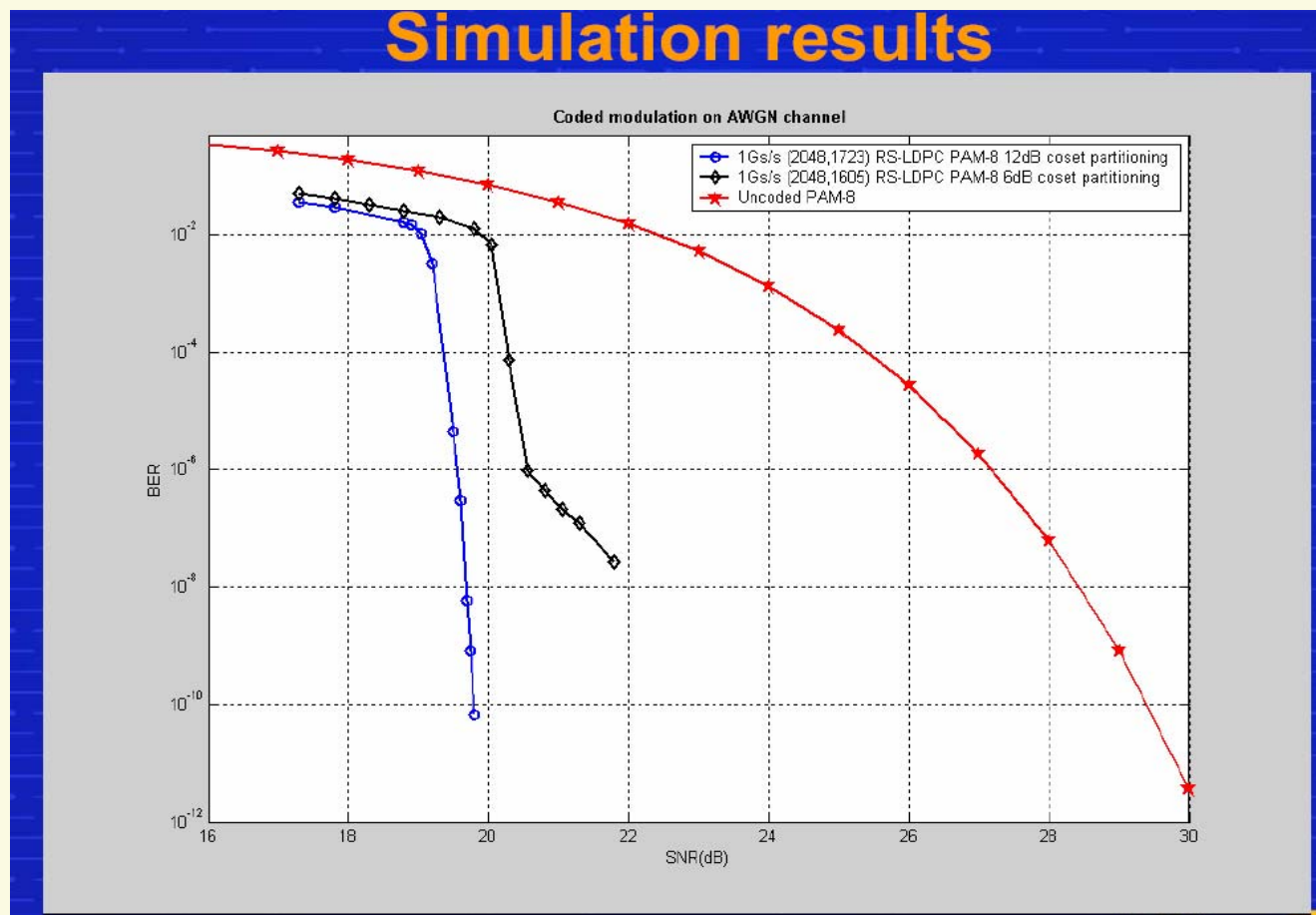
Example Simulation results





Simulation Results

from: rao_1_1103.pdf, November 2003, slide 16

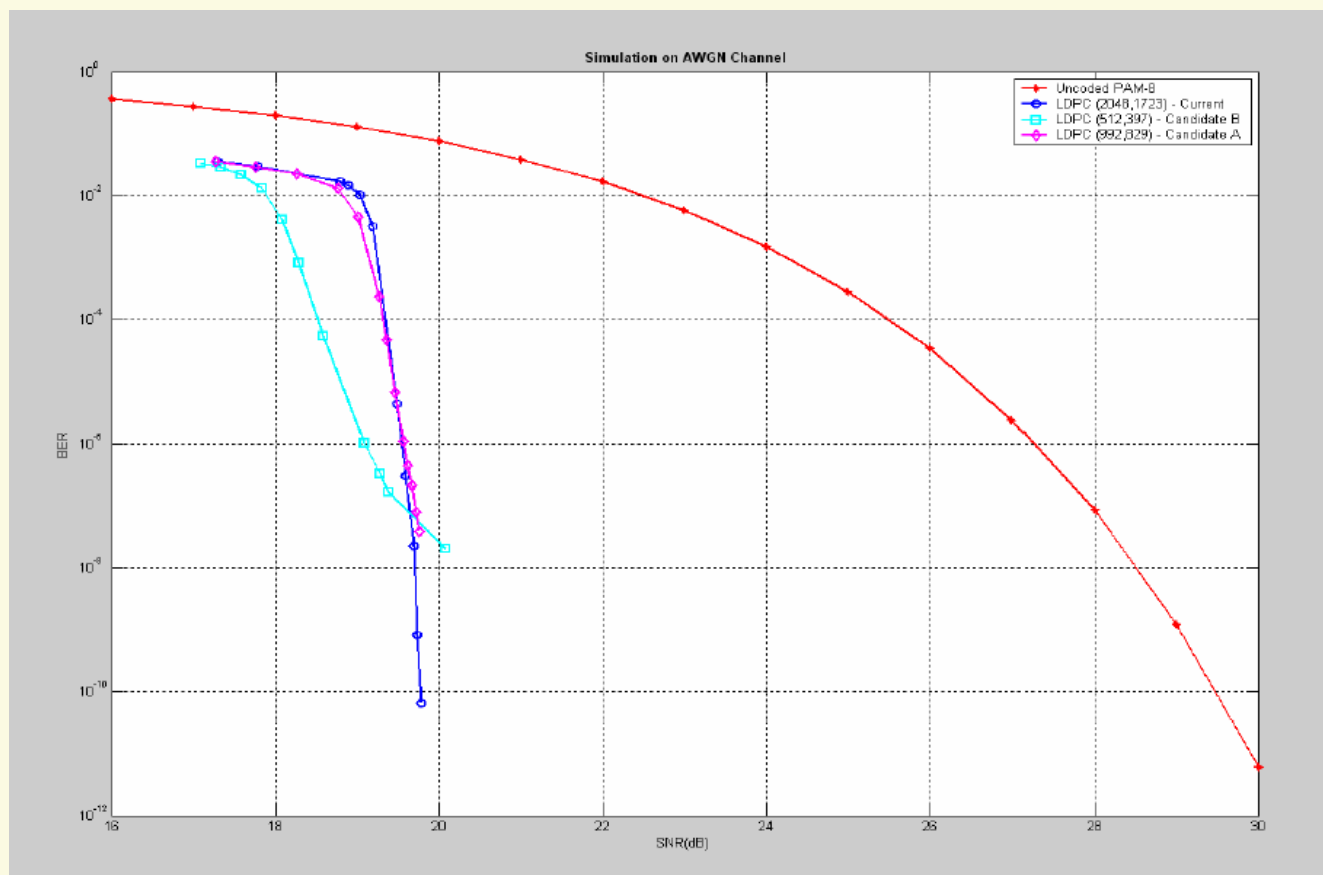


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THE LDPC 4D-PAM8 Proposal

Lower latency LDPC codes

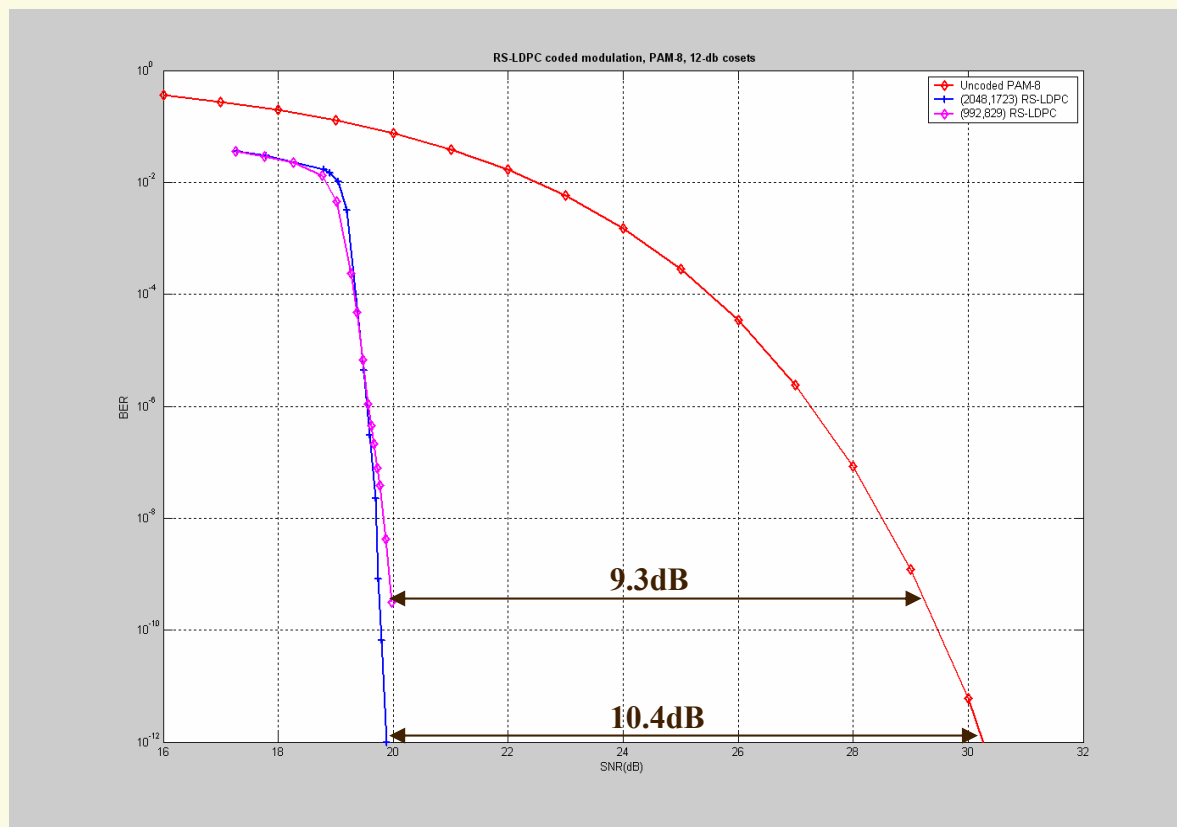
from: rao_1_0504.pdf, May 2004, slide 7



Updated Simulation Results



(2048,1723) curve augmented from seki_1_0304.pdf, March 2004, slide 4



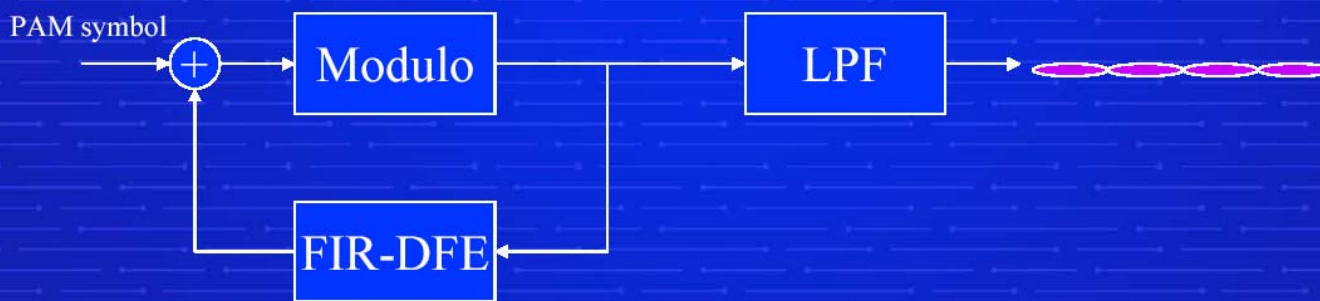


Tomlinson-Harashima Pre-coding

from: rao_1_1103.pdf, November 2003, slide 17

Tomlinson-Harashima Pre-coding

- Independently developed by Tomlinson and Harashima in 1971.
- Uses a Decision Feedback Equalizer at the transmitter instead of the receiver
 - receiver computes DFE coefficients during startup and sends coefficients over to transmitter
 - advantage - allows for block processing and decoding at the receiver.
 - advantage - reduces complexity of receiver analog front end.
 - drawback - increases complexity of transmitter.

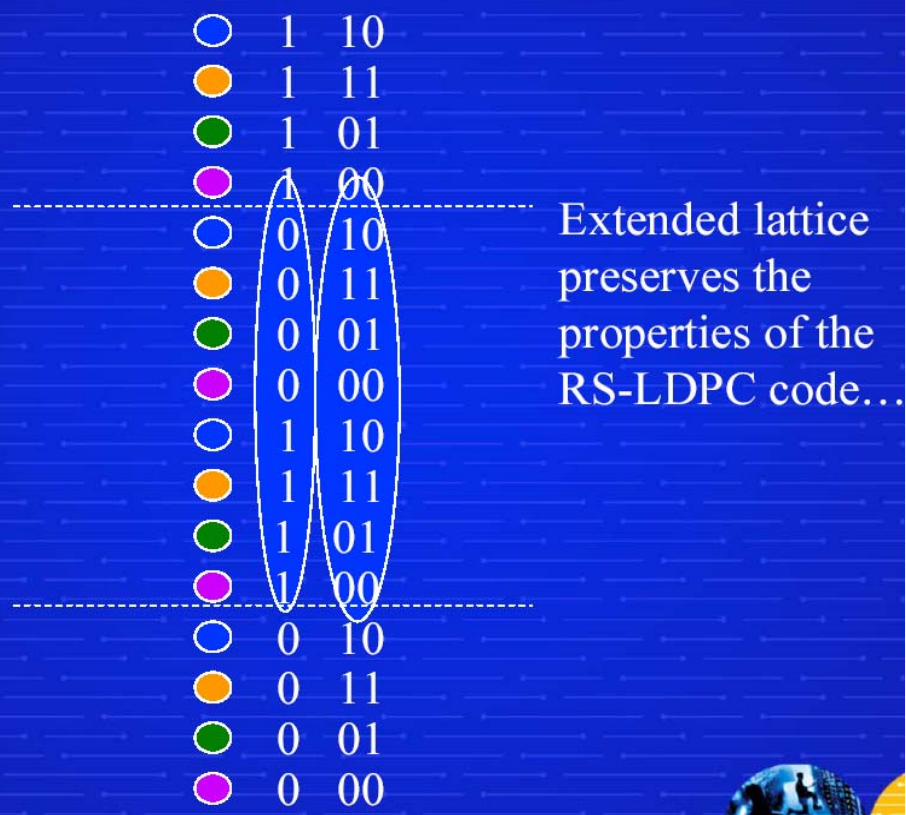




Extended Lattice Mapping

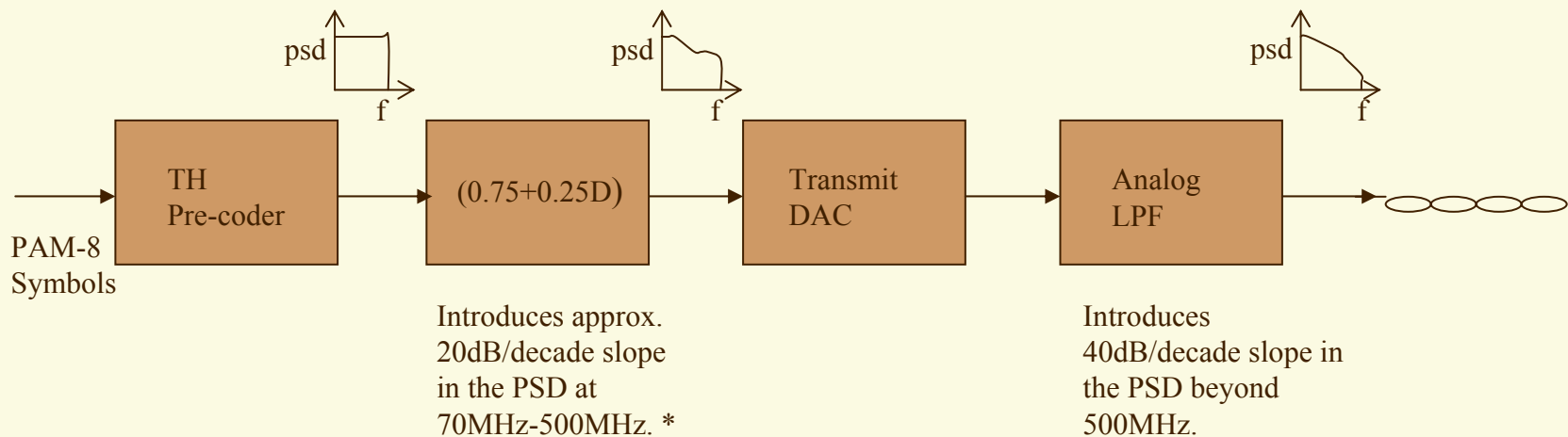
from: rao_1_1103.pdf, November 2003, slide 18

Extended Lattice Mapping





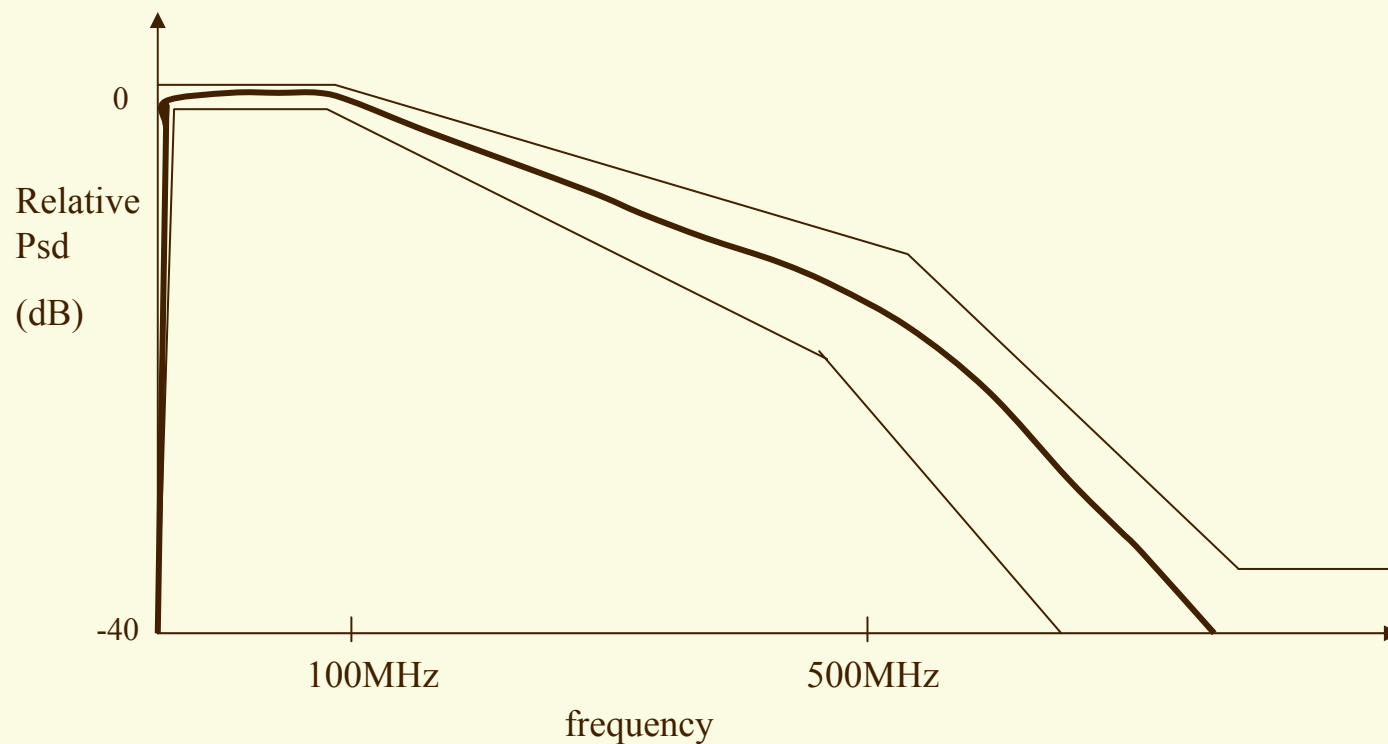
Transmitter Block Diagram



1. *20dB/decade slope in the transmit power spectral density (PSD) at 30MHz-125MHz was engineered in the 100BASE-Tx system using MLT-3 encoding
2. *20dB/decade slope in the transmit PSD at 30MHz-125MHz was engineered in the 1000BASE-T system using the $(0.75+0.25D)$ digital filter
3. 20dB/decade slope at high frequencies dovetails with the 20dB/decade increase in the emissions characteristics of cabling systems

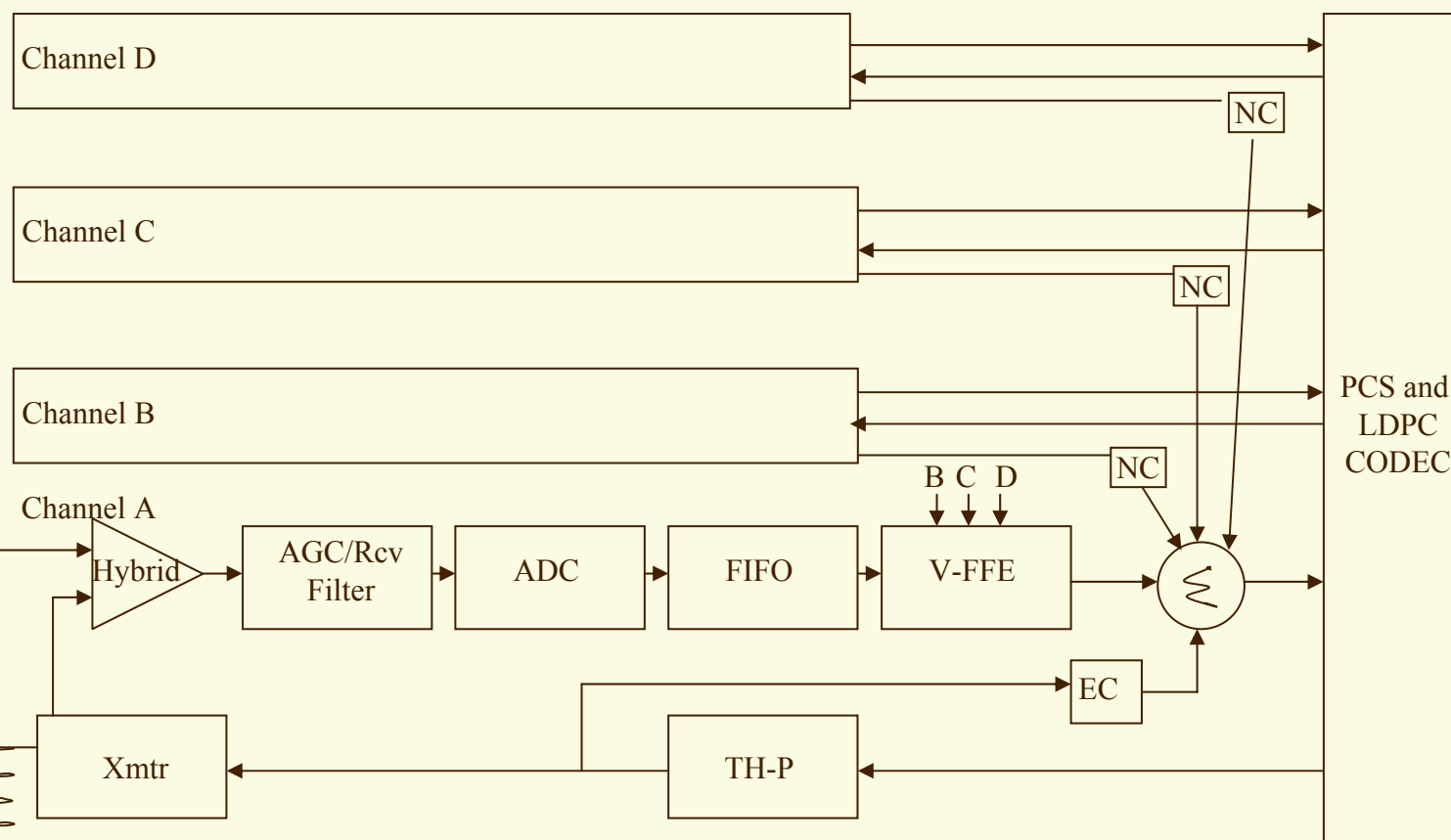


Relative PSD Specifications





Transceiver Block Diagram



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THE LDPC 4D-PAM8 Proposal

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Task Force Spreadsheet

Information needed for evaluation of proposals	Rationale for request	Comments/details	units	results
Performance				
Link margin on channel models 1, 2, 3; use CAT6 formulas extrapolated to 625MHz for other parameters than IL and ANEXT	To determine if the proposal meets the reach objectives and by what margin: REQUIRED	increase in anext coefficient (not slope) that will allow 1E-12 BER	dB	m1:5.2dB m2:6.1dB m3:6.3dB
Distance with 3dB margin (worse insertion loss) on channel model #4	To determine reach over installed base: REQUIRED	3dB margin applied to anext coefficient.	meters	110m
Intrinsic Latency (from XGMII on TX side to XGMII on RX side assuming 100m cable)	To come up with specification in standard	assume 500ns for cable itself	ns	768ns
Transmit PSD at phy output for channel models 1,2,3)	To evaluate if proposal will meet CISPR/FCC Class A requirements: REQUIRED	plotted up to 700Mhz, include assumed transfer function of transformer; Is there interest in Class B?	dBm/Hz	See Presentation Plot
Crane test result: Immunity to sinusoidal noise without adaptation	To evaluate robustness of proposal to sinusoidal interference			68mV ptp
Jitter tolerance	To evaluate feasibility of implementation	Use channel model #1; assume gaussian distribution of jitter; provide max rms value that give 1E-12 BER	ps	3ps RMS



Task Force Spreadsheet

Transmitter Assumptions for stated performance				
Modulation	Will have to be specified in standard: REQUIRED	Format (PAM, QAM, VSB, DMT, MLT etc), number of levels		4DPAM-8
FEC code	Will have to be specified in standard: REQUIRED	LDPC, RS, TCM etc.	code rate; block size, # of states etc.	(2048,1723) LDPC
Symbol rate	Will have to be specified in standard: REQUIRED		MHz	1Gs/s
Transmitter equalization	Will have to be specified in standard: REQUIRED	Structure, #taps, fixed vs. adaptive		T-H precoding 32-tap Adaptive
Digital transmit filter assumed in specified transmit PSD	To enable others to validate transmit PSD claimed in item #6	number of taps, coefficients		(0.75+0.25D)



Task Force Spreadsheet

Assumed DAC resolution	To enable others to validate transmit PSD claimed in item #6	Assume ideal DAC	bits	9bit effective
Assumed DAC speed	To enable others to validate transmit PSD claimed in item #6	Assume ideal DAC	MHz	1000
Analog transmit filter	To enable others to validate transmit PSD claimed in item #6	number of poles; transfer function		BW5 @500M Hz
Max transmit launch voltage (differential)	Will have to be specified in standard: REQUIRED		V	0.75V pk-pk TO 2.5V pk-pk
Transmit peak voltage	To estimate feasibility of implementing transmitter PMA		dB	2.5V pk-pk
Max allowable distortion on transmitter	To estimate feasibility of implementing transmitter PMA	Budget for TX distortion relative to TX power for channel model #3	dB	2.5mV peak



Task Force Spreadsheet

Receiver assumptions for stated performance				
Assumed echo suppression	To enable others to validate performance claims	dB	dB	55dB
Assumed echo canceller length	To enable others to validate feasibility of claimed echo suppression & complexity	span of echo being cancelled	# of symbol intervals	512
Assumed next canceller length	To enable others to validate performance and complexity claims	span of NEXT being cancelled	# of symbol intervals	256
Assumed Fext canceller length	To enable others to validate performance and complexity claims	span of FEXT being cancelled	# of symbol intervals	64
Assumed equalization approach & parameters	To enable others to validate performance and complexity claims	structure, # taps		64tap FFE
Assumed ideal ADC speed	To estimate feasibility of implementing receiver AFE and power consumption		MHz	1000Ms/s



Task Force Spreadsheet

min required resolution of ADC	To estimate feasibility of implementing receiver AFE and power consumption	Assume ideal ADC	bits	8bit effective
PAR at input to ADC	To enable others to validate viability of claimed performance relative to ADC resolution	Channel model #3; signal power relative to ADC full scale range	dB	14dB
How much echo cancellation required prior to ADC?	To enable others to validate viability of claimed performance relative to ADC resolution	level of echo suppression	dB	25dB
Assumed Base line wander correction if proposed	To enable others to validate viability of claimed performance relative to ADC resolution	max base line wander	Volts	None
Assumed additive gaussian noise of receiver	To estimate feasibility of implementing receiver AFE and power consumption	This is distinct from the line background noise of -150dBm/Hz	dBm/Hz	-150
Assumed analog receive filter prior to ADC	To estimate feasibility of implementing receiver AFE and power consumption	# of poles, zeros, location of poles zeros, assumed performance of magnetics		BW3 @ 500MHz



Task Force Spreadsheet

Complexity estimate of digital processing	To let task force members estimate power consumption, cost of PHY being proposed and judge broad market potential	assuming clock rate of digital processing is equal to symbol rate	gate count, million	6M gates
Maximum voltage on PHY side of transformer	To estimate max supply voltage and requirements on process used to implement AFE circuits	Consider a short cable with both near end and far end transmitters operating	Volts	3.75V pk-pk at 100m
Estimated power consumption of PHY	Include AFE, Digital, any external components etc.		Watts	7W



Current Status

- ☞ Currently, there are 6 proposals on the table for 10GBASE-T
 - 5 of the 6 proposals use PAM line coding, with number of levels varying from 8 to 12
 - 5 of the 6 proposals use LDPC Block coding for Forward Error Correction
 - 4 of the 6 proposals use a Tomlinson-Harashima pre-coding strategy for channel equalization
 - ~significant consensus on the key ingredients of the LDPC 4D-PAM8 proposal since it was introduced to the study group in November 2003.
- ☞ The Task Force has also agreed to use a Transmit Power back-off scheme to deal with Alien FEXT issues.



Proposals under consideration

Name Attribute	1000BASE-T (for Reference)	LDPC 4D- PAM8	PAM8 with No Filter	LDPC 4D- PAM12 (2)	TCM 4D- PAM10	LPDC OFDM
Symbol Rate (Period)	125Ms/s (8.0ns)	1000Ms/s (1.0ns)	1000Ms/s (1.0ns)	820Ms/s (1.23ns)	833Ms/s (1.2ns)	156Ms/s (6.4ns)
Number of PAM Levels	5	8	8	12	10	30+18+18 +8+8
Coset Partition (Coding Gain)	6dB	12dB	12dB	12dB	6dB	12dB
Transmit Filter	(0.75+0.25D)	(0.75+0.25D)	None	None	None	None



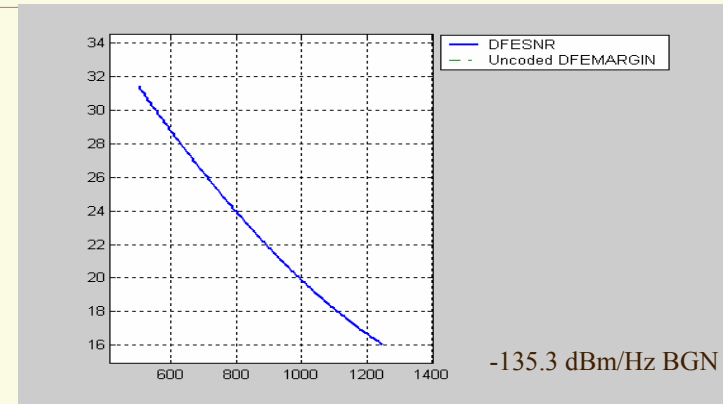
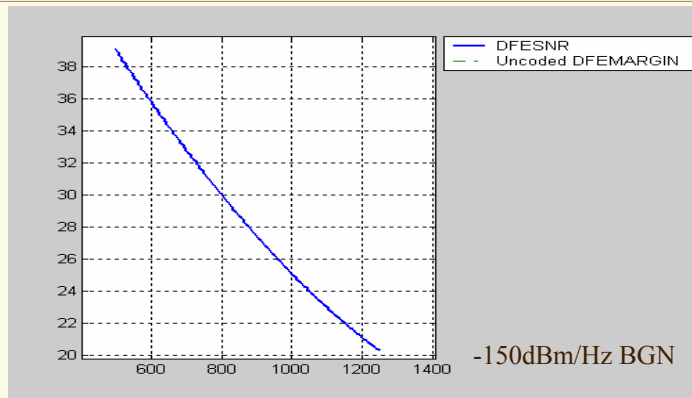
Performance Evaluations

1. Use `solarsep_varlen7a.m` code AS IS and report optimum DFE SNR and margin for the 3 channel models
 - M1: 100m 4-connector Cat6e with 64.5dB ANEXT intercept
 - M2: 55m 4-connector Cat6e with 49.5dB ANEXT intercept
 - M3: 100m 4-connector Cat7 with 62.5dB ANEXT intercept
2. Increase Background noise component in `solarsep_varlen7a.m` code and report maximum background noise level at which $1E-12$ BER is achieved.

Model 1: Performance Comparison



100m Cat6e 4Conn IL, 64.5dB ANEXT at 100MHz, split slope, Default Cancellation Parameters

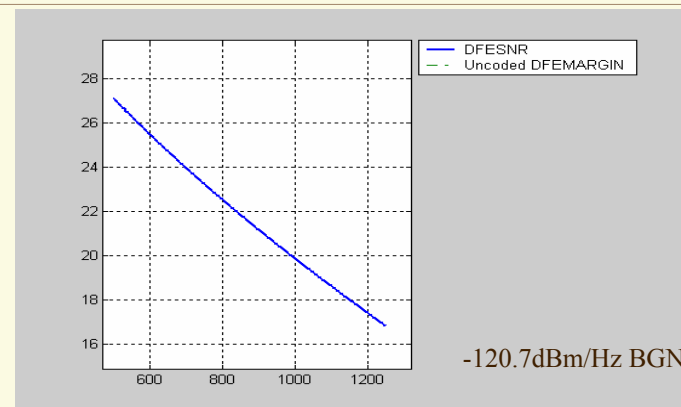
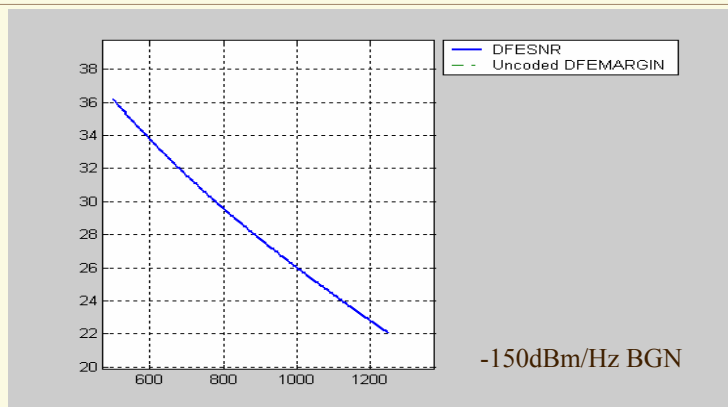


Proposal	Symbol Rate	SNR for 1E-12 BER	SNR at -150dBm WGN	Margin at -150dBm WGN	WGN for 1E-12 BER	SNR at -135.3dBm WGN	Margin at -135.3dBm WGN
LDPC 4D-PAM8	1000Ms/s	19.9dB	25.1dB	5.2dB	-135.3dBm	19.9dB	0dB
LDPC 4D-PAM12	820Ms/s	23.8dB	29.5dB	5.7dB	-135.8dBm	23.5dB	-0.3dB
TCM 4D-PAM10	833Ms/s	26.2dB	29.1dB	2.9dB	-140.5dBm	23.1dB	-3.1dB

Model 2: Performance Comparison



55m Cat6e 4Conn IL, 49.5dB ANEXT at 100MHz, split slope, Default Cancellation Parameters

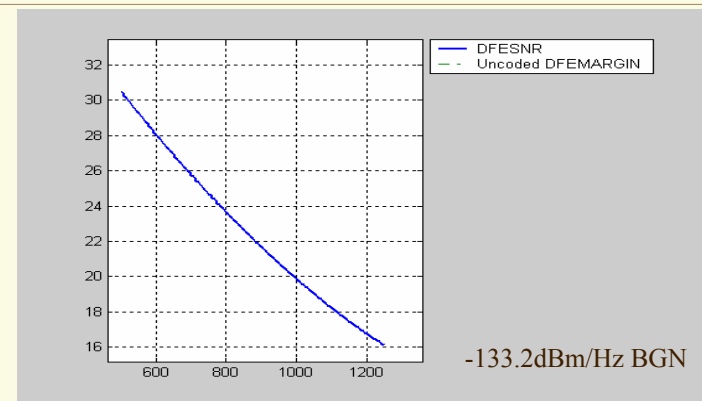
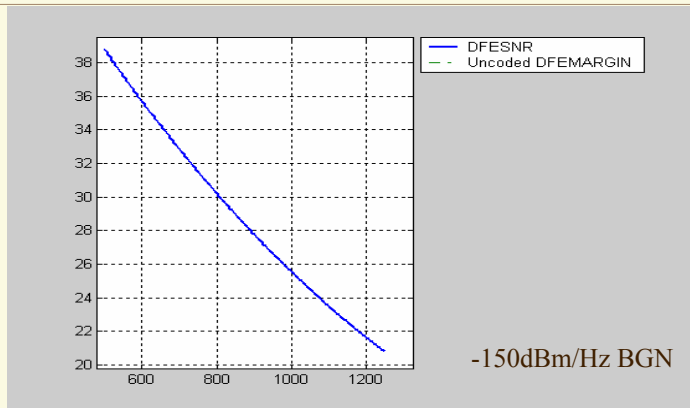


Proposal	Symbol Rate	SNR for 1E-12 BER	SNR at -150dBm WGN	Margin at -150dBm WGN	WGN for 1E-12 BER	SNR at -120.7dBm WGN	Margin at -120.7dBm WGN
LDPC 4D-PAM8	1000Ms/s	19.9dB	26.0dB	6.1dB	-120.7dBm	19.9dB	0dB
LDPC 4D-PAM12	820Ms/s	23.8dB	29.2dB	5.4dB	-123.1dBm	22.3dB	-1.5dB
TCM 4D-PAM10	833Ms/s	26.2dB	28.9dB	2.7dB	-128.2dBm	22.0dB	-4.2dB

Model 3: Performance Comparison



100m Cat7 4Conn IL, 62.5dB ANEXT at 100MHz, split slope, Default Cancellation Parameters



Proposal	Symbol Rate	SNR for 1E-12 BER	SNR at -150dBm WGN	Margin at -150dBm WGN	WGN for 1E-12 BER	SNR at -120.7dBm WGN	Margin at -120.7dBm WGN
LDPC 4D-PAM8	1000Ms/s	19.9dB	25.5dB	5.6dB	-133.2dBm	19.9dB	0dB
LDPC 4D-PAM12	820Ms/s	23.8dB	29.7dB	5.9dB	-134.0dBm	23.2dB	-0.6dB
TCM 4D-PAM10	833Ms/s	26.2dB	29.4dB	3.2dB	-138.5dBm	22.9dB	-3.3dB



Unit Pulse Analysis

QUESTION: Why is the LDPC 4D-PAM12 system more sensitive to external background noise than the LDPC 4D-PAM8 system on Models 1 and 3 even though it clearly had the better SNR margin at -150dBm/Hz?

- The answer requires us to go back to first principles, i.e., “unit pulse analysis”

Assume that the transmit launch voltage is 2V peak-to-peak for all proposals

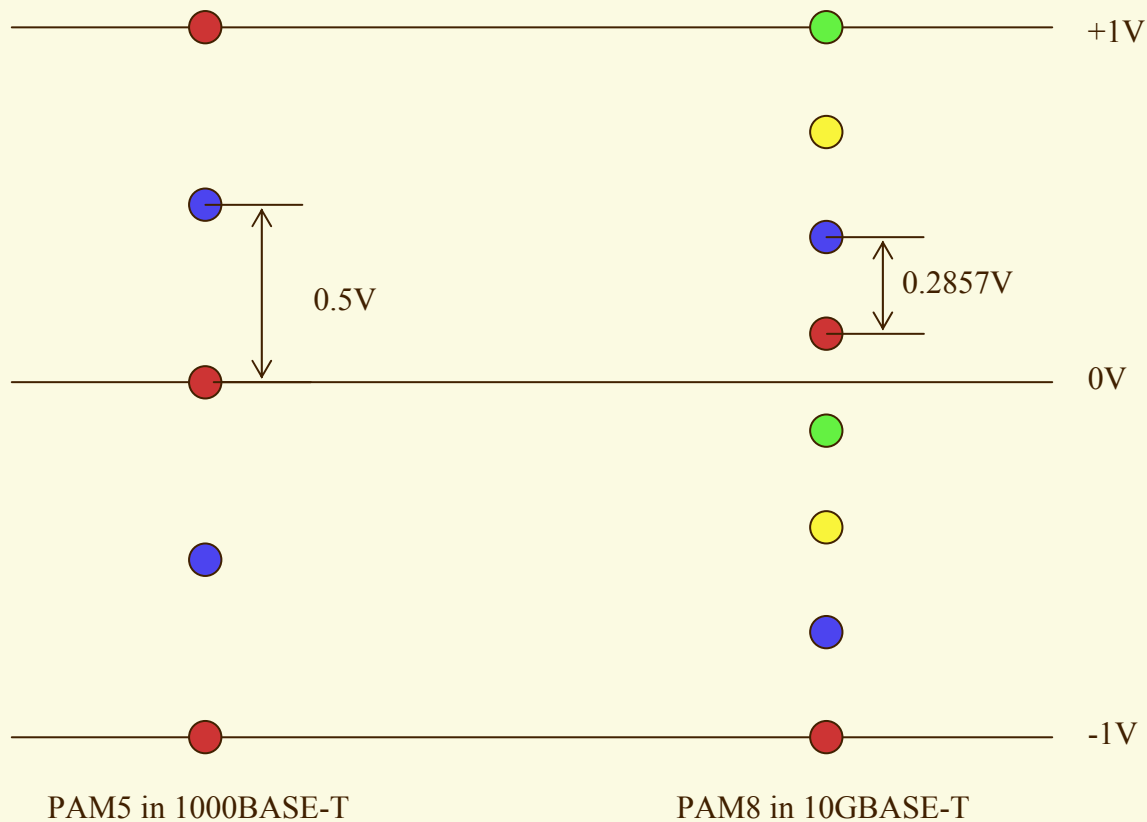
- Peak voltage determines the difficulty of the transceiver analog circuit design.

Compare the Received Unit Pulse Response for each proposal at the end of a 100m/55m worst-case 4-connector Extended Category 6 cable

- Matlab source code (Etxt2a.m) for unit pulse response calculation was distributed in the IEEE 802.3ab task force.
- The peak amplitude of the Received Unit Pulse Response determines the robustness of the system to external disturbances (Crane test result for pre-equalized systems).

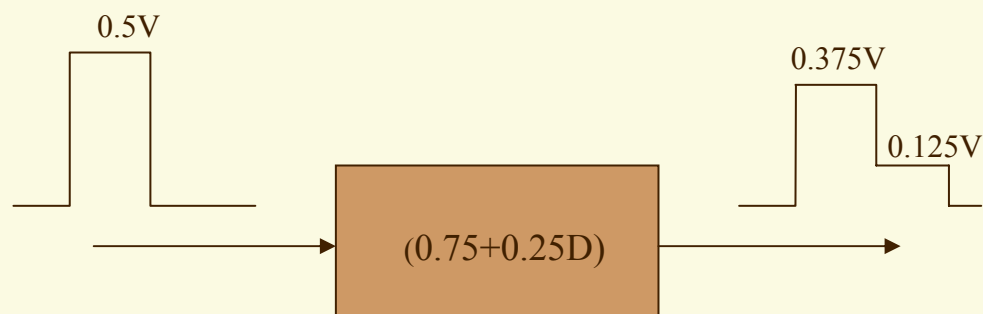


Separation Between Levels



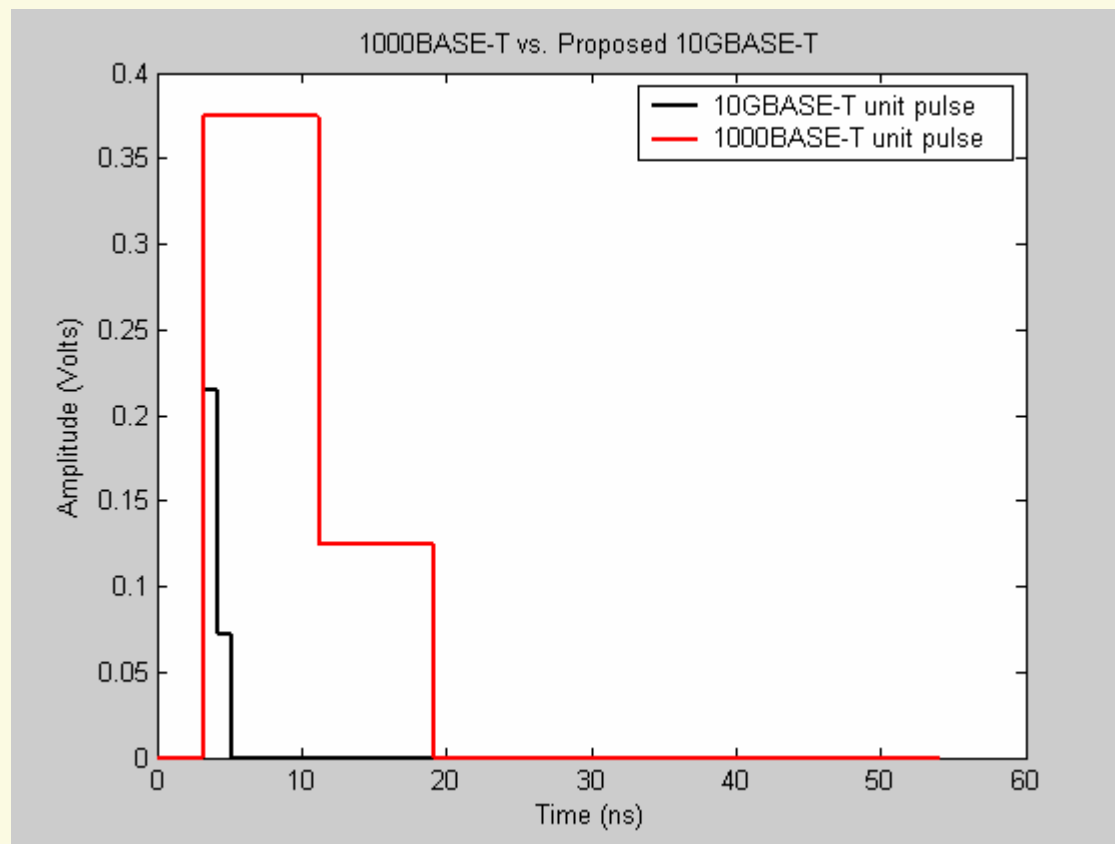


Shaping due to $(0.75+0.25D)$ Filter



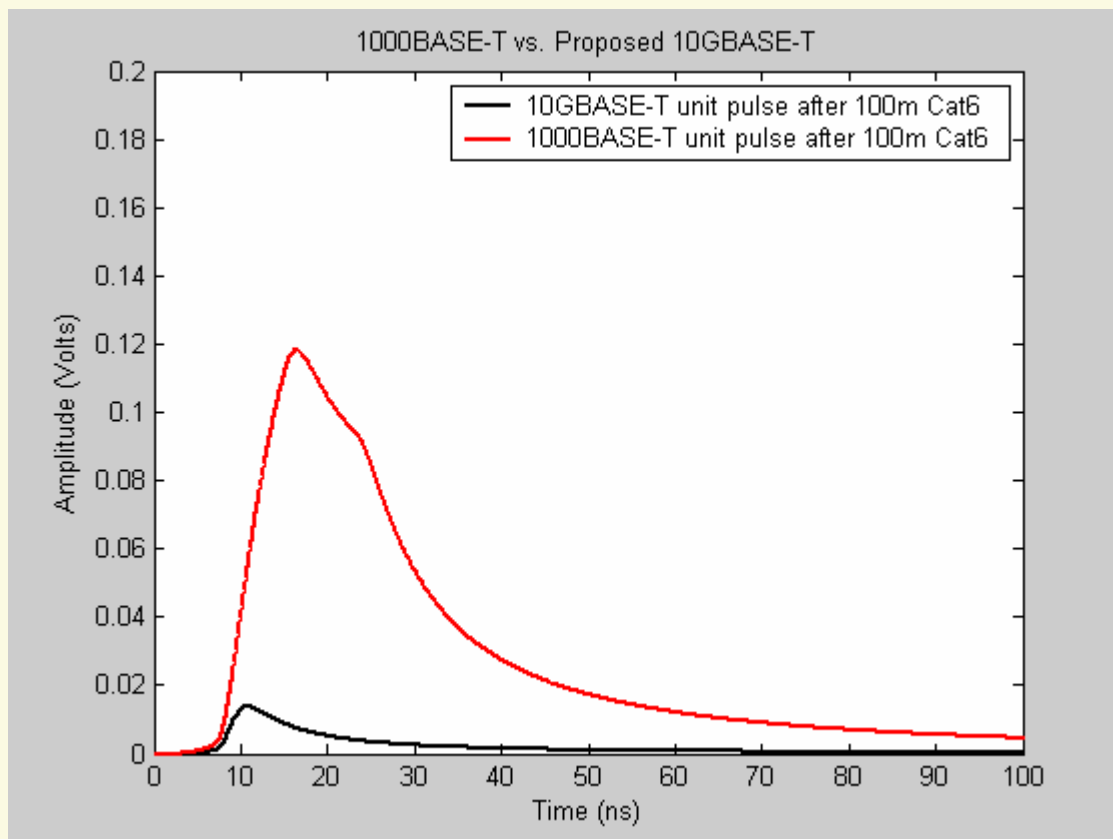


Input comparison



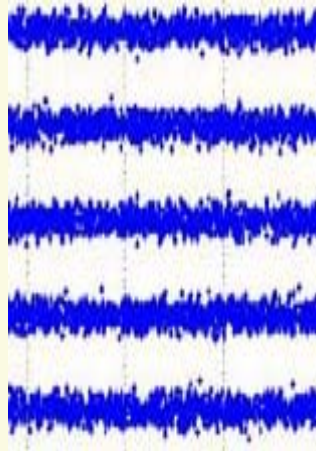


After 100m Cat6e cable:

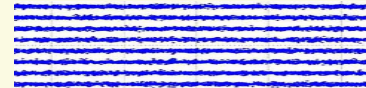




After 100m Cat6e cable:



PAM-5 eye diagram at the receiver for 1000BASE-T

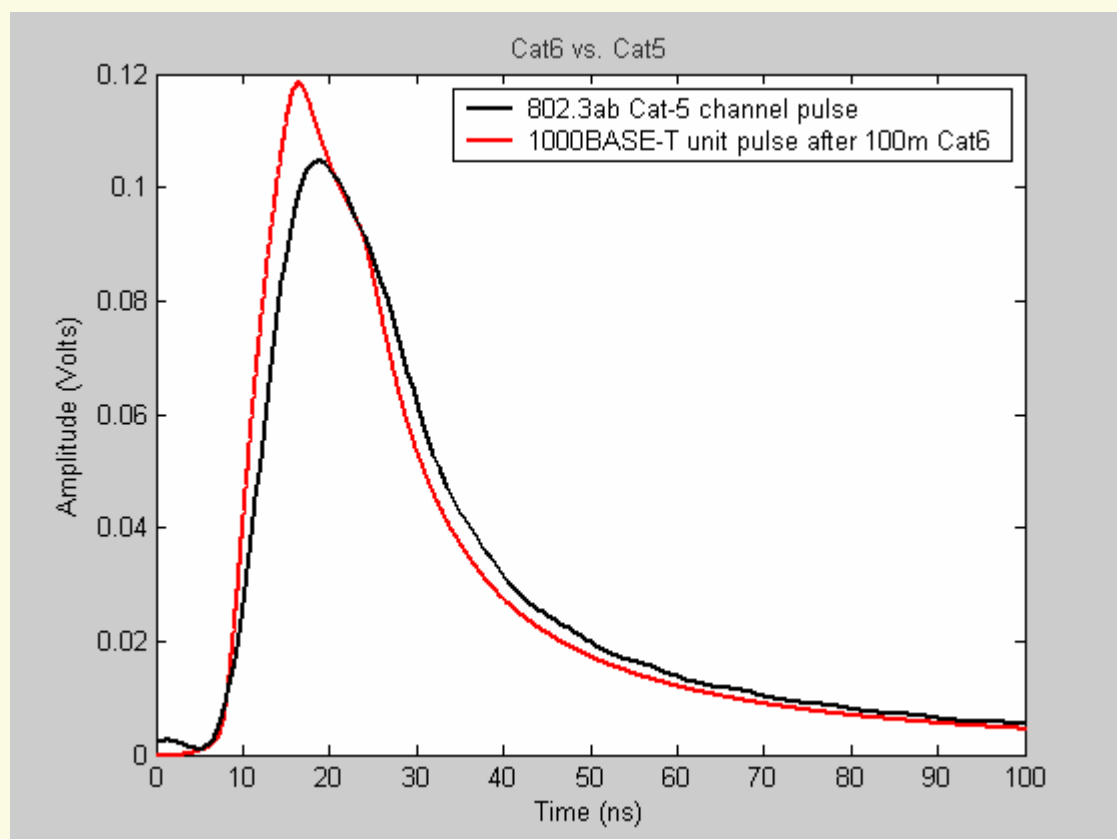


PAM-8 eye diagram at the receiver for 10GBASE-T (amplitude is to scale)

Separation between levels is 759% larger in 125Ms/s PAM5 vs. 1Gs/s PAM8

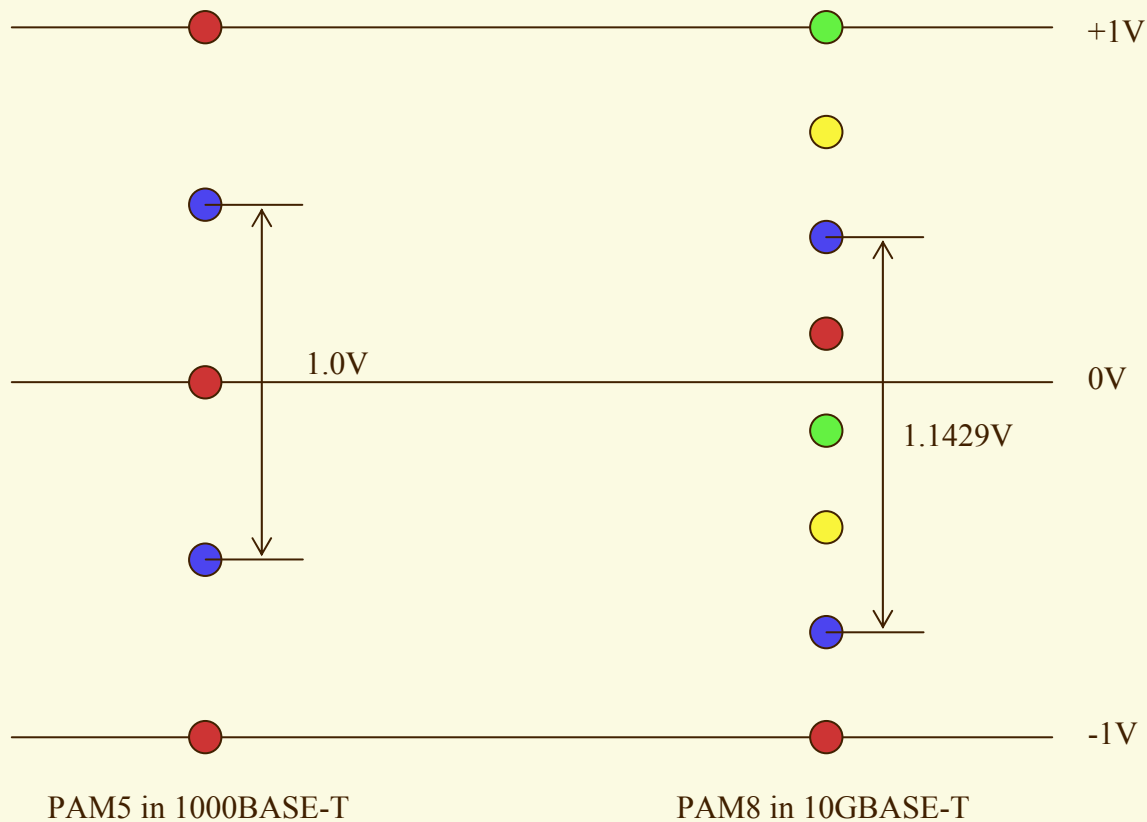


Sanity Check...



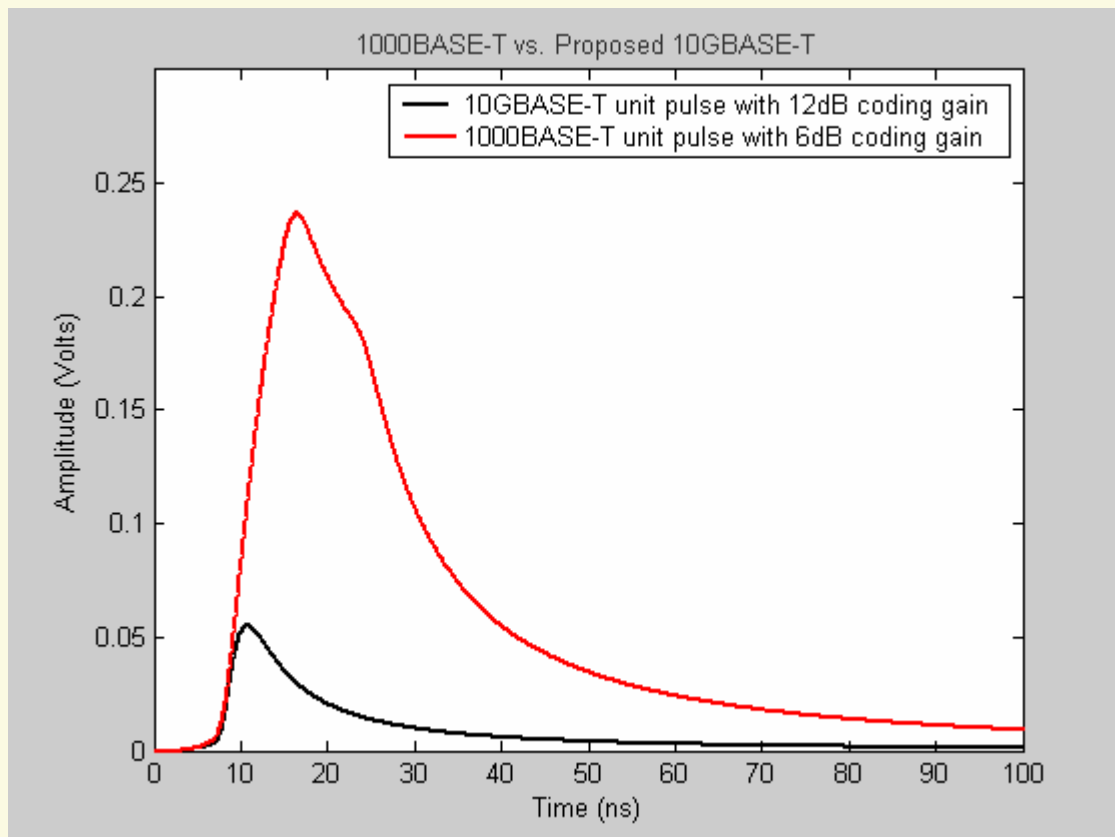


Equivalent Spacing (with coding gain)



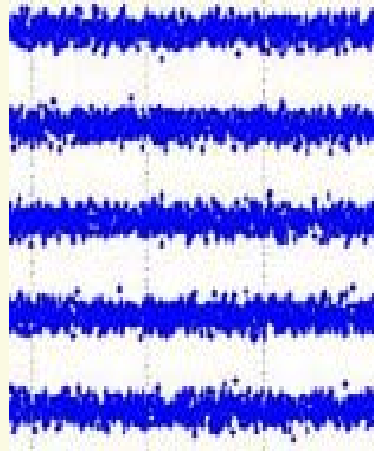


With Coding Gain

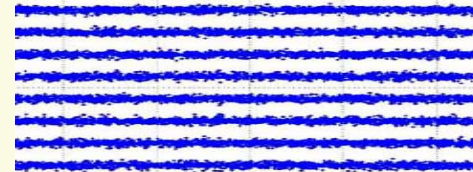




After 100m Cat6e cable + coding:



PAM-5 eye diagram at the receiver for 1000BASE-T with 6dB coding gain

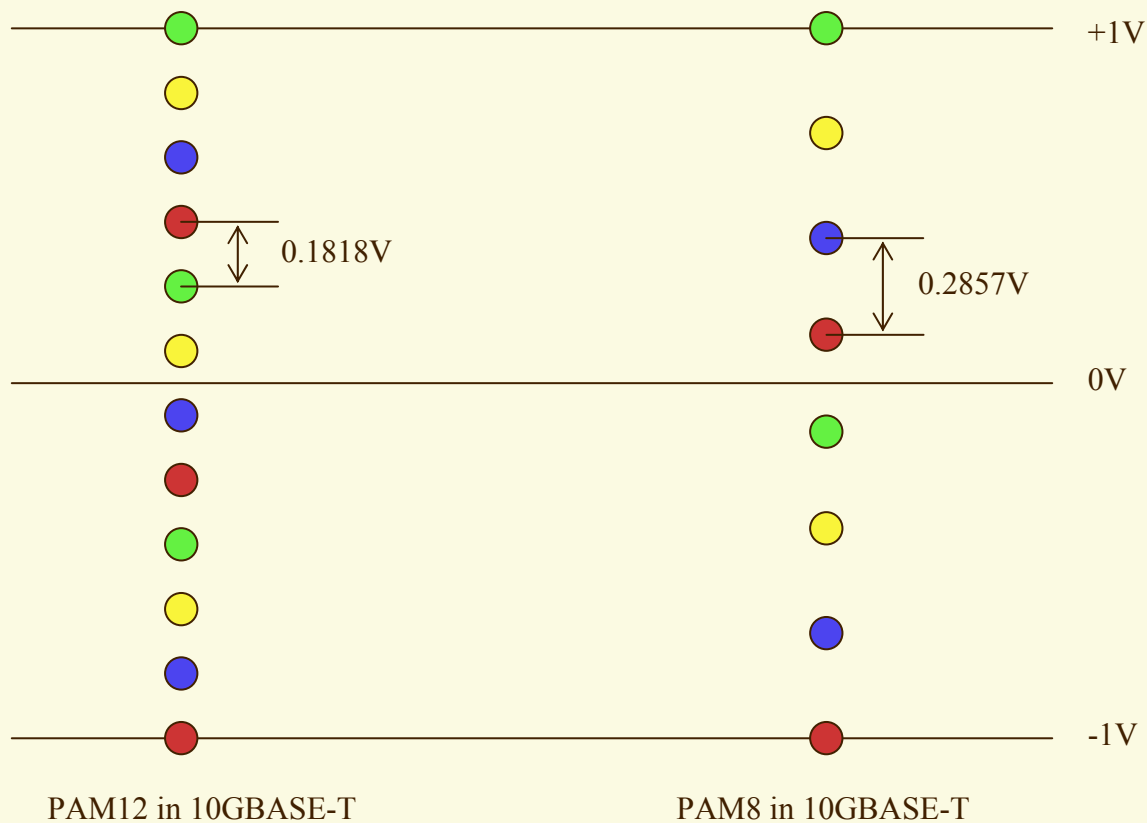


PAM-8 eye diagram at the receiver for 10GBASE-T with 12dB coding gain

Separation between levels is 329% larger in 1000BASE-T vs. LDPC 4D-PAM8

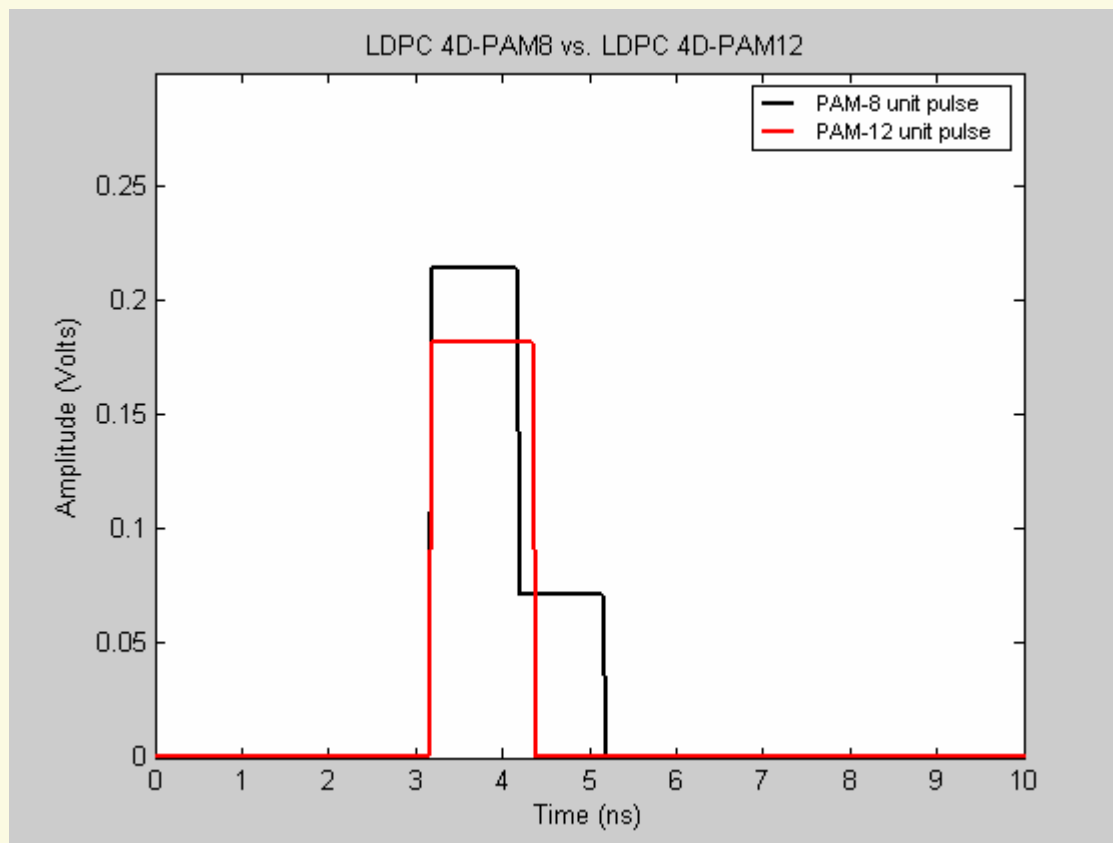


PAM8 vs. PAM12 Spacing



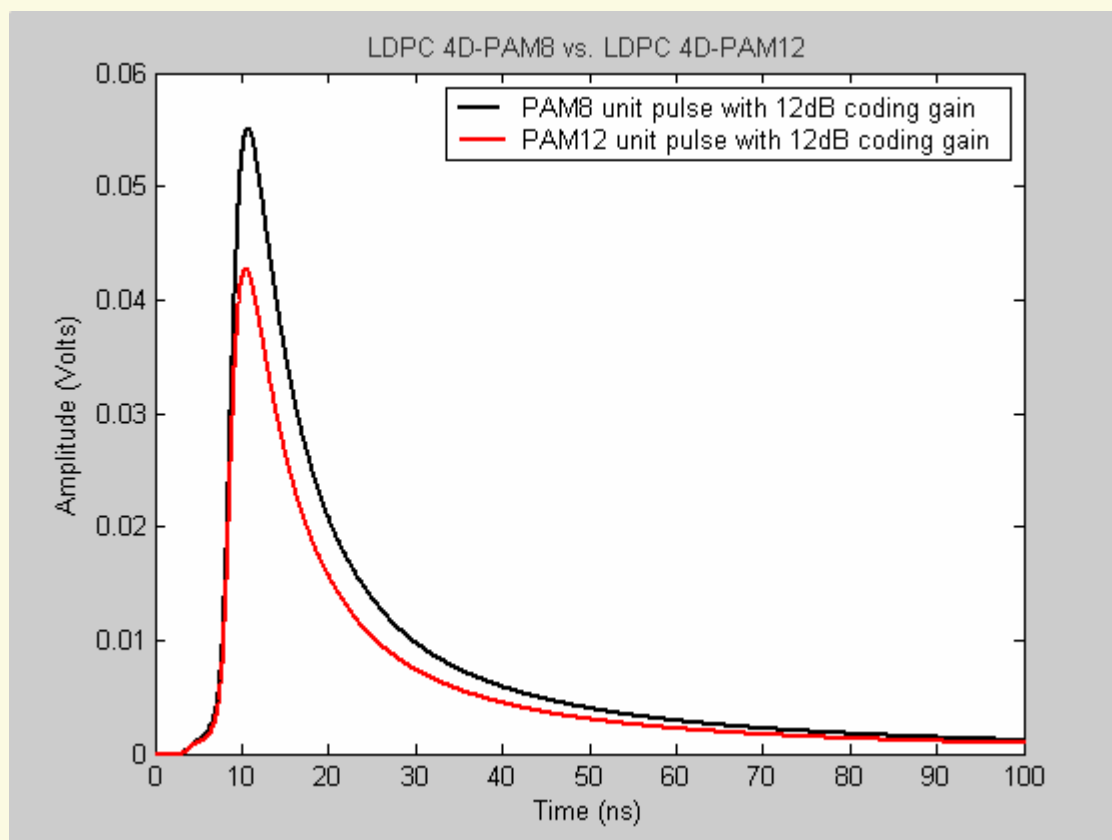


PAM8 vs. PAM12 (input)



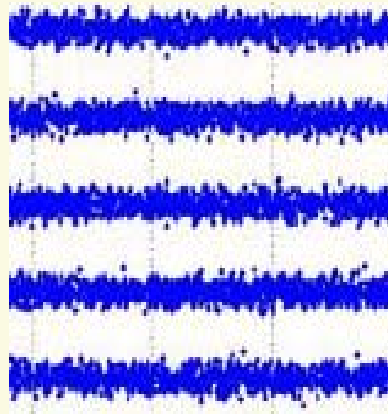


After 100m Cat6e Cable + coding:

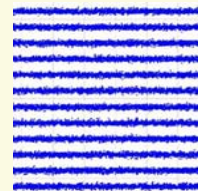




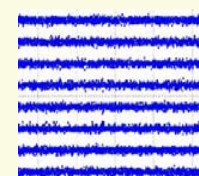
After 100m Cat6e Cable + coding:



PAM-5 eye diagram at the receiver for 1000BASE-T with 6dB coding gain



PAM-12 eye diagram at the receiver for 10GBASE-T with 12dB coding gain



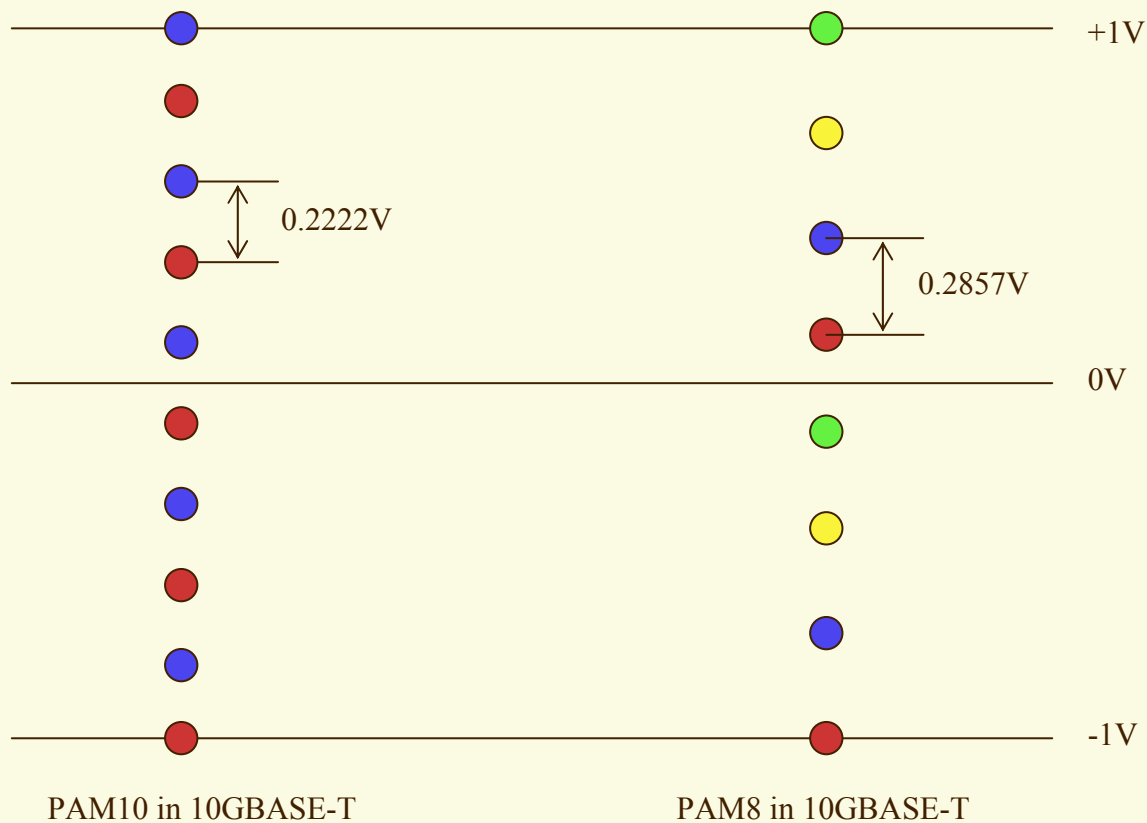
PAM-8 eye diagram at the receiver for 10GBASE-T with 12dB coding gain

Separation between levels is 453% larger in 1000BASE-T vs. LDPC 4D-PAM12

Separation between levels is 29% larger in LDPC 4D-PAM8 vs. LDPC 4D-PAM12

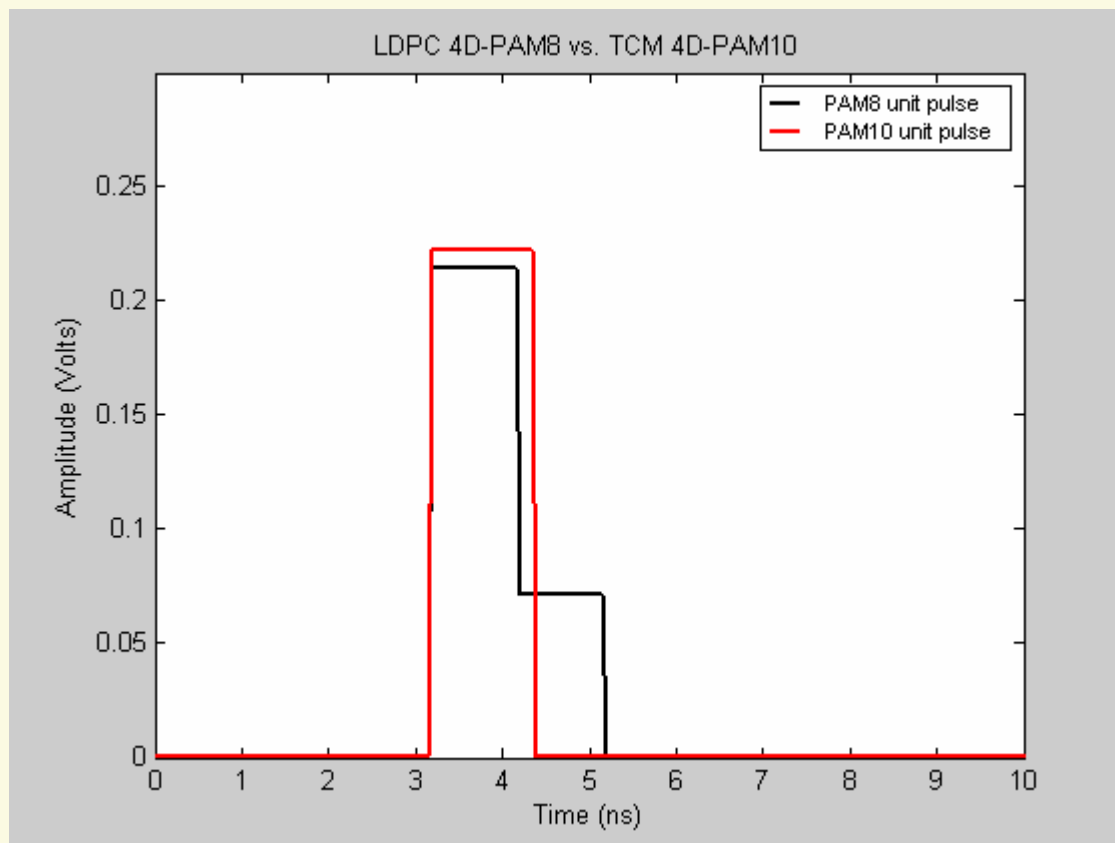


PAM8 vs. PAM10 Spacing



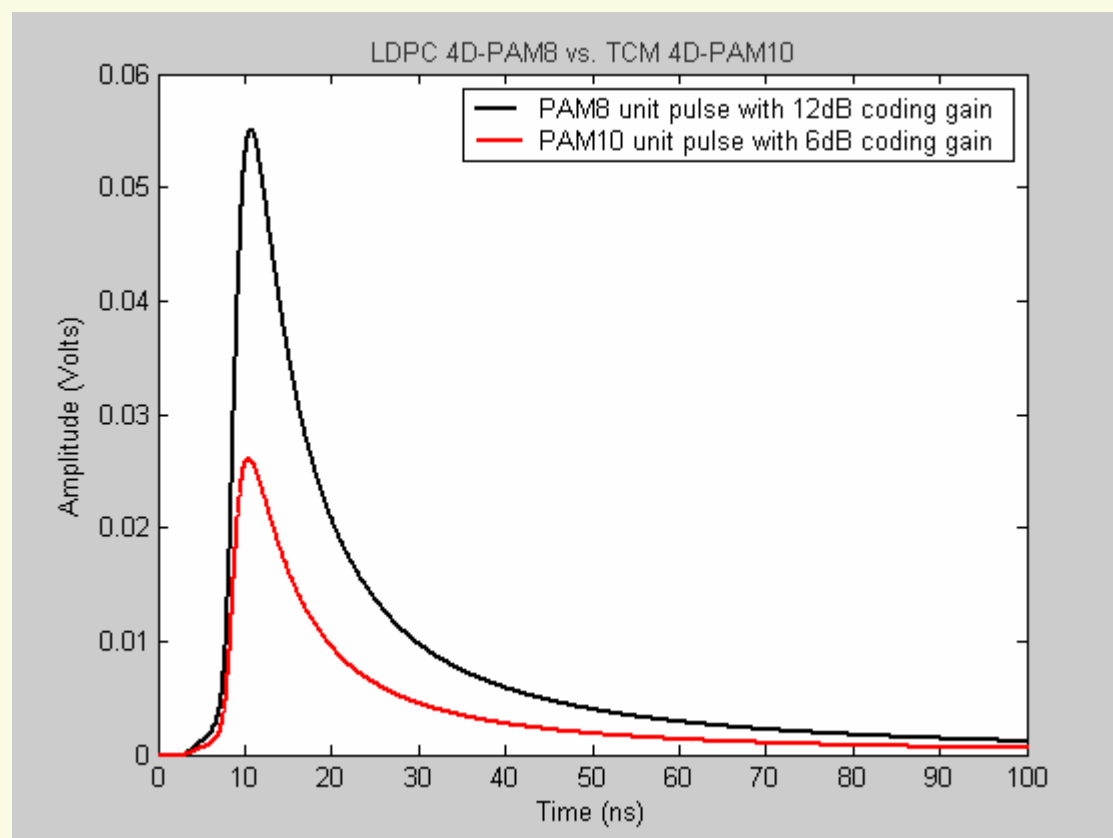


PAM8 vs. PAM10 (input)



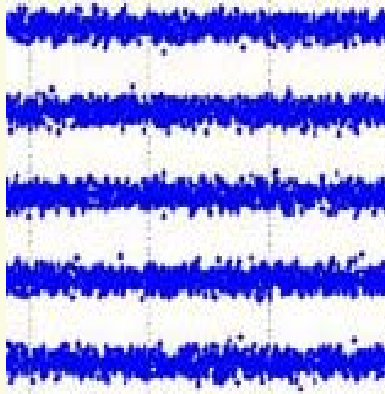


After 100m Cat6e Cable:

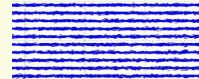




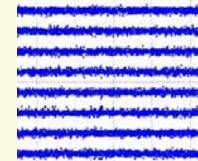
After 100m Cat6e Cable + coding:



PAM-5 eye diagram at the receiver for 1000BASE-T with 6dB coding gain



PAM-10 eye diagram at the receiver for 10GBASE-T with 6dB coding gain



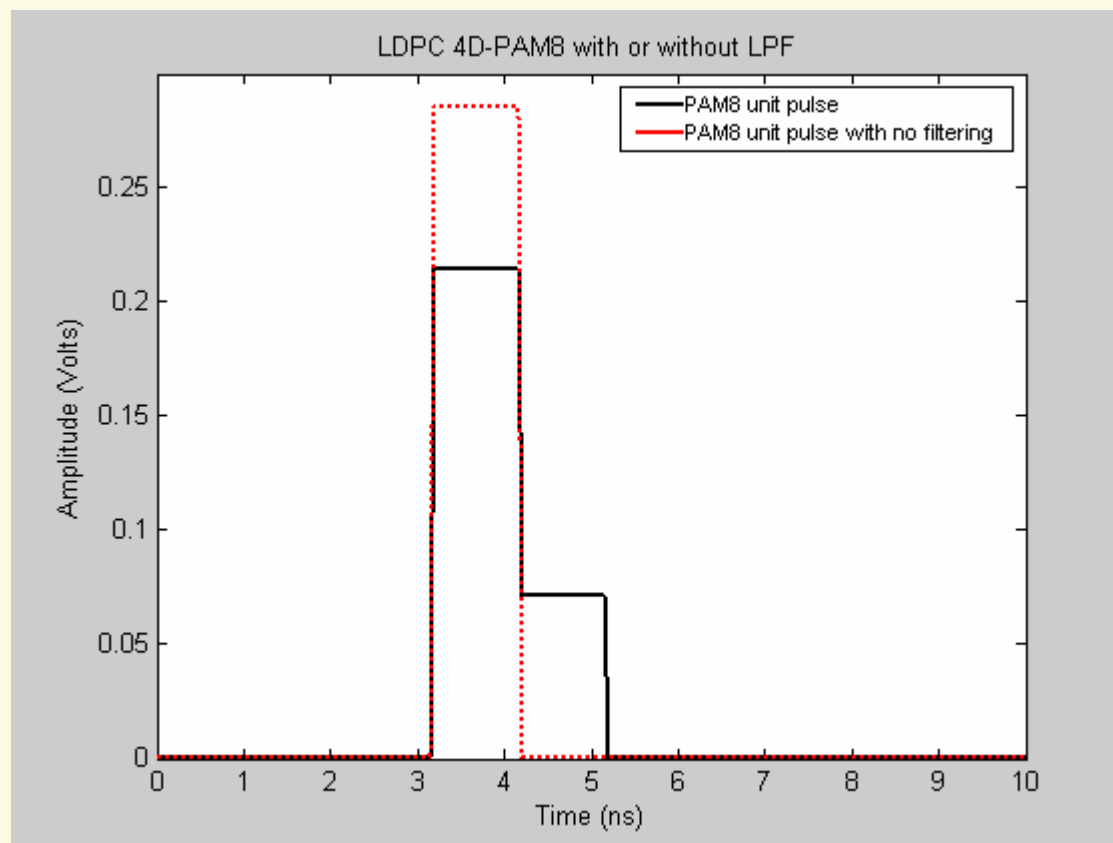
PAM-8 eye diagram at the receiver for 10GBASE-T with 12dB coding gain

Separation between levels is 805% larger in 1000BASE-T vs. TCM 4D-PAM10

Separation between levels is 111% larger in LDPC 4D-PAM8 vs. TCM 4D-PAM10

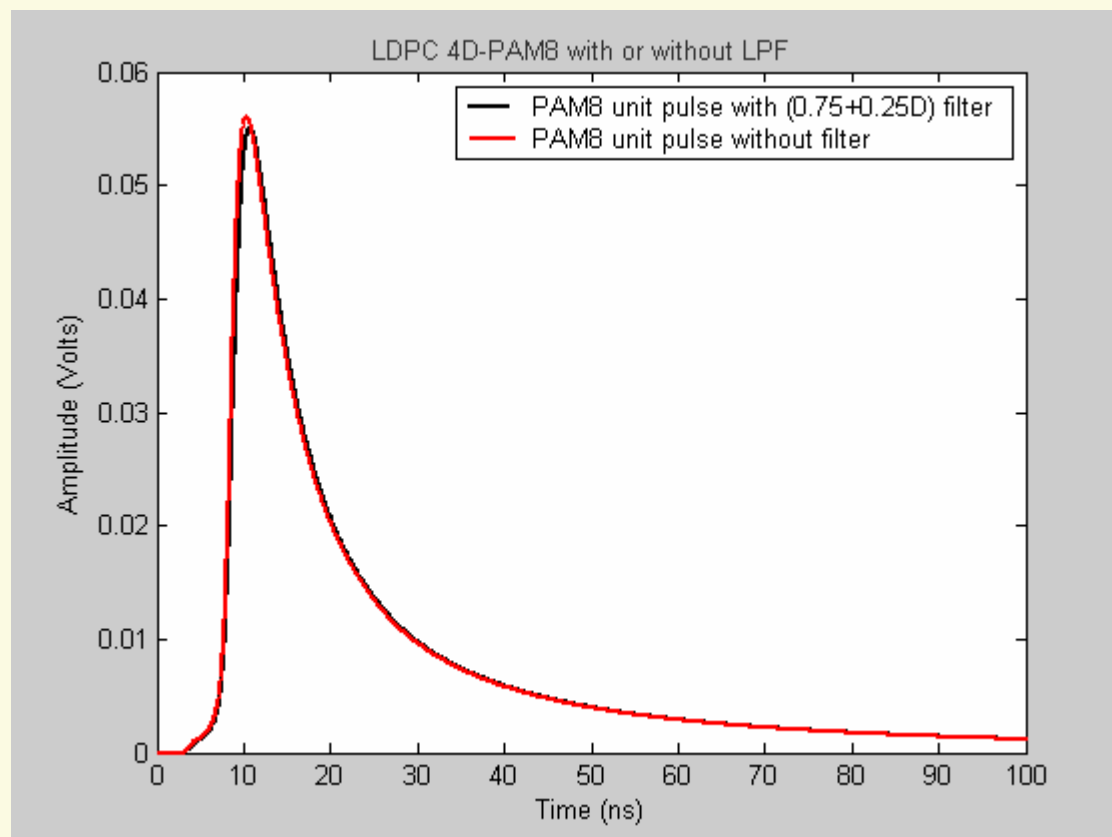


PAM8 With or Without LPF (Input)





After 100m Cat6e Cable:



LDPC 4D-PAM8 vs. LDPC OFDM



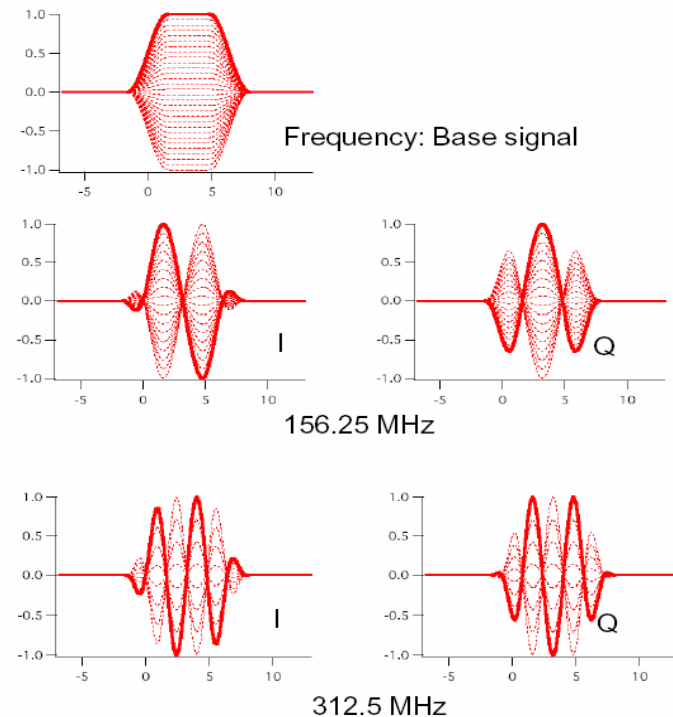
from: higuchi_1_0504.pdf, May 2004, slide 5

New proposal for OFDM signaling

Carrier frequency	Data (bits)	PAM levels
Base signal	4.9	30
156.25 MHz (I,Q)	4.2+4.2	18
312.5 MHz (I,Q)	3+3	8
469 MHz pilot signal	0	0

Total: 19.3 bits

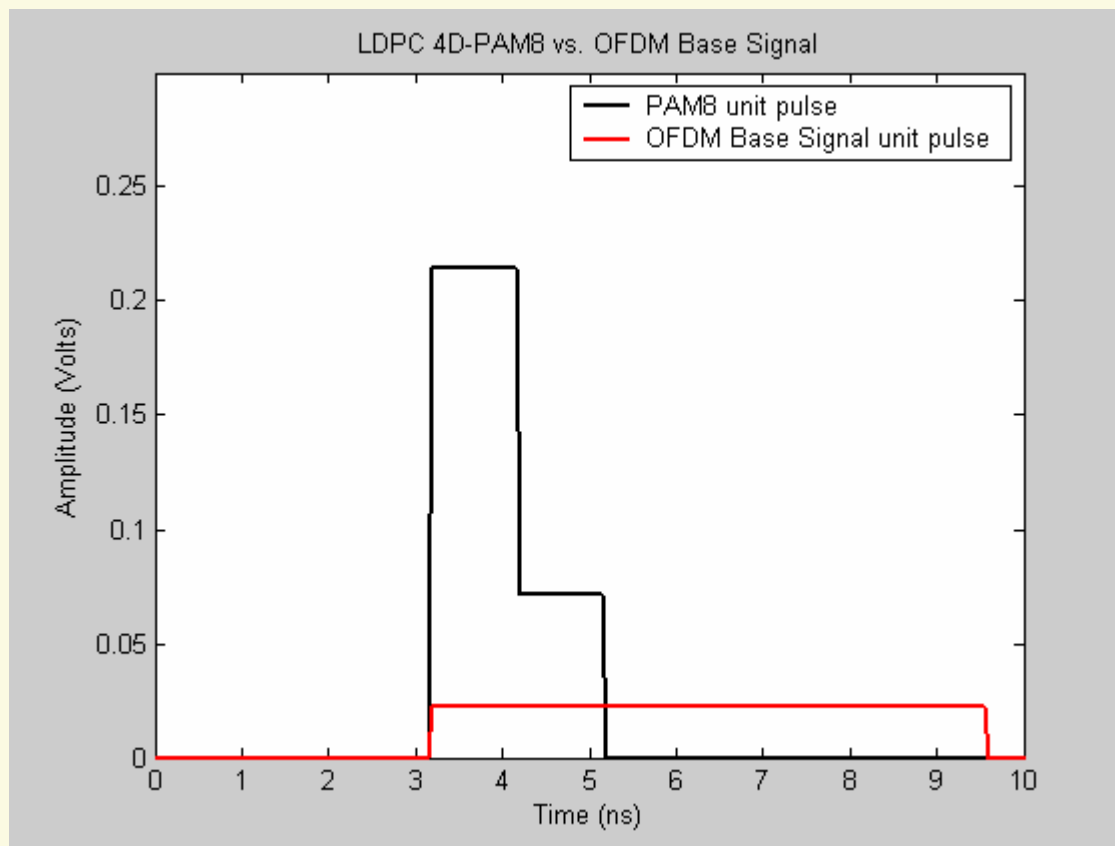
I: In-phase, Q: Quadrature-phase





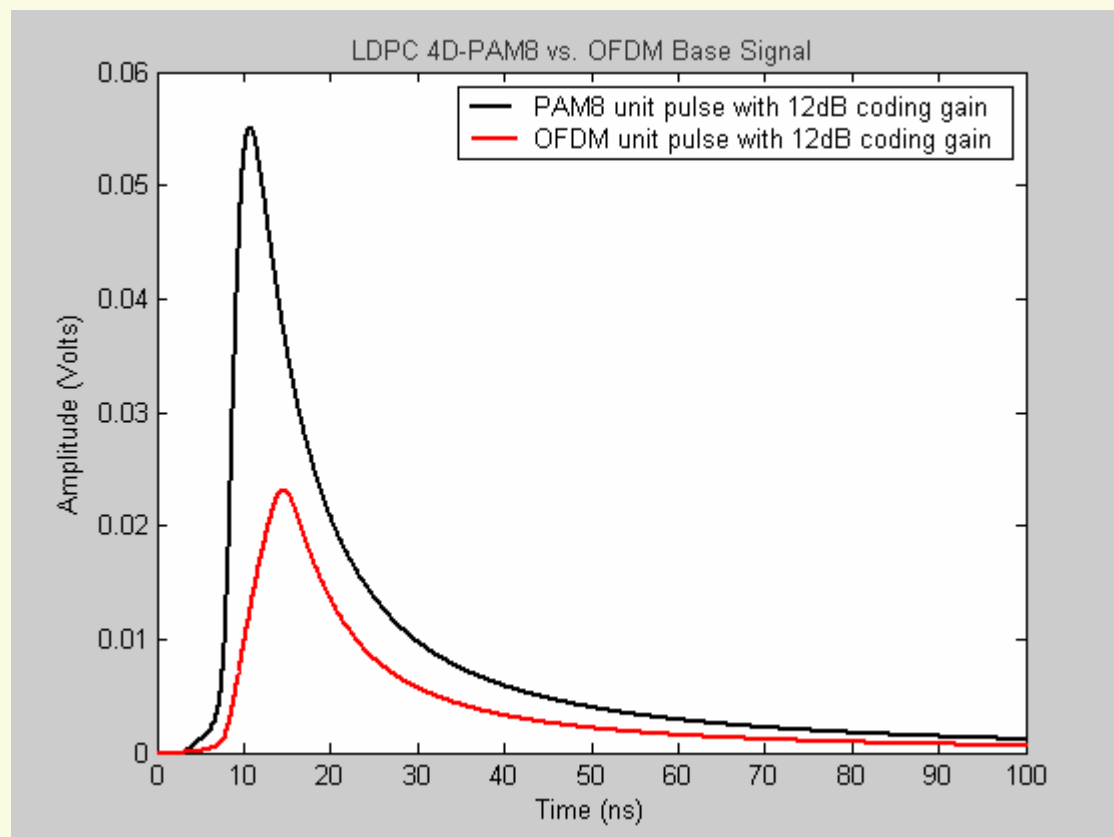
PAM8 vs. OFDM Base Signal

Height of unit pulse for OFDM Base Signal = $2.0V/3/(30-1) = 0.0221V$





After 100m Cat6e Cable:



Separation between levels is 139% larger in LDPC 4D-PAM8 vs. OFDM Base Signal



LDPC 4D-PAM8 vs. LDPC OFDM

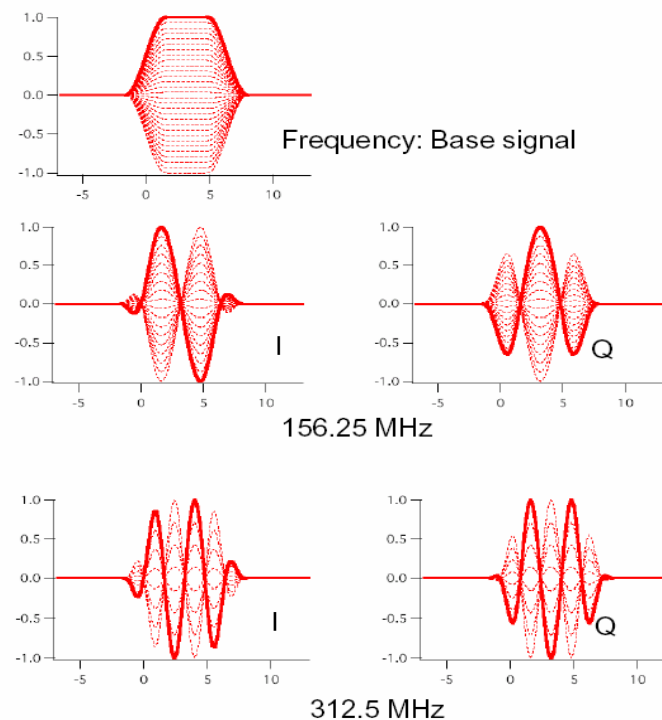
from: higuchi_1_0504.pdf, May 2004, slide 5

New proposal for OFDM signaling

Carrier frequency	Data (bits)	PAM levels
Base signal	4.9	30
156.25 MHz (I,Q)	4.2+4.2	18
312.5 MHz (I,Q)	3+3	8
469 MHz pilot signal	0	0

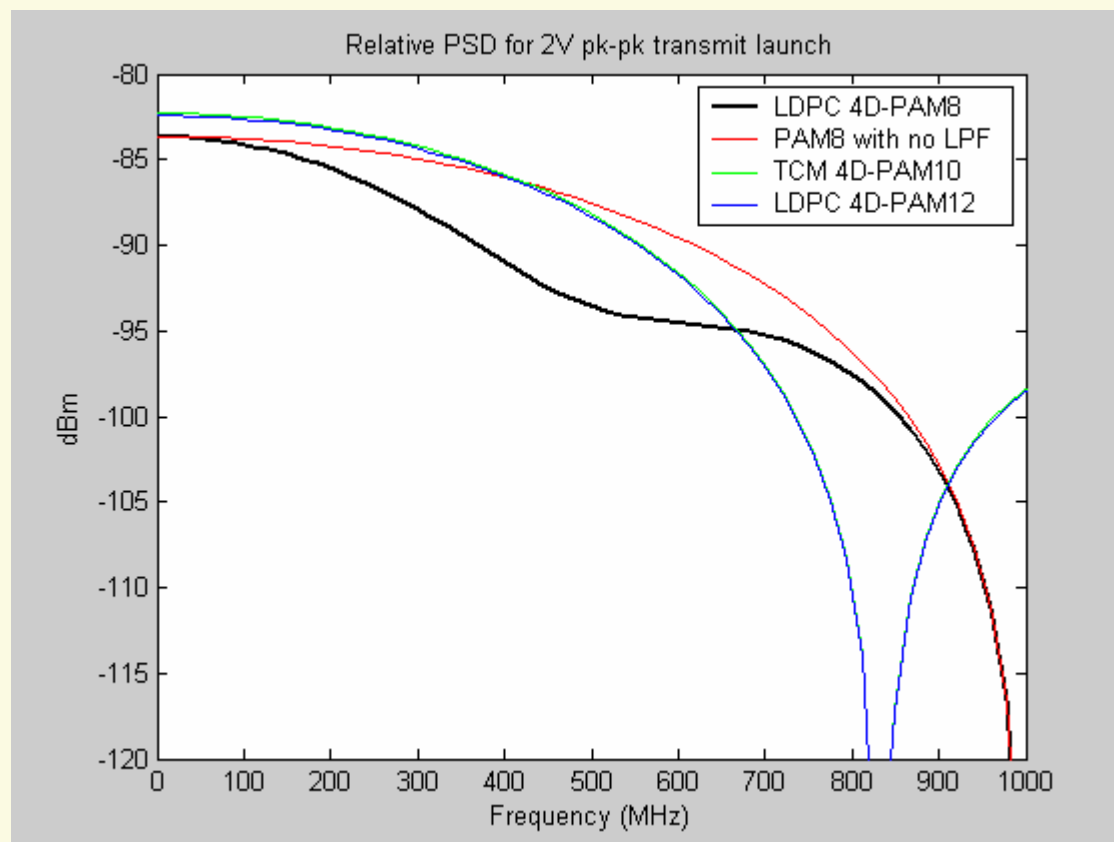
Total: 19.3 bits

I: In-phase, Q: Quadrature-phase



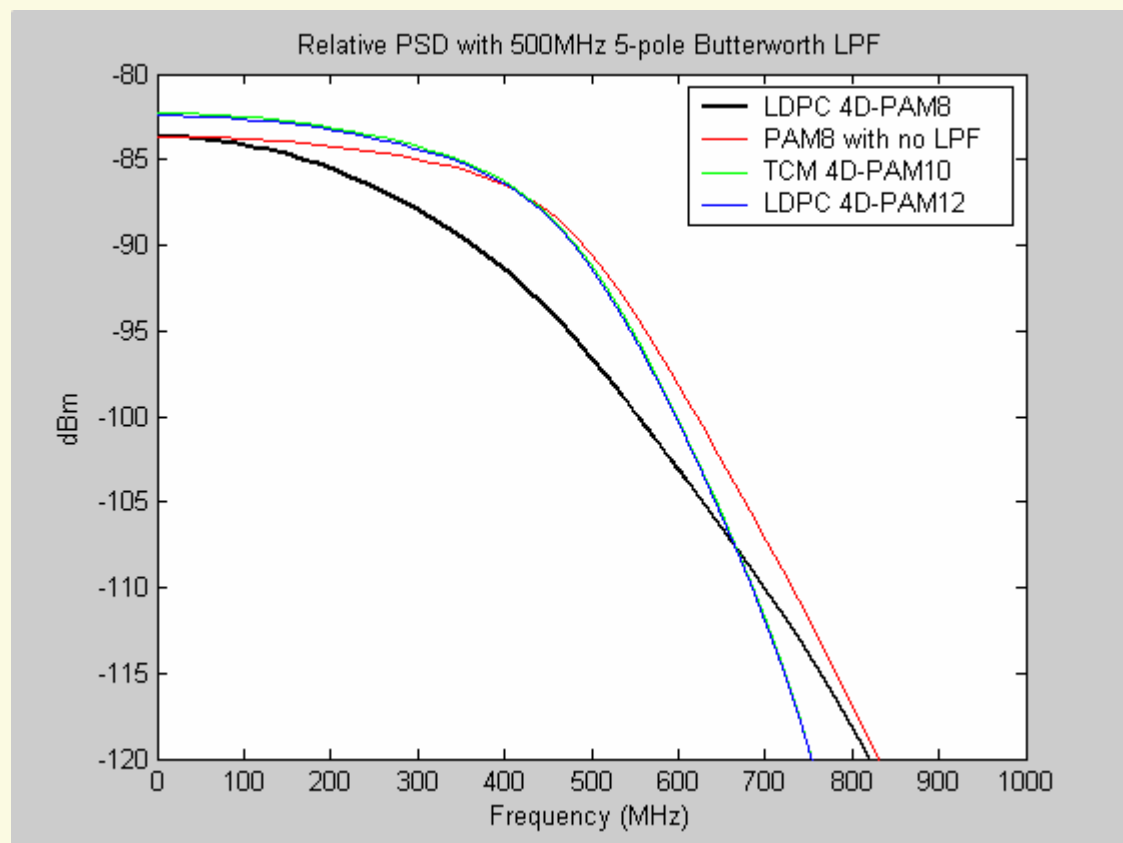


Input PSD Comparison



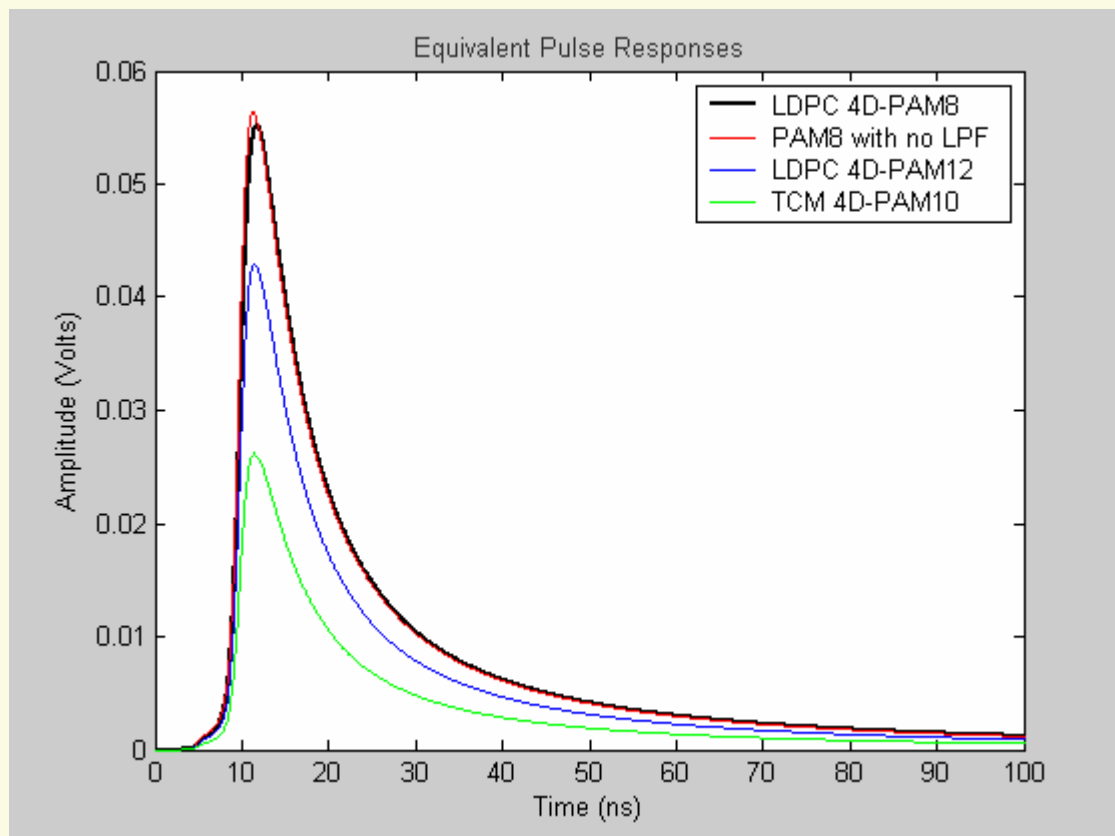


Input PSD with LPF



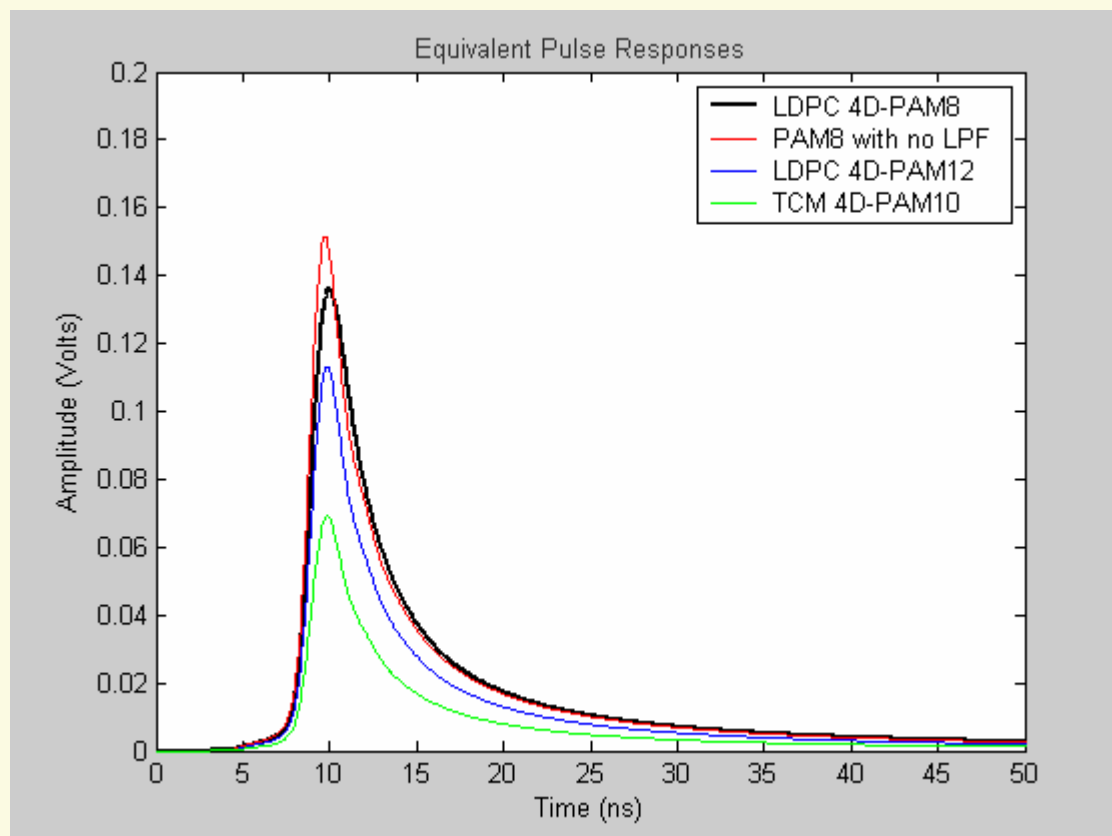


100m Pulse Responses with LPF





55m Pulse Responses with LPF





Summary Observations

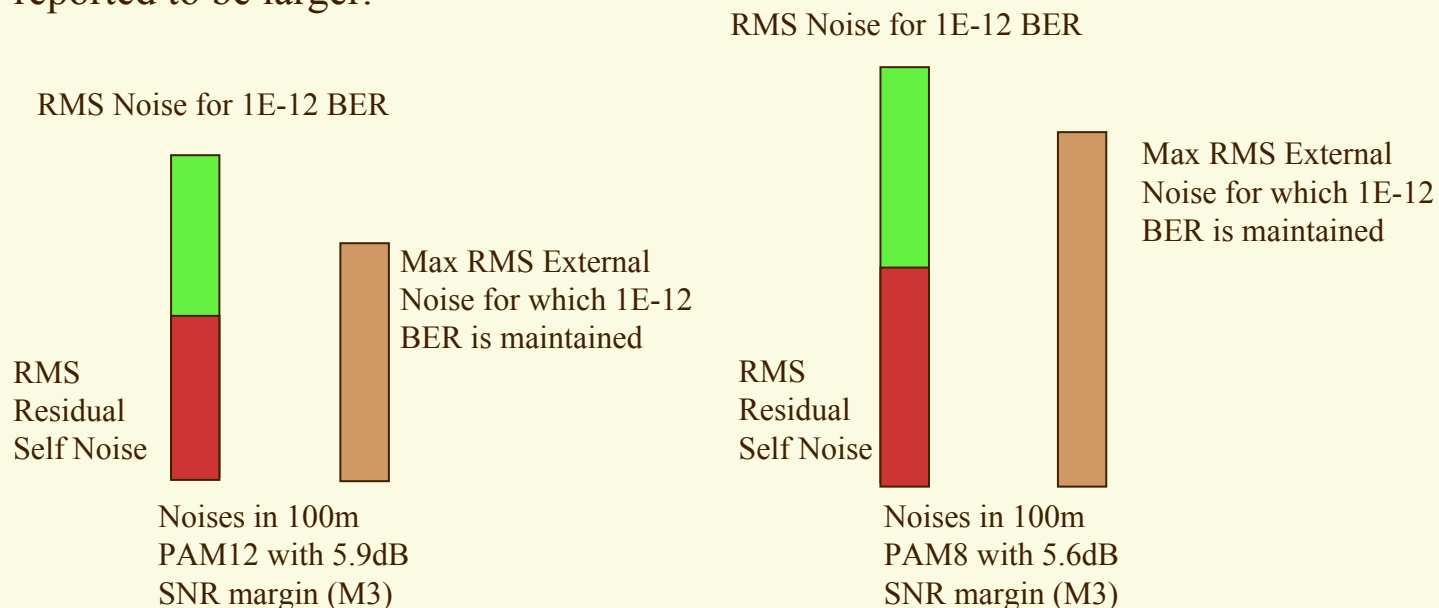
- ☞ The LDPC 4D-PAM8 Proposal results in the **LARGEST** separation of levels at the end of a cable compared to the LDPC 4D-PAM12 proposal or the TCM 4D-PAM10 proposal or the LDPC OFDM proposal, **AND**
- ☞ The LDPC 4D-PAM8 Proposal results in the **LOWEST** transmit Power Spectral Density compared to the LDPC 4D-PAM12 proposal or the TCM 4D-PAM10 proposal
 - Lowest transmit PSD implies **lowest echo** power, **lowest NEXT/FEXT** power and **lowest alien NEXT/FEXT** coupling.
- ☞ The $(0.75+0.25D)$ LPF causes negligible degradation of the received PAM8 unit pulse response while it causes a 20dB/decade slope in the high frequency energy of the transmit PSD.



SNR Margins Explained

☞ SNR Margins are always reported relative to the separation of levels of the system

- If residual self-noise shrinks more than the separation of levels, the SNR margin is reported to be larger.



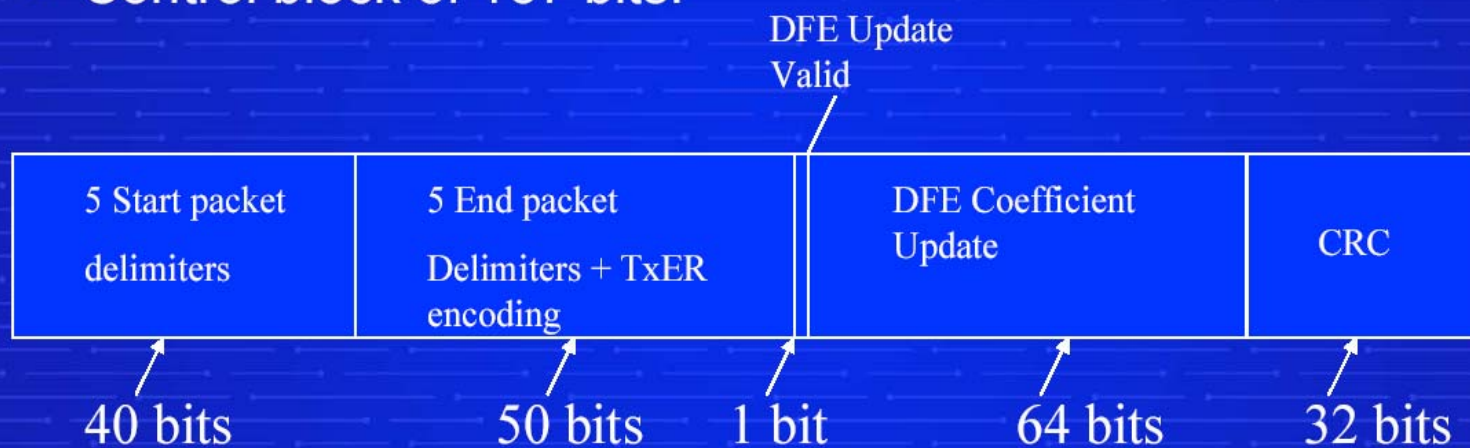


Physical Coding Sublayer (PCS)

from: rao_1_1103.pdf, November 2003, slide 19

PCS Encoding

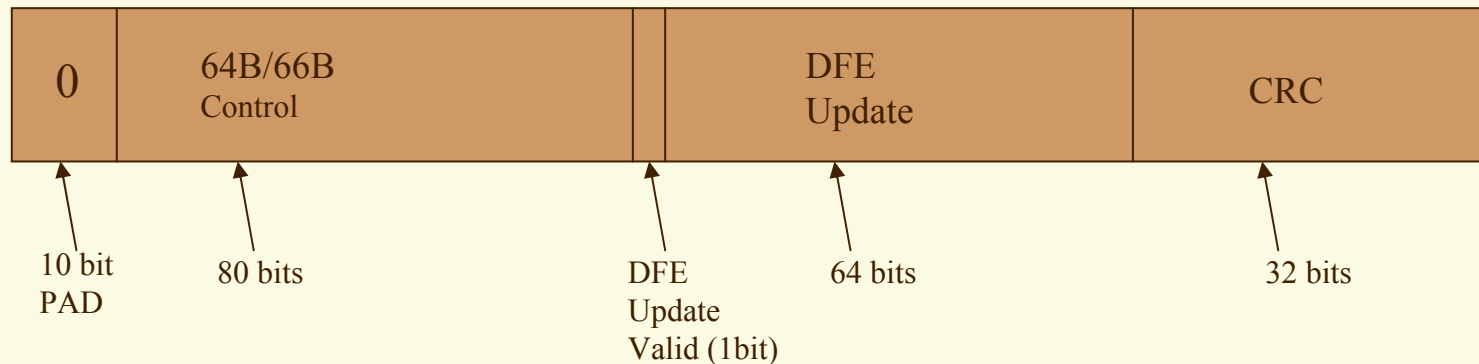
- Data words transmitted as is in each block of 256 4D symbols
- Control block of 187 bits:





Refinement of PCS

- ❏ Data words transmitted after 64B/66B encoding in 256 4D symbols
- ❏ The control word of 187 bits is split as





Startup

from: rao_1_1103.pdf, November 2003, slide 20

Startup

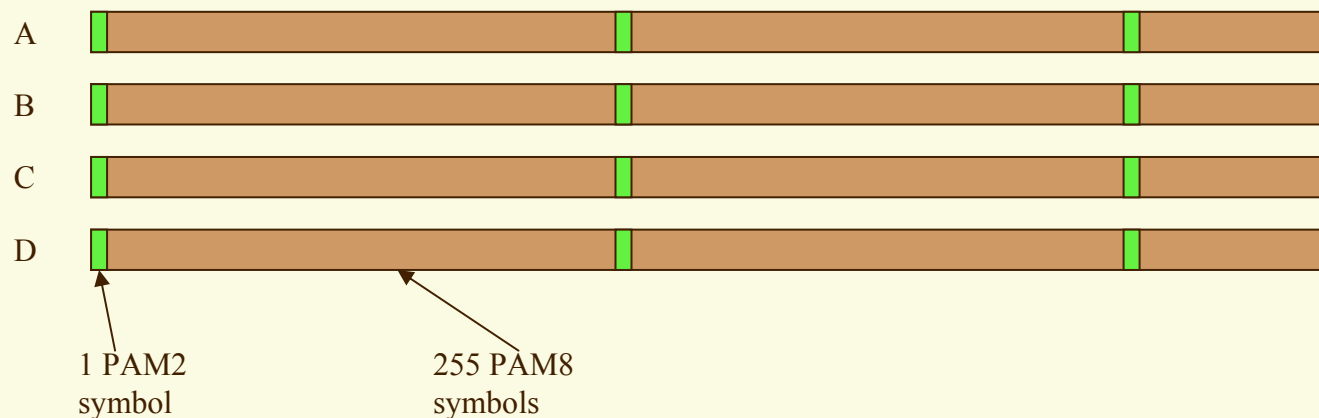
- Initial startup using 2-level transmission
 - Corresponds to +/- 4 level.
 - Recover timing and adaptive filter coefficients
 - Establish polarity correction, pair swap
 - Establish 256-symbol block boundaries
 - Exchange initial DFE coefficients
 - Switch to Block coded transmission.





Framing

- Use 8 of the zero PAD bits in the control word to convert 4 PAM8 symbols into PAM2 symbols
 - Use +/-4 as the PAM2 levels
- Transmit a PAM2 symbol on each pair at the start of a 256 symbol frame





Power Backoff

- ☞ Alien ELFEXT coupling varies by 10dB between 0m and 100m
 - Ref: koeman_1_0304.pdf, March 2004, page 24
- ☞ Recommend transmit levels change by approx;. 10dB from 0m to 100m
 - 0.75V pk-pk at 0m to 2.5V pk-pk at >80m in a few discrete steps (e.g., 0.75V, 1V, 1.5V, 2V, 2.5V at 20m,40m,60m,80m)
- ☞ Transmit levels to be determined during auto-negotiation and fixed between link partners
 - Exact mechanism of line length determination and transmit level resolution TBD.
 - Both link partners use the same pk-pk transmit voltage during 10GBASE-T transmission.



Concluding Remarks

- ☞ The LDPC 4D-PAM8 proposal is optimum for addressing the most pressing problem in 10GBASE-T – the excessive insertion loss of a 100m twisted pair line at high frequencies.
 - It achieves at least 29% larger separation of levels than the nearest competing proposal
- ☞ The LDPC 4D-PAM8 proposal is based on very simple block encoding and framing principles
 - Data transmitted in blocks of 320bytes or 80 XGMII words
 - PCS Encoding in blocks of 256 symbols – power of 2 block size allows for efficient FFT based signal processing
 - Symbol clock is an integer sub-multiple of the data rate (1Gs/s)
 - Robust SSD/ESD and control signaling
- ☞ The majority of other 10GBASE-T proposals have incorporated key ingredients of the LDPC 4D-PAM8 proposal
 - 12dB Co-set Partitioning, LDPC Block Encoding, TH Pre-Coding



Concluding Remarks

- ☞ Compared to the LDPC 4D-PAM8 proposal, the LDPC 4D-PAM12 proposals have
 - Degraded separation of levels at the receiver
 - Symbol frequency of 820Ms/s that is not a simple sub-multiple of the data rate
 - Complex framing requirement
 - SSD/ESD and Control signals that are not better protected than normal data.
 - More analog precision requirement
- ☞ Compared to the LDPC 4D-PAM8 proposal, the TCM 4D-PAM10 proposal has
 - Excessively degraded separation of levels at the receiver
 - SSD/ESD and Control signals that are not better protected than normal data.
- ☞ Compared to the LDPC 4D-PAM8 proposal, the PAM8 with No Filter proposal has
 - Degraded emissions performance in the 70-500MHz range for little added benefit in the separation of levels
- ☞ Compared to the LDPC 4D-PAM8 proposal, the LDPC OFDM proposal has
 - Excessively degraded separation of levels at the receiver