Refinements of the LDPC 4D-PAM8 proposal

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Outline

- **Main features of LDPC 4D-PAM8 proposal**
  - 12dB Co-set Partitioning
  - Tomlinson-Harashima Pre-coding
  - (2048, 1723) RS-LDPC Block Encoding
- **Using 10GBASE-R (Clause 49) 64B/66B PCS Encoding**
  - (2048, 1605) RS-LDPC block code?
- **Tx+Rx Latency**
  - Lower latency LDPC block code?

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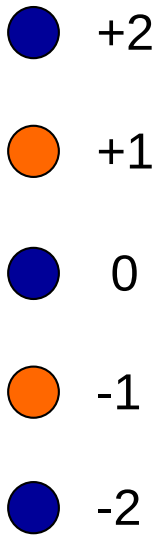
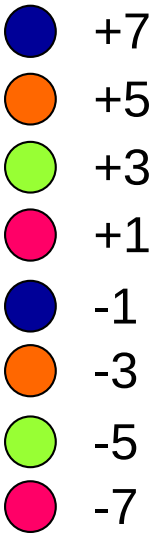
12dB Co-set Partitioning



1000BASE-T 4D PAM-5



10GBASE-T 4D PAM-8

- **Symbols in the same co-set are not protected by the Error Correcting Code**
  - re-use of 6dB co-set partitioning of 1000BASE-T TCM code will severely degrade robustness of 10GBASE-T solution
- **12dB co-set partitioning is a must for 10GBASE-T**

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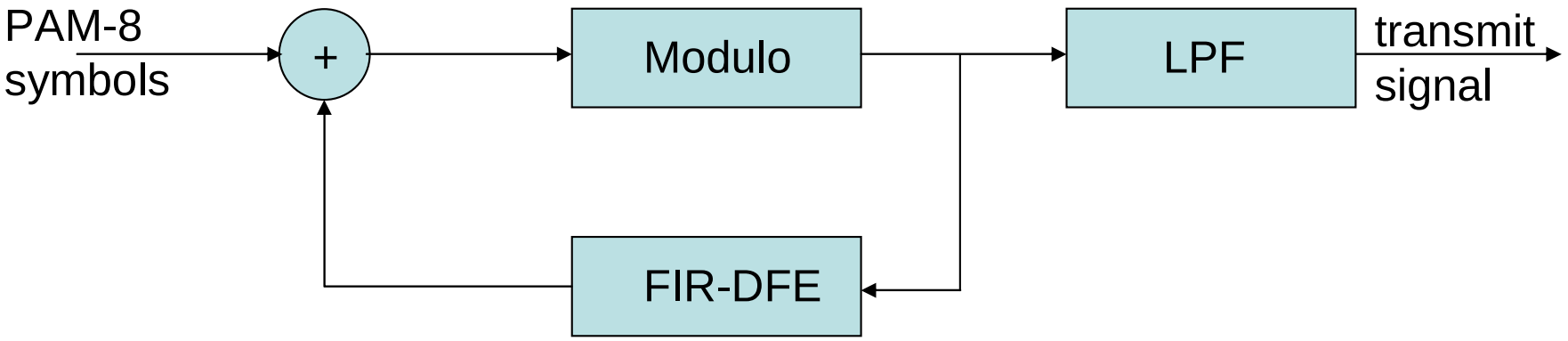
Tomlinson-Harashima Pre-coding



- **FIR-DFE coefficients are programmed by link partner during start-up**
  - can eliminate the provision in the proposal for "updating" DFE coefficients if the effect of environmental variations on the cabling parameters are negligible.
- **Can be used to reduce precision requirement of the receiver Analog Front End by > 10dB.**
  - T-H pre-coding is essential to achieve cost-effective 10GBASE-T solutions.
- **Choose LPF parameters to ease emissions compliance of 10GBASE-T system**
  - (0.75 + 0.25D) filter used in 1000BASE-T is a viable candidate.

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(2048,1723) RS-LDPC Encoding

- **Achieves excellent coding gain with relatively low latency processing**
  - simulations showed > 9.4dB coding gain over uncoded PAM-8 at 1E-11 error rate.
  - assuming systematic encoder, XGMII-MDI Tx latency is less than 0.25us
  - assuming 256-symbol block processing, MDI-XGMII Rx latency is less than 0.75us.
- **Naturally lends itself to a "Power of 2" (256=2^8 symbols) block processing**
  - Block processing is essential for reducing complexity of receiver
  - Power of 2 block processing facilitates use of well-known Fast Fourier Transform techniques in the receiver
- **Concatenated RS+TCM codes cannot match the "Low Latency + High Coding gain" combination offered by LDPC code**
  - Need several microseconds of RS inter-leaver latency in both Tx and Rx to overcome "error bursts" in the TCM decoder

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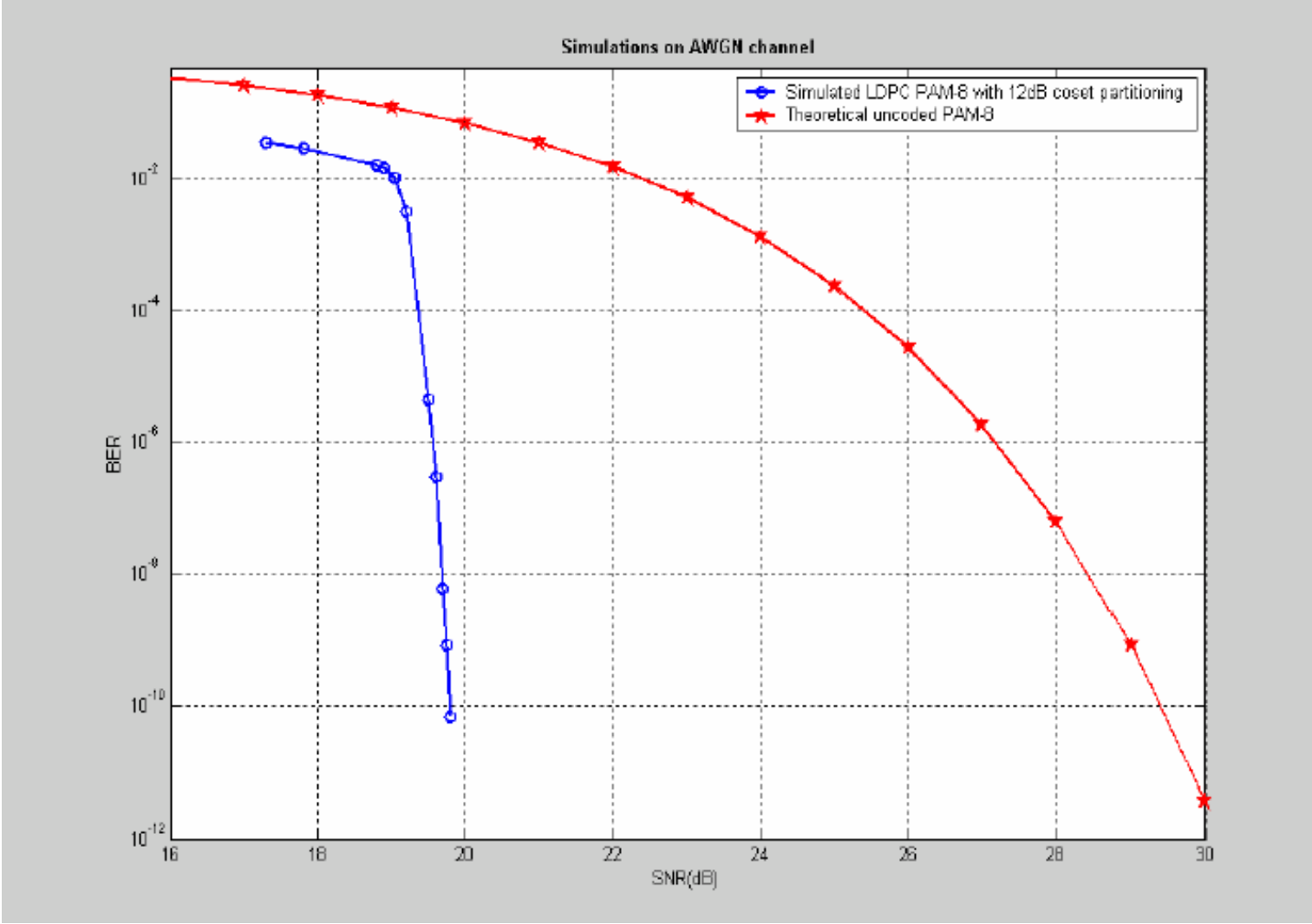
Simulation results (from rao_1_1103.pdf)



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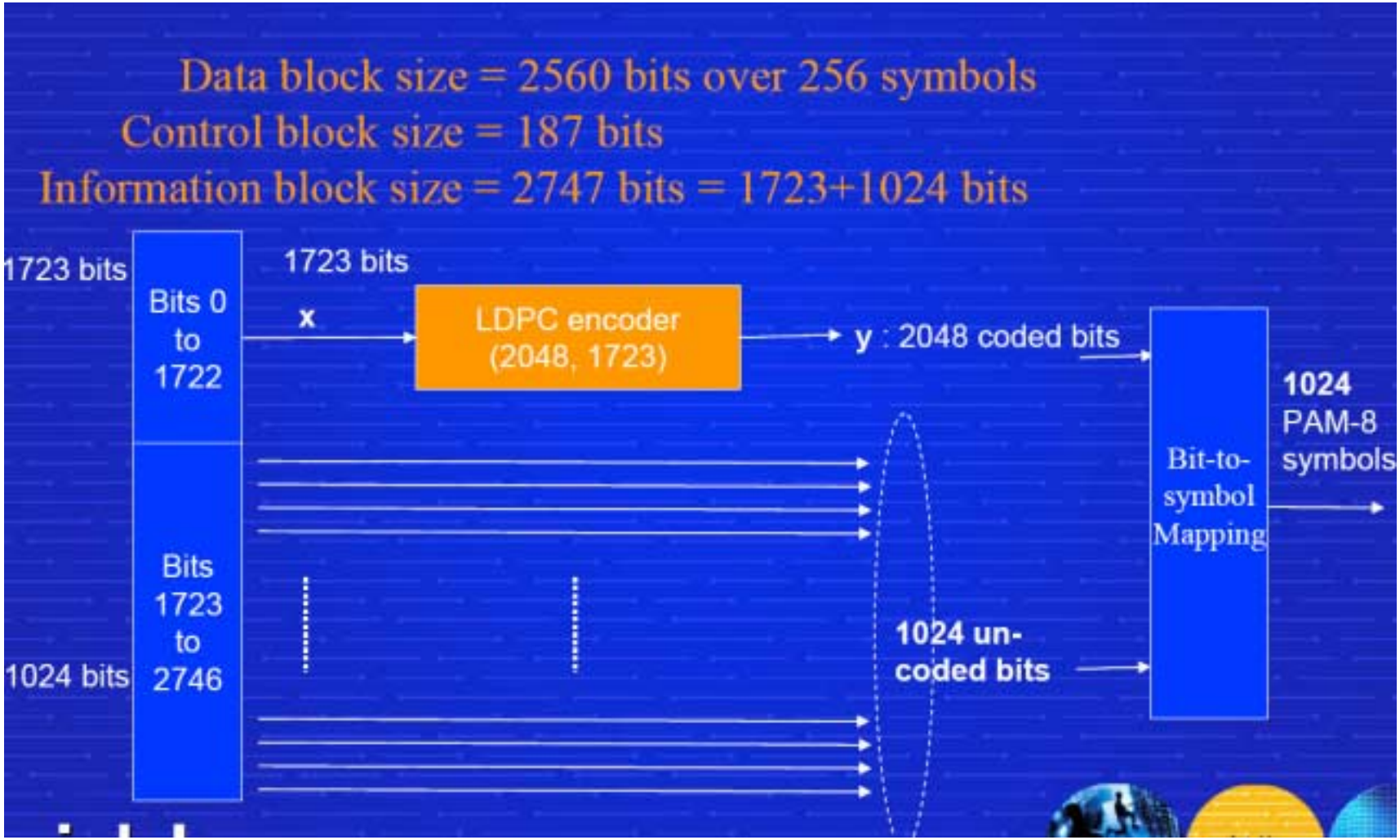
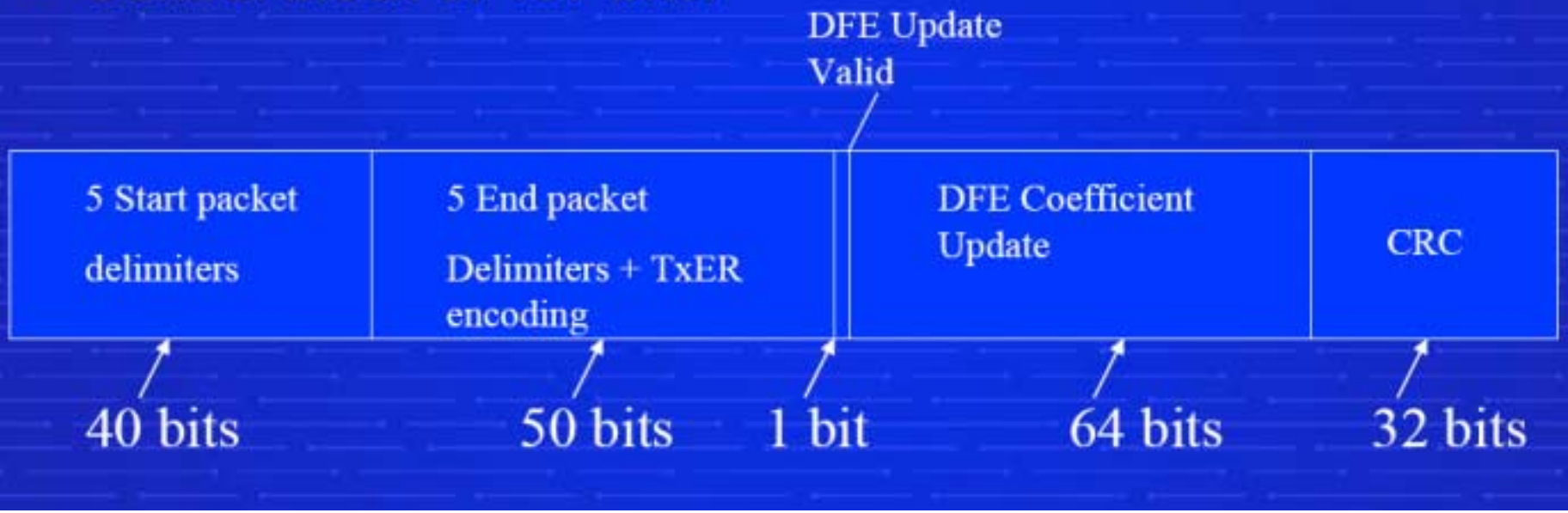
LDPC coder (from rao_1_1103.pdf)



Control coding (from rao_1_1103.pdf)

- Data words transmitted as is in each block of 256 4D symbols
- Control block of 187 bits:



Using 64B/66B 10GBASE-R PCS

- **10GBASE-R (Clause 49) has already specified a 64B/66B PCS encoder to encapsulate frame delimiter information**
  - Re-use will result in an 80-bit frame delimiter overhead for a 256 symbol block, which is less than the 90-bit overhead assumed in proposal
- **If DFE update is deemed to be not necessary**
  - Can pad the remaining bits appropriately to achieve some “shaping gain” for the encoding
  - Alternately, can reduce the frame delimiter overhead to 40-bits and increase the number of check nodes in the LDPC code

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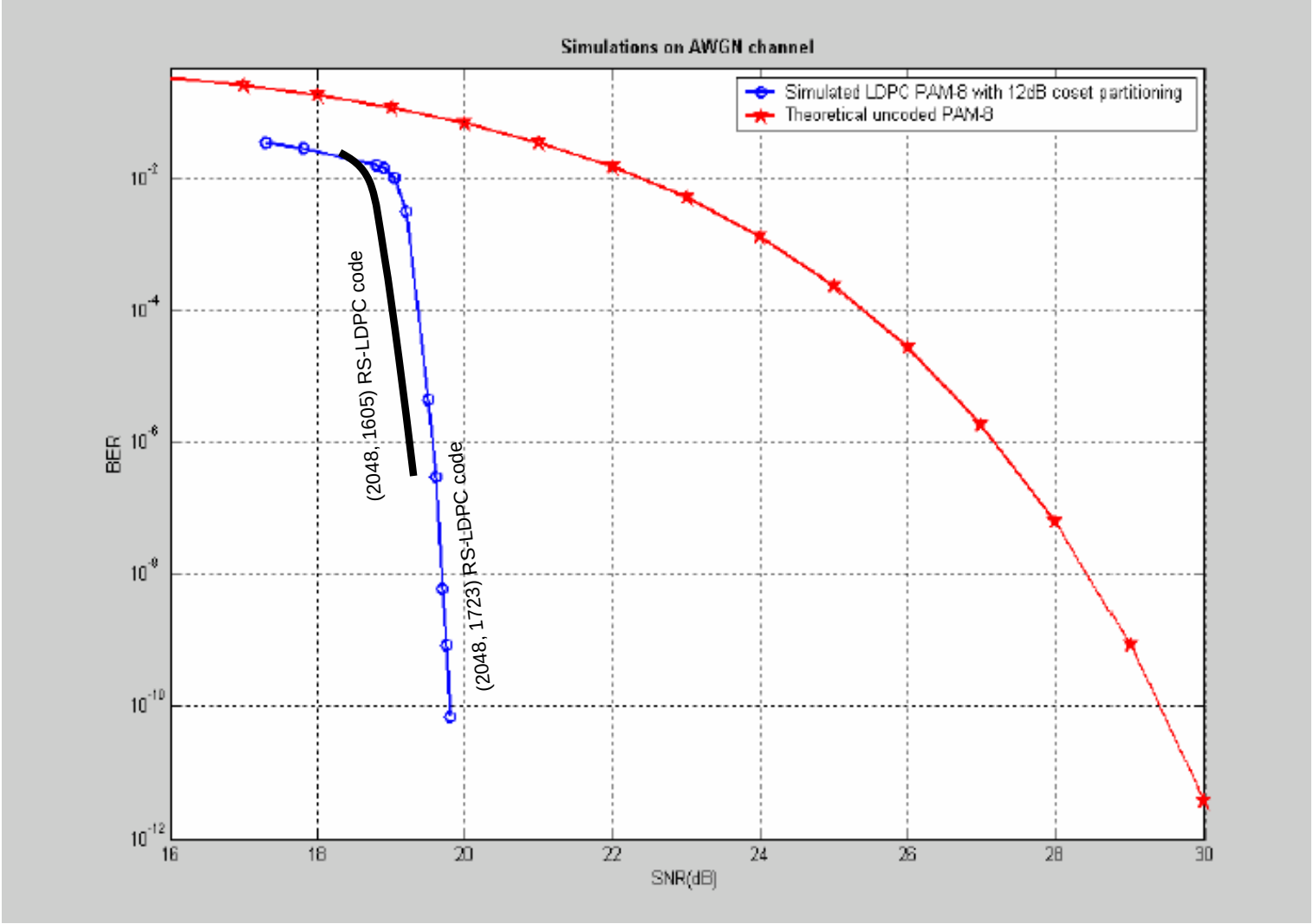
Example (2048,1605) RS-LDPC code



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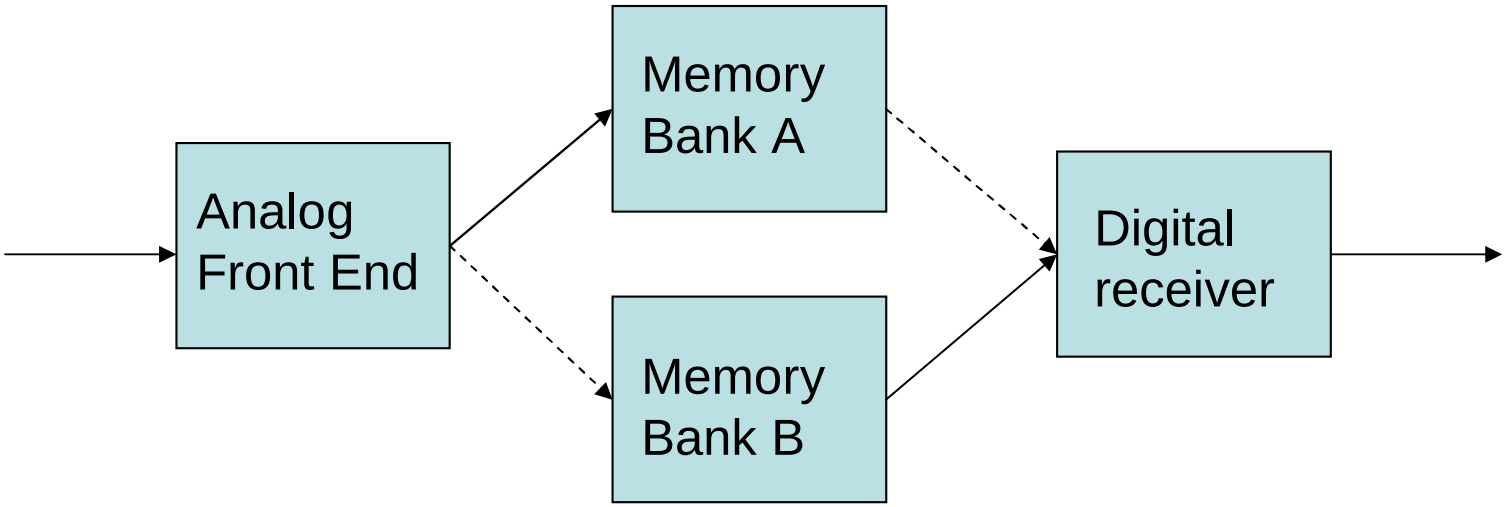
Latency reduction



- **Can use smaller LDPC block code to reduce latency**
  - For the (2048, 1723) LDPC block code, Tx+Rx latency will be less than 1us.
  - Smaller block code will lead to higher complexity in the receiver
  - Reducing the length of block code by a factor of 2 will not reduce latency by a factor of 2
    - For a (1024, 862) block code, Tx+Rx latency will be around 0.75us.

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Thank You!

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