PAM2 Training Frame Alignment Proposal

IEEE P803.2an Task Force

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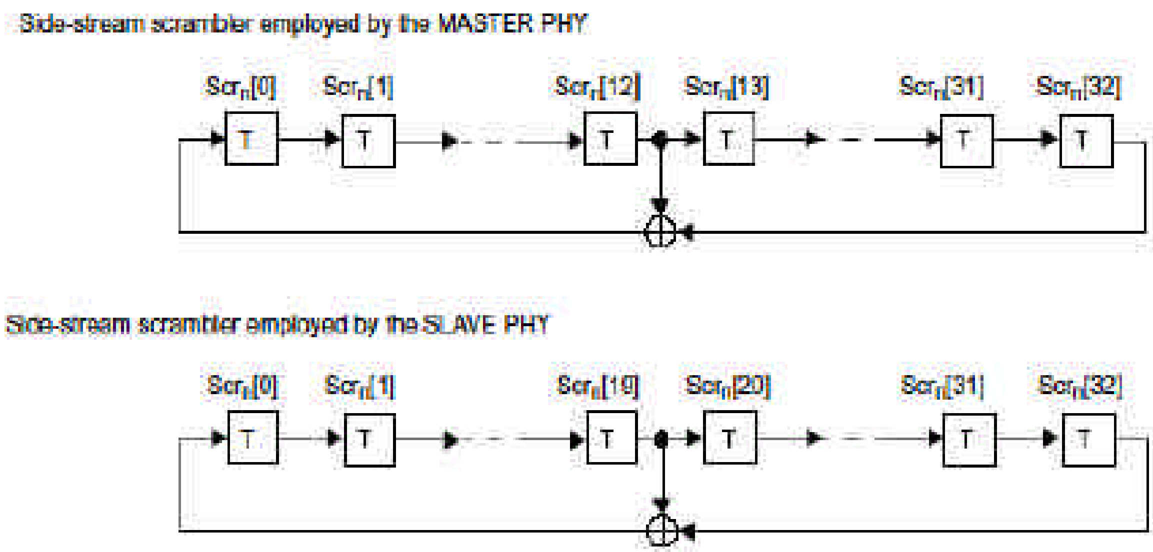
Objectives

- **Seki_2_0904 list the following startup objectives**
  - **Recover timing and adaptive filter coefficients**
  - **Establish polarity correction, pair swap, pair deskew**
  - **Establish LDPC block boundary**

- **This proposal addresses all three objectives using the PAM2 training pattern.**

PAM2 Training Signal

Side stream scrambler: (ref IEEE802.3 40.3.1.3.1)



$$g_M(x) = 1 + x^{13} + x^{33}$$

$$g_S(x) = 1 + x^{20} + x^{33}$$

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PAM2 Training Signal cont.

Generation of bits Syn[3:0]

$$Sy_n[0] = Scr_n[0]$$

$$Sy_n[1] = g(Sy_n[0]) = Scr_n[3] \wedge Scr_n[8]$$

$$Sy_n[2] = g(Sy_n[1]) = Scr_n[6] \wedge Scr_n[16]$$

$$Sy_n[3] = \begin{cases} g(Sy_n[2]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24] & if\,(loc\_rcvr\_pma\_status = NG) \\ g(Sy_n[2]) \wedge Sy_n[0] = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24] \wedge Scr_n[0] & else \end{cases}$$

$$g(x) = x^3 + x^8$$

Generation of Transmit symbol vector

$$A = \begin{cases} 7 \; if\,(Sy_n[0] = 0) \\ -7 \; else \end{cases} \quad B = \begin{cases} 7 \; if\,(Sy_n[1] = 0) \\ -7 \; else \end{cases}$$

$$C = \begin{cases} 7 \; if\,(Sy_n[2] = 0) \\ -7 \; else \end{cases} \quad D = \begin{cases} 7 \; if\,(Sy_n[3] = 0) \\ -7 \; else \end{cases}$$

This PMA training signal can meet objectives of polarity correction, pair swap, pair deskew.

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Current Issues

- **Pair Swap**
  - **For unexpected pair swap detection, pair A should be distinct from the other pairs yet still psuedo-random as in 1000BASE-T.**
  - **For fast startup, pair A detection should be fast.**
- **LDPC block frame alignment**
  - **Pair A may be used to establish the LDPC block boundary**

PAM2 Training Sync Bit

- **Sync Bit Generation**

$$Sy_n[0] = \begin{cases} !Scr_n[0] & \text{for } \mathrm{n} = \mathrm{k} \bullet 128, \mathrm{k} = 1,2,3,.... \\ Scr_n[0] & \text{else} \end{cases}$$

- **Achieves the startup objectives**
  - **Pair A transmit sequence is still psuedo-random for timing and EQ training.**
  - **Pair A is easily determined for pair swap detection**
  - **LDPC block boundary is easily and quickly determined**

Simple Frame Synchronization

- **Four steps**
  1. Find the LFSR sequence match for length L < 128
  2. Wait for the sync bit
  3. Verify additional sync bits
  4. Establish start of frame boundary
     – Note LFSR match test continues through steps 2 and 3

- **Fast LDPC block boundary detection**
  - Can be done in 1 frame
  - Extremely robust in 2 frames

Detection Example

- For L = 33, and frame boundary established on the 2^{nd} sync bit
  - Probability of False Detection over random data
    - PFD $< 2^{-33} \bullet 2^{-128} <$ 4E-49
    - > 1E32 years at 800MHz
  - Maximum sync time < 2 frames
    - < 320ns for 128 baud frame
    - Compare to 128 frames (20 μs) for Clause 49 type “slip” synchronization

Conclusion

- **PAM2 training frame alignment pattern achieves the startup objectives.**
  - **psuedo-random sequence**
  - **Pair A is easily determined**
  - **Denotes LDPC block boundary**
- **Minor change to Seki's proposal.**
- **Very simple hardware implementation.**