Ad Hoc Meeting minutes: 19Aug04

Attendees:

joel@force10networks.com

ging-lun.chen@intel.com

Brian.Brunn@xilinx.com

Steve.Anderson@xilinx.com

Edward.w.gong@intel.com

galo.r.acuna@intel.com

john.dambrosia@tycoelectronics.com

mlerer@fpga.com

pravinp@us.ibm.com

richard.mellitz@intel.com

charles_moore@agilent.com

shannon_sawyer@agilent.com

glen@vitesse.com

schelto.vandoorn@intel.com

brian.seemann@xilinx.com

why@pmc-sierra.com

m_oltmanns@comcast.net

cathyl@lsil.com

aghiasi@broadcom.com

tomaz@force10networks.com

michael.w.altmann@intel.com

BrianVon@FPGA.com

william.r.peters@intel.com

Mike Oltmanns taking notes.

General Business:

IEEE Interim will be last week of September.

Agenda Items for discussion:

Test card SMA Launch

Joel provided a general overview of the test card architecture as review. The primary issue as can be seen in the test data is the SMA launch. The goal is to get agreement on how to properly de-embed the SMA launch.

Due to some confusion, a clarification of TP1 and TP4 is warranted. We will not reach agreement on how to de-embed a BGA pad so we have to just have a clean launch into a channel starting at TP1. So we should clean the SMA launch, so that we can show all the requirements of TP1 through TP4. The proposal is to discuss methods for cleaning up the SMA footprint. Additionally, it is proposed that we look at BGA pad and associated via effect and DC blocking cap effects on SDD21. We need to understand those effects even though they occur outside of TP1 and TP4, and therefore are not part of the channel.

It has been previously decided that the breakdown for TP1 and TP4. The point where the transmit component hits the pad is the break point for TP1. The via for the BGA is an issue but it is more of an implementation issue and is difficult to plan as part of the channel model..

The capacitor is another issue as how we account for it. In Goergen_030704, the straw polls have never shown a negative feedback about the DC blocking caps. It has been clearly defined where TP1 and TP4 are, and the DC blocking point is included on the receiver side of TP4. This is a very similar situation to the OIF CEI.

The issue is that the capacitor issue has been a work item that we have not yet addressed. The response to this is that the channel group does not need to address this as the definition of TP1 and TP4 removes the cap. from the channel. It may still be an issue, but is not currently in the scope for the channel group. The interactions outside of TP1 through TP4 may require an entire separate analysis.

The position of the channel group is that the cap is for now a signaling item and is outside of the channel group. But this is still debated. The DC blocking cap has traditionally always been with the receiver though and has formed the basis of the Channel group's progress.

There is a question of where the cap should be and a second question is that there should be informative or an annex about design expectations of what the channel implementation should look like regardless where the capacitor is at relative to the Channel Ad Hoc channel model. So to address this, we could set a bar or a set of assumptions for the TX to TP1 and TP4 to Rcvr.

One issue with current locations of TP1 and TP4 is the difficulty to measure a real system at these locations.

From the TX to TP1, the pad has to belong with the package(no debate), the dogbone and via is a grey area, but is currently part of the TX, then we have the channel to TP4. Then into the DC Cap to the via and the pad/package.

Current BGA tests are only to the solder ball, so the issue can still be ownership of the pad, dogbone, and via

Bringing the debate to a straw poll:

1. We place the pad on the tx side of TP1 Yes, I agree No, I don't agree

John D - Y
Mike A. - Y
Pete T. - Y
Ali - Y
Cathy - Y
Mike O. - Y
Graeme - Y
Brian S. - A
Steve A. - Y
Adam - Y
Joel - Y

Brian VH - Y

 $Brian \; Brunn - Y$

Rich - Y

Charles Moore - Y

Shelto - Y

```
\begin{aligned} Glen &- Y \\ Shannon & Sawyer - Y \\ Mike & Lerer - Y \end{aligned}
```

18 Yes, 0 No, 1 Abstain

2. For the channel side of TP1 we define a clean launch and the definition of clean launch no greater imp change than already exists for backplane connectors, typically about 8-9 Ohms.

Yes, I agree - No, I don't agree

Brian VH – Y John D - A Mike A - A Pete T. - Y Ali - Y Cathy - A Mike O. - Y Graeme - Y Brian S. - A Steve A. - Y Adam – Y Joel – Y

Brian Brunn - Y

Rich - A

Charles Moore - Y

Shelto – A

Glen - A

Shannon Sawyer - A

Mike Lerer – Y

11 Yes, 0 No, 8 Abstain

3. We define a clean launch for the channel into TP4 and the definition of clean launch no greater imp change than already exists for backplane connectors, typically about 8-9 Ohms.

Yes, I agree No, I don't agree

Brian VH – Y John D - A

Mike A - A

Ali - Y

Cathy - A

Mike O. - Y

Graeme - Y

Brian S. - A

Steve A. - Y

Adam-Y

Joel - Y

Brian Brunn - Y

Rich – A

Charles Moore - Y

Shelto - A

Glen - A

Shannon Sawyer - Y

Mike Lerer - Y

11 yes, 0 no, 7 abstain

4. The pad and DC cap, if exists, on the RX side of TP4 Yes, I agree No, I don't agree

 $Brian\ VH-Y$

John D - A

Mike A - Y

Pete- Y

Ali - N

Cathy - N

Mike O. - Y

Graeme - Y

Brian S. - A

Steve A. - N

Adam - Y

Joel - Y

 $Brian \; Brunn - A$

Rich - N

Charles Moore - N

Shelto – A

Glen - N

Shannon Sawyer - N

Mike Lerer - Y

8 yes, 7 no, 4 abstains

Discussion regarding next week's call for the signaling group and how this straw poll for #4 may hold up activity. There may be a joint signaling and channel call next week

Meeting brought to a close.