Presentation to IEEE P802.3ap Backplane Ethernet Task Force
January 2005 Working Session

Title: **NRZ Simulation Results over Ad-hoc Channels**

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Abstract: This contribution provides simulation results of performance analysis across the set of test channels proposed for use by the signaling ad-hoc. Simulations are performed using a full function simulator which constructs a complete end to end transceiver-package-channel-package-transceiver model.

Outline

Simulator review from abler_01_0904

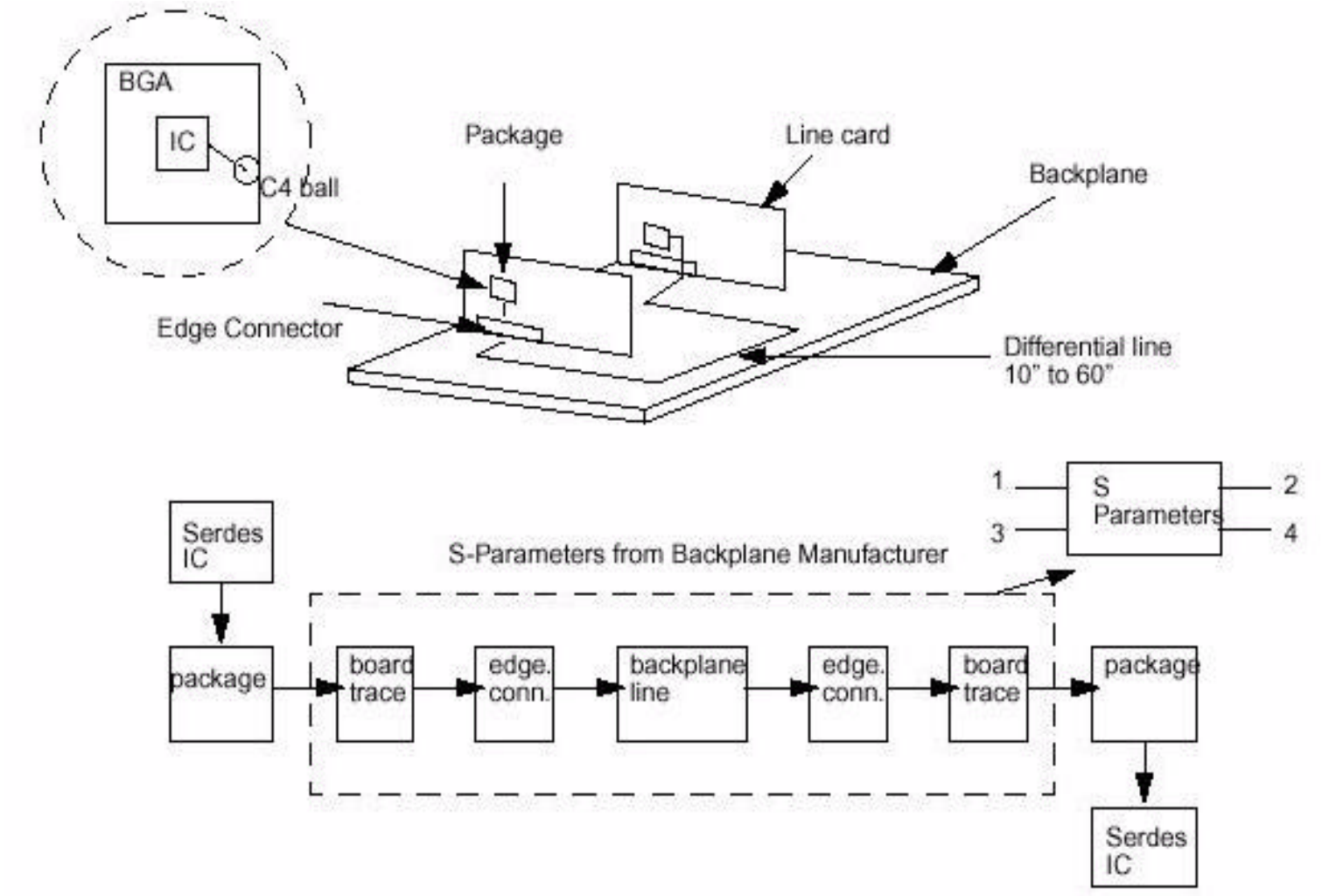
Configuration for signaling ad-hoc simulation model

Bridge from abler_01_0904 results

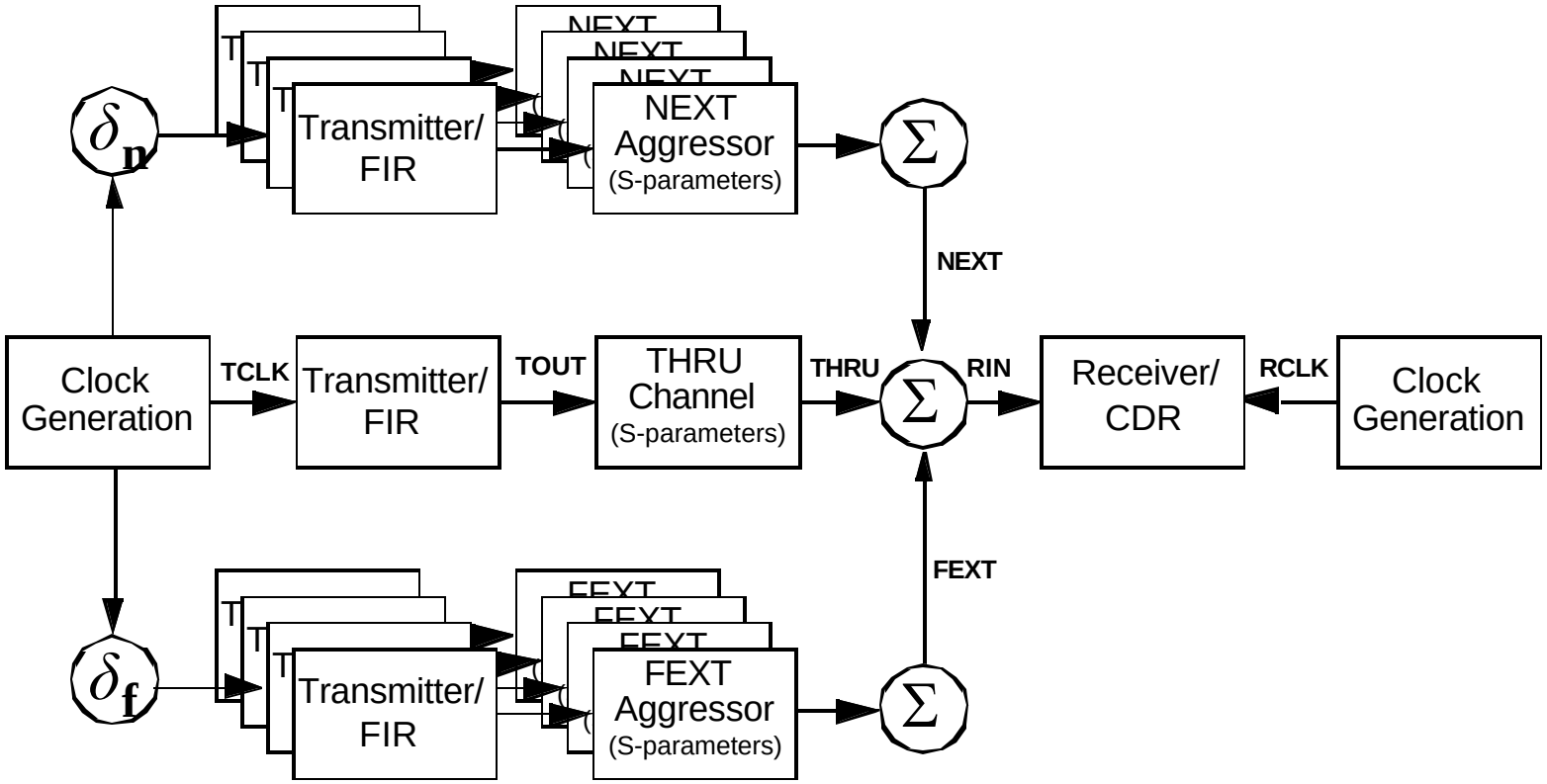
Simulation Results

Summary

DFECDR High Level Simulation Structure:



High Level Simulation Structure:



Configuration from 0904 Simulations

Configure for worst case (expected) standard definition

- Launch amplitude set to minimum — 800 mVpp
- Transmitter DJ set to maximum — 0.15 UIpp
- Transmitter RJ set to maximum — 0.0107 UIrms (0.15UIpp @ 10^{-12} BER)
- Tx/Rx termination skewed to maximum tolerance — 4040/6060 ohms

Conservatively model receiver implementation

- Receiver DJ in addition to termination parasitics — 0.05 UIpp
- Receiver RJ set to maximum — 0.0107 UIrms (0.15UIpp @ 10^{-12} BER)

Approximate parasitics for worst case 12Gbps implementation

- Use nominal case parasitics from 6Gbps design in 0.13um technology
  - Extracted parasitics for 12Gbps implementation are not available
  - These parasitics considered highly conservative relative to WC parasitics of 90nm 12Gbps design

Configure system parameters

- Data rate: 10.3 Gbps
- Receiver offset: 200 ppm
- Data pattern: Random
- Use all cross talk channels for each test case
- Vary FFE/DFE configuration across runs
  - FFE2 as single post-cursor
  - FFE3 & FFE4 includes a single pre-cursor
- Run test suite across 2 package types (organic & flip chip plastic)
- 10M bit simulation time per testcase

Steps to bridge to ad-hoc simulation model

Reduce simulation time to 1M bits

- Too many runs, too little time....

Levelset less significant parameters

- Terminations set to 5050/5050 ohms (vs. 4040/6060 ohms)
- Frequency offset removed (vs. 200ppm)
- Use PRBS15 data pattern (vs. random)

Upgrade to latest level simulator

- Includes true 4-port sparameter cascading and other improvements

Update IC model & improved CDR algorithm

- 6G extractions are conservative
  - Used extractions from a later design (significantly reduced Tx loading)
  - Scale frequency on receiver to double bandwidth and return loss corner frequency
  - Much more representative of 10G design
- Used new CDR algorithm for 10G design
  - Improved eye centering

Use ad-hoc defined noise

- 1.46mV rms (vs 0.8 mV rms)

Add Duty Cycle Distortion

- 3%

Add TP4-TP5 segment

- 4.7nf segment cascaded to both through and xtalk channels

Simulations for ad-hoc model

Simulation model summary

Launch amplitude set to minimum	800 mVpp
Transmitter DJ set to maximum	0.15 UIpp
Transmitter RJ set to maximum	0.0107 UIrms (0.15UIpp @ 10^{-12} BER)
Tx/Rx termination set to nominal (ideal)	5050/5050 ohms
Receiver DJ	0.10 UIpp
Receiver RJ set to maximum	0.0107 UIrms (0.15UIpp @ 10^{-12} BER)
Data rate	10.3 Gbps
Receiver offset	0 ppm
Data pattern	PRBS15
Random noise	1.46mV rms
AC coupling:	4.7nf

Simulate across package types

- Spec_RL_ind_like
- Spec_RL_cap_like
- IBM organic package for comparison purposes

Simulate 3 primary NRZ configurations

- FFE3/DFE3
- FFE3/DFE5
- FFE4/DFE5

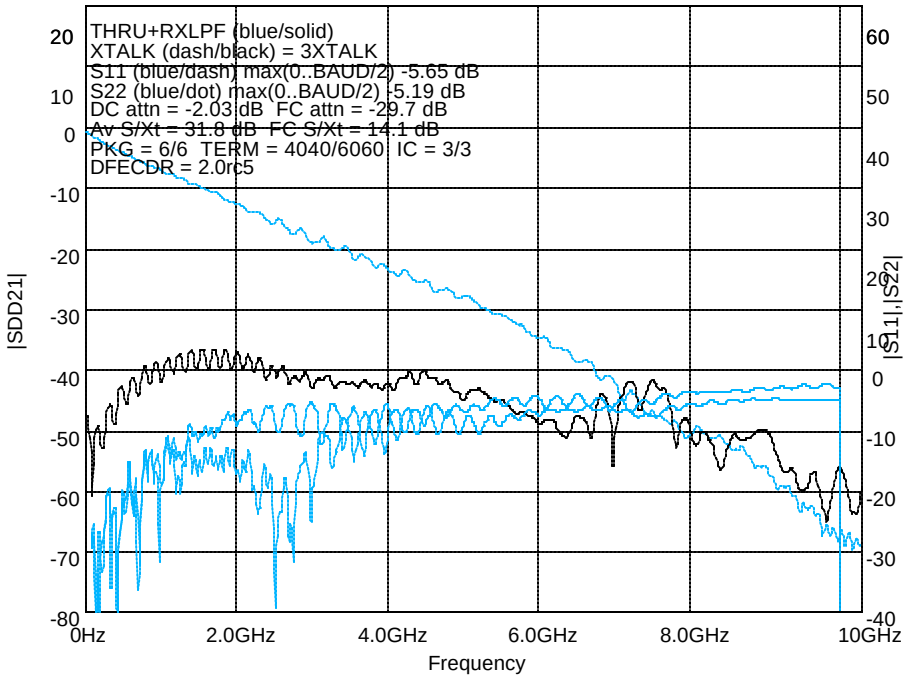
Results provided for 3 different BER

- E-12, E-15, E-17 (simulator defaults, not re-written to provide E-18)

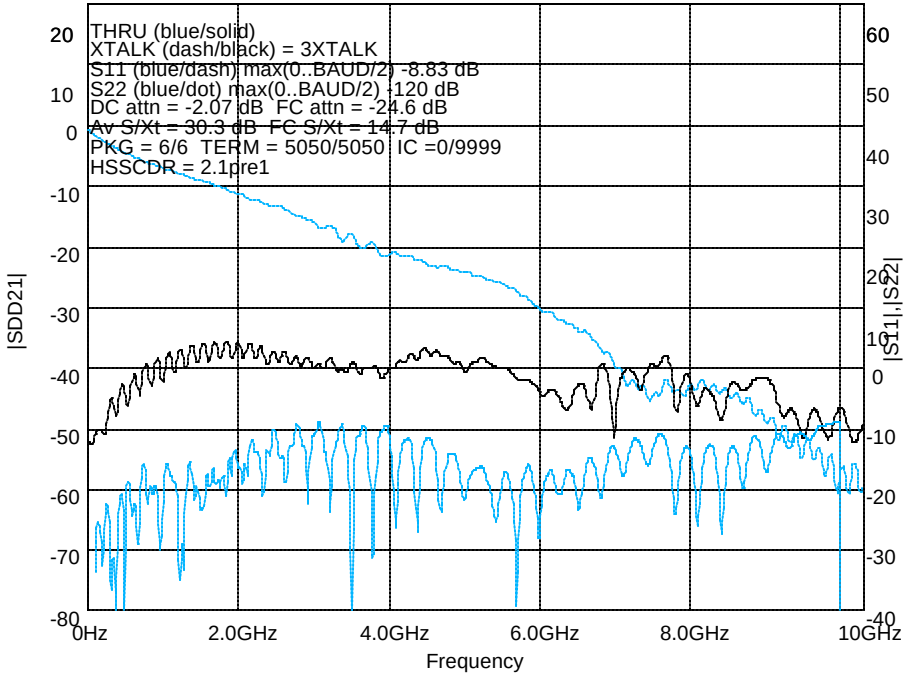
Bridge from abler_01_0904 results

Tyco Case 1, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	21.8%	22.0%	20.9%
cut sim time to 1M bits	21.7%	20.0%	15.9%
50ohm, 0ppm, PRBS15	21.8%	19.4%	21.5%
updated simulator	22.7%	20.1%	16.9%
new IC model & CDR	25.7%	27.5%	25.4%
use ad-hoc noise	19.6%	22.0%	20.8%
add DCD (3%)	8.2%	12.4%	15.9%
add AC coupling	11.8%	15.4%	11.6%

Original Channel Response



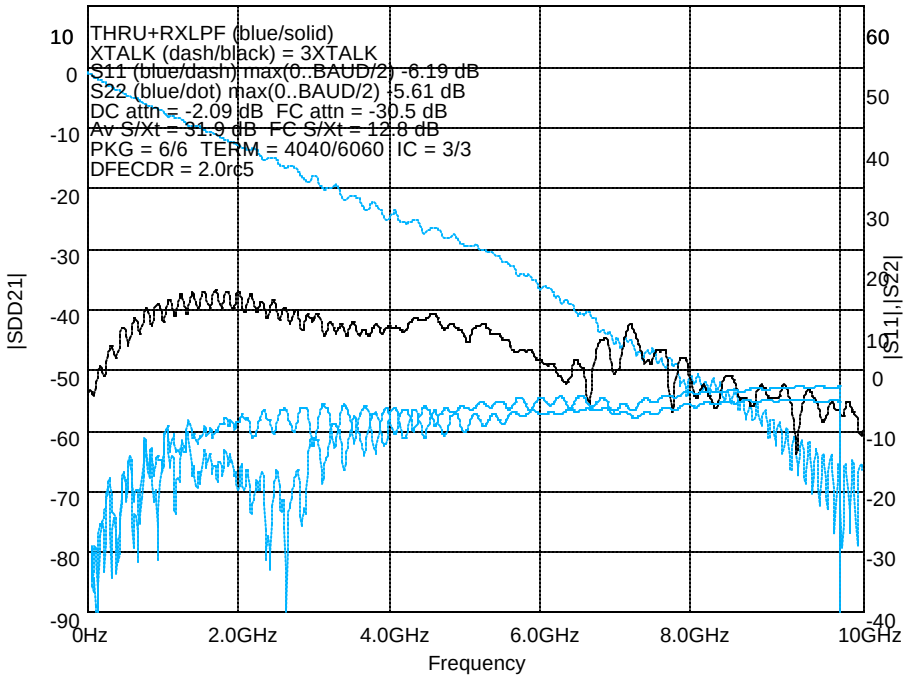
Updated Channel Response



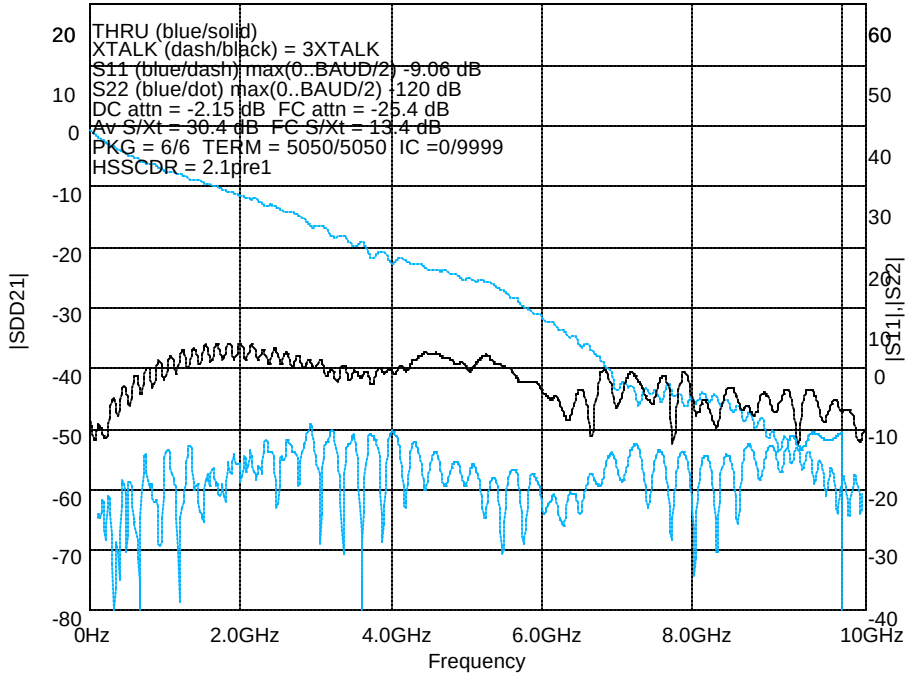
Bridge from abler_01_0904 results

Tyco Case 2, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	12.8%	21.0%	17.7%
cut sim time to 1M bits	9.1%	10.6%	14.0%
50ohm, 0ppm, PRBS15	9.0%	10.5%	13.9%
updated simulator	10.2%	15.7%	16.0%
new IC model & CDR	11.4%	27.3%	21.5%
use ad-hoc noise	4.2%	21.8%	16.2%
add DCD (3%)	0%	16.5%	16.1%
add AC coupling	E-09	13.9%	11.5%

Original Channel Response



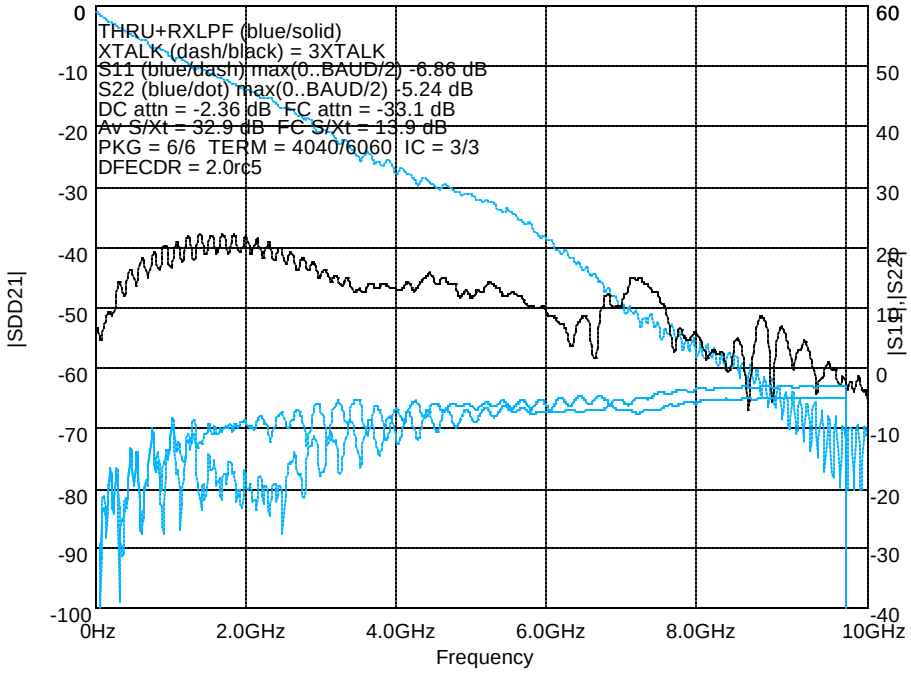
Updated Channel Response



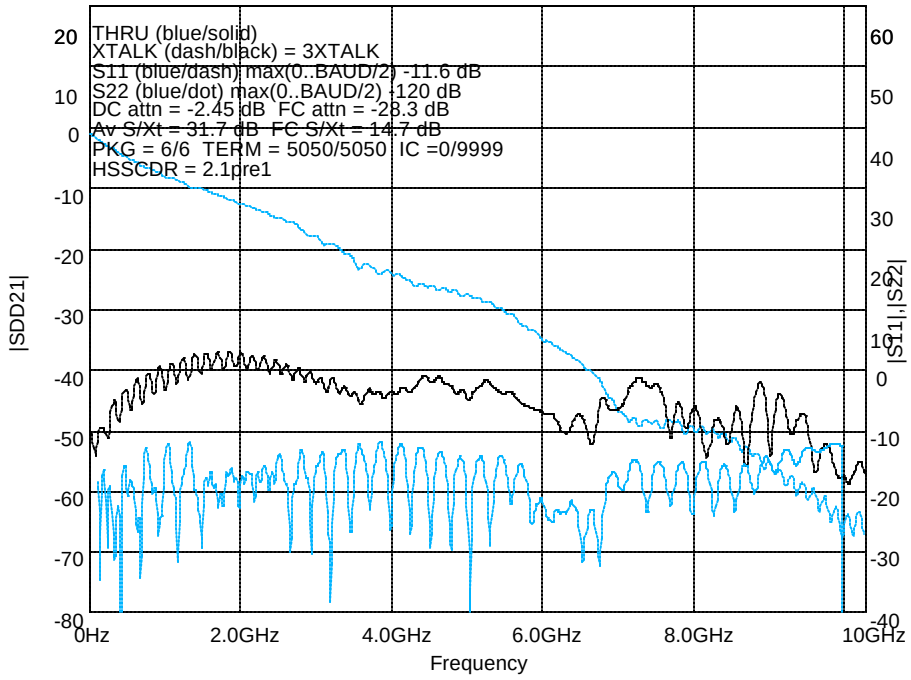
Bridge from abler_01_0904 results

Tyco Case 3, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	5.6%	17.6%	15.4%
cut sim time to 1M bits	0%	5.7%	5.0%
50ohm, 0ppm, PRBS15	0%	3.8%	5.7%
updated simulator	0%	9.4%	6.7%
new IC model & CDR	15.8%	17.5%	21.9%
use ad-hoc noise	7.1%	11.8%	15.3%
add DCD (3%)	0%	4.2%	10.9%
add AC coupling	E-07	3.6%	9.5%

Original Channel Response



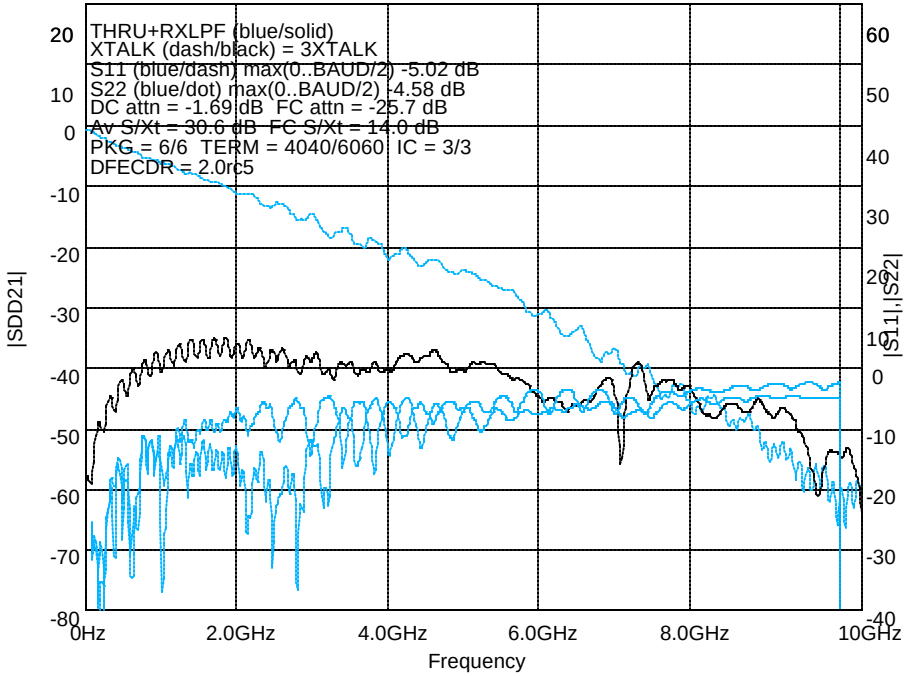
Updated Channel Response



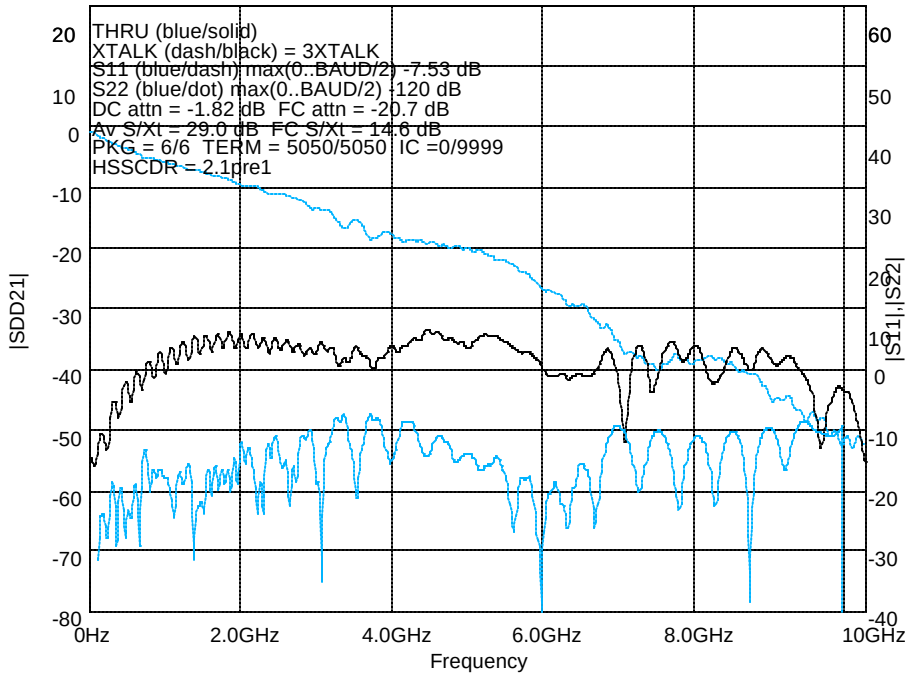
Bridge from abler_01_0904 results

Tyco Case 4, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	19.5%	21.9%	20.9%
cut sim time to 1M bits	16.5%	16.5%	21.8%
50ohm, 0ppm, PRBS15	26.8%	28.3%	27.0%
updated simulator	23.2%	23.7%	21.6%
new IC model & CDR	15.4%	21.5%	25.7%
use ad-hoc noise	13.0%	17.6%	22.9%
add DCD (3%)	13.6%	22.1%	21.3%
add AC coupling	2.1%	11.3%	20.4%

Original Channel Response



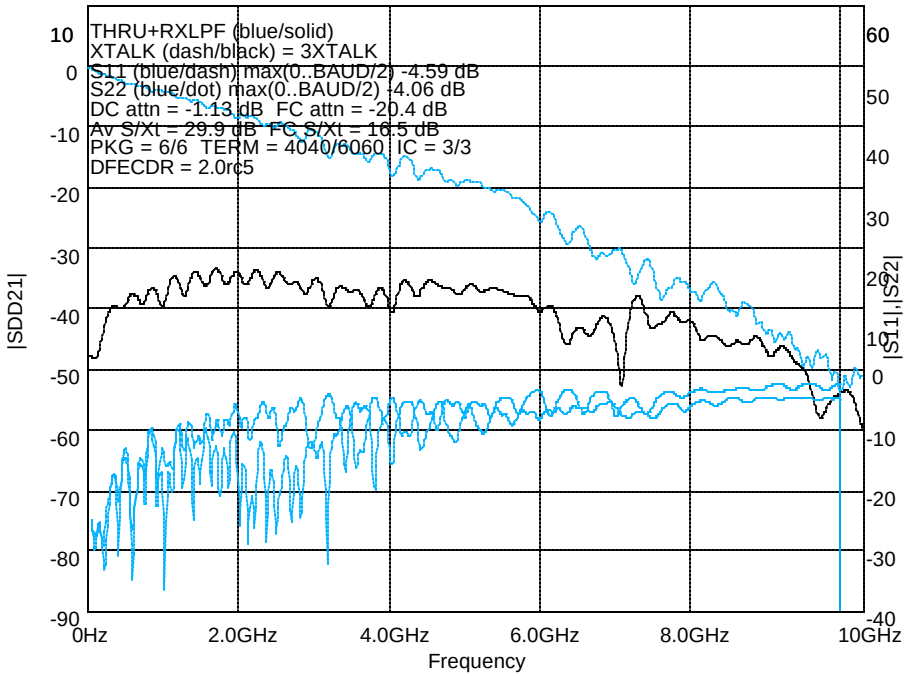
Updated Channel Response



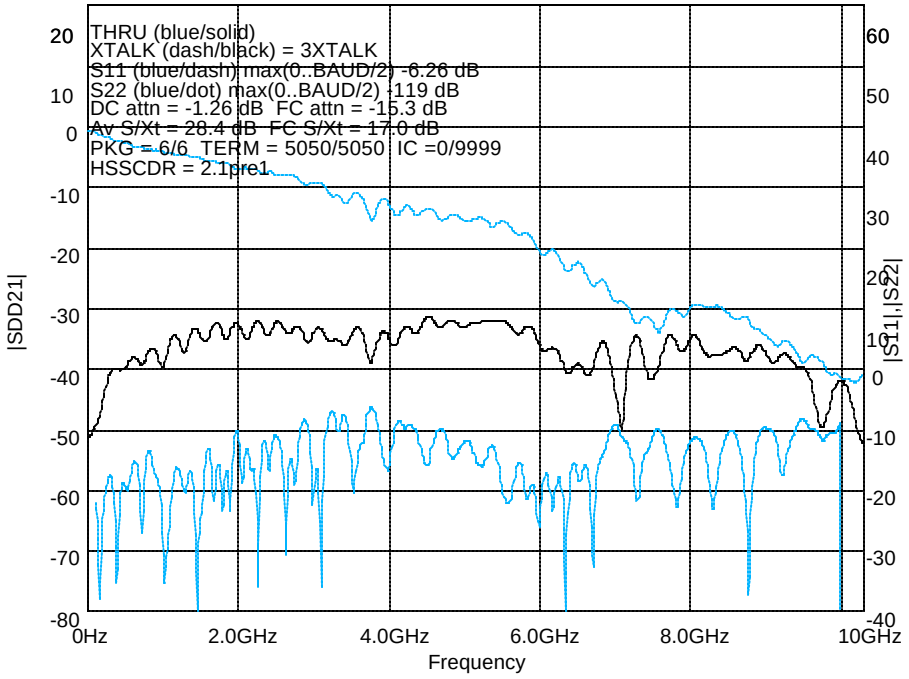
Bridge from abler_01_0904 results

Tyco Case 5, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	18.9%	22.2%	10.4%
cut sim time to 1M bits	20.6%	22.2%	23.6%
50ohm, 0ppm, PRBS15	21.6%	24.3%	25.2%
updated simulator	17.5%	22.4%	22.2%
new IC model & CDR	26.2%	27.0%	26.0%
use ad-hoc noise	23.7%	27.0%	23.3%
add DCD (3%)	20.9%	27.7%	22.1%
add AC coupling	20.2%	26.8%	19.8%

Original Channel Response



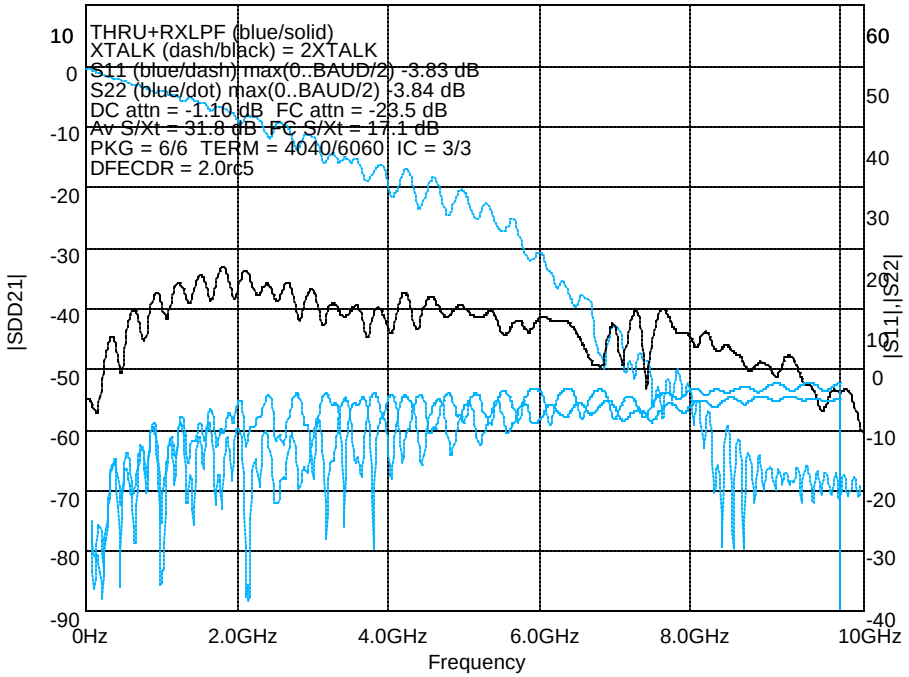
Updated Channel Response



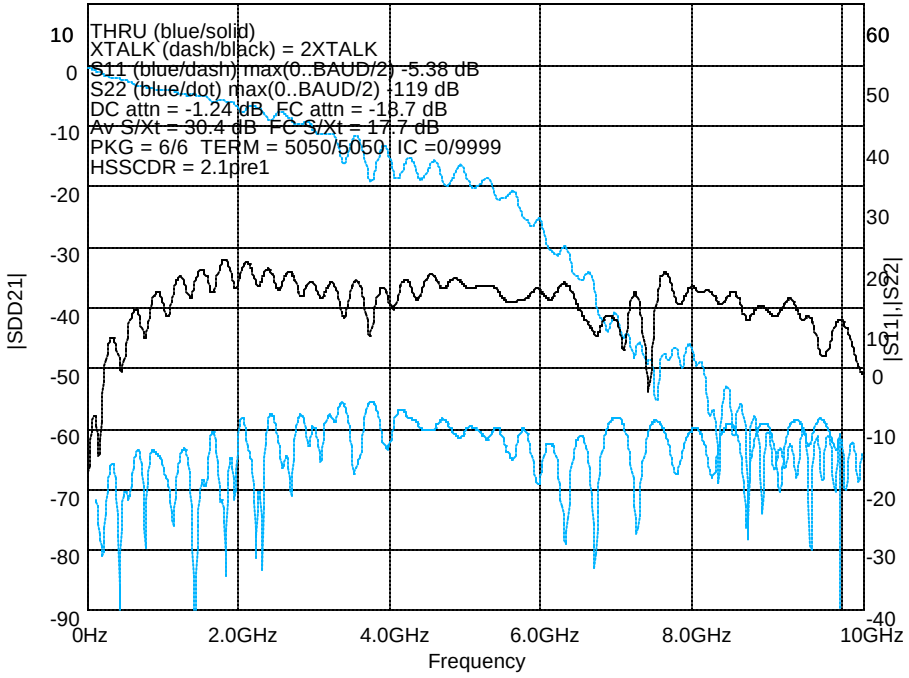
Bridge from abler_01_0904 results

Tyco Case 6, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	0%	5.5%	8.4%
cut sim time to 1M bits	3.5%	3.9%	7.1%
50ohm, 0ppm, PRBS15	3.6%	7.6%	8.7%
updated simulator	7.2%	9.0%	7.4%
new IC model & CDR	2.9%	13.9%	10.0%
use ad-hoc noise	0.1%	11.0%	8.9%
add DCD (3%)	0.1%	7.7%	5.6%
add AC coupling	E-07	E-07	E-09

Original Channel Response



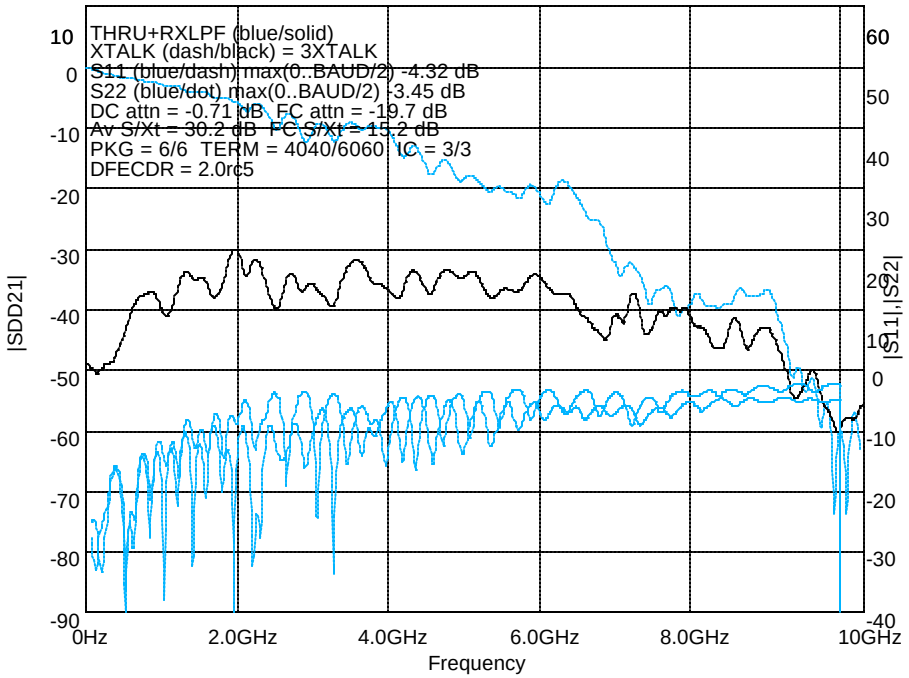
Updated Channel Response



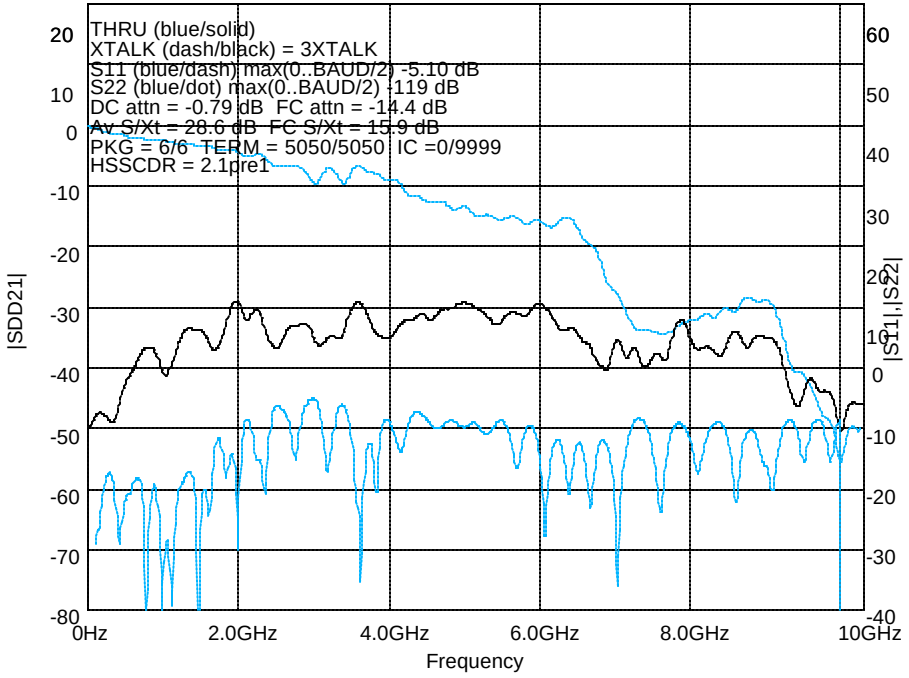
Bridge from abler_01_0904 results

Tyco Case 7, organic package (E-12)	FFE3/DFE3	FFE3/DFE5	FFE4/DFE5
abler_01_0904 results	4.4%	9.7%	9.7%
cut sim time to 1M bits	0%	13.1%	3.7%
50ohm, 0ppm, PRBS15	9.0%	15.8%	15.5%
updated simulator	3.4%	10.8%	13.2%
new IC model & CDR	16.2%	17.3%	15.9%
use ad-hoc noise	16.1%	16.9%	15.9%
add DCD (3%)	13.4%	18.0%	14.3%
add AC coupling	19.5%	22.0%	17.4%

Original Channel Response



Updated Channel Response



Results for signaling ad-hoc template

Tyco Channels

- Results across 3 configurations and 3 package types
- %Eye opening margin at BER E-12
- Complete entries provided in spreadsheet

FFE3/DFE3 (E-12)	Case1	Case2	Case3	Case4	Case5	Case6	Case7
IBM organic pkg	11.8%	E-09	E-07	2.1%	20.2%	0.8%	19.5%
Spec_RL_ind_like pkg	6.9%	0	0	8.4%	16.1%	E-08	14.7%
Spec_RL_cap_like pkg	6.0%	0	E-09	1.8%	16.9%	0	9.9%

FFE3/DFE5 (E-12)	Case1	Case2	Case3	Case4	Case5	Case6	Case7
IBM organic pkg	15.4%	13.9%	3.6%	11.3%	26.8%	3.7%	22.0%
Spec_RL_ind_like pkg	9.9%	11.2%	8.9%	17.1%	21.2%	6.1%	8.8%
Spec_RL_cap_like pkg	10.3%	11.1%	0.1%	12.4%	17.2%	9.9%	13.1%

FFE4/DFE5 (E-12)	Case1	Case2	Case3	Case4	Case5	Case6	Case7
IBM organic pkg	11.6%	11.5%	9.5%	20.4%	19.8%	0.5%	17.4%
Spec_RL_ind_like pkg	11.0%	7.3%	7%	17%	17.7%	9.7%	9.9%
Spec_RL_cap_like pkg	13.4%	8.5%	5%	18.1%	21.8%	8.9%	4.2%

Simulation with other ad-hoc Channels

Peters

- Some potential seen in "b" channels, but borderline performance at best
- "m" and "t" channels are in the mud
- Limited time did not allow for analysis of primary performance detractors
  - Xtalk was seen as having a significant impact in many cases, particularly "m" and "b" channels
- Results are included in spreadsheet

Molex

- Not simulated primarily due to lack of time
- Also, not clear which xtalk channels went with which through channels

Goergen

- Sparms are in error, could not run
  - Frequency steps are out of whack

Summary

Simulation results provided based on ad-hoc signaling model

- Reasonable model for the most part
  - Environmental noise considered high
- Other key parameters still conservatively set, but modeled for worst case standard
  - Jitter, launch voltage

Key factors which can significantly vary performance

- Package & IC model
- Crosstalk
- Duty cycle distortian

Channel model

- Tyco channels can be solutioned
- Channel model is stretching the bounds of traditional system performance requirements
  - Should be reeled in, or
  - A normative model with performance metrics should be provided

Signaling

- NRZ with advanced FFE/DFE equalization can meet backplane performance needs at 10+ Gbps