IEEE 802.3ap
Proposal to use PR-4 Signaling for 10Gbase-KR links

IEEE 802.3ap Task Force
Jan'05

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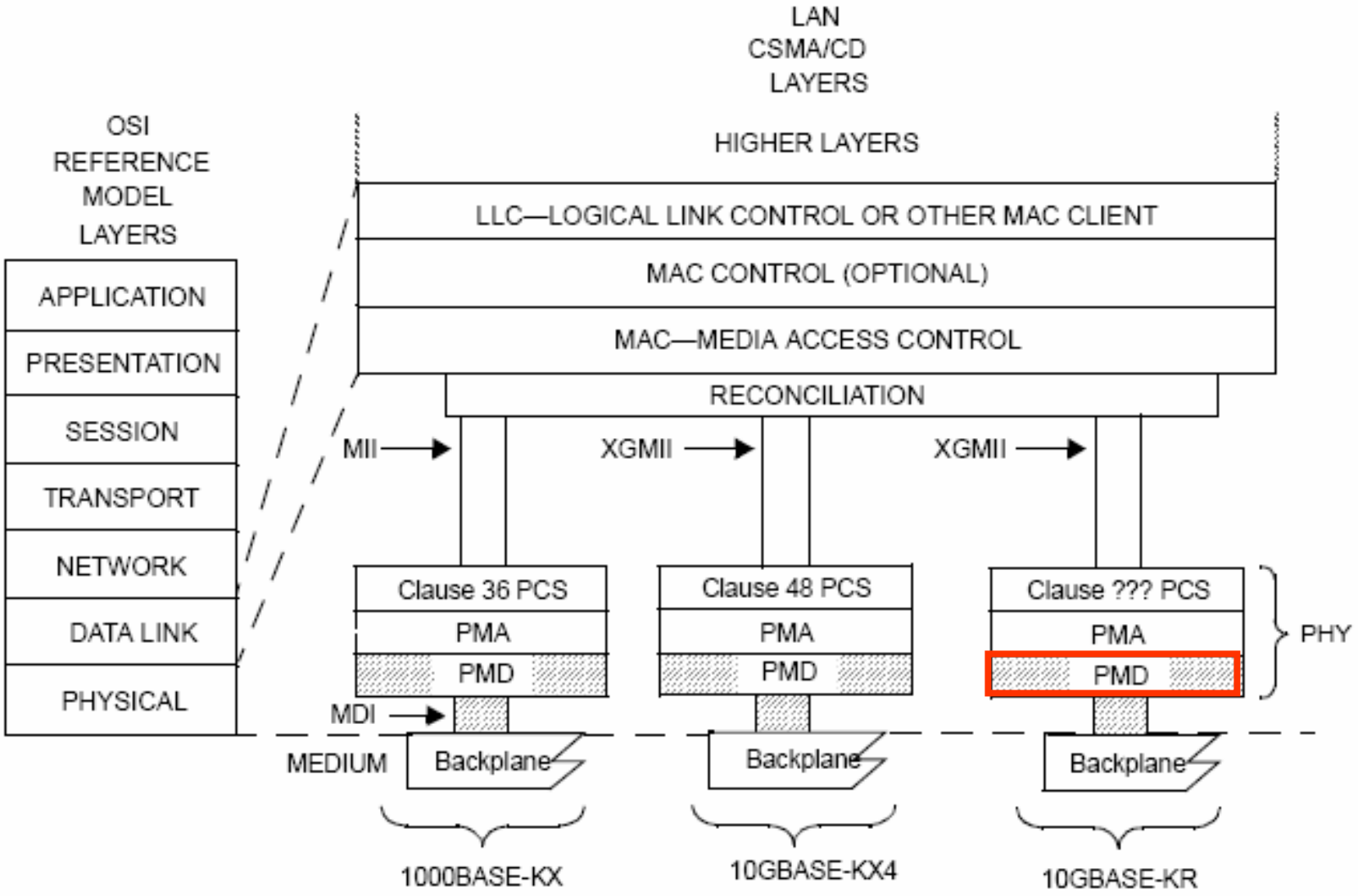
Objectives

- Propose a PR-4 based signaling solution for 10Gbase-KR signaling on backplanes
- Allows leveraging signaling techniques & experience from the storage industry
- PR4 signaling can acceptably equalize typical BP channels
  - Simulation results will be shown

Agenda

- Layer Model
- Proposal Overview
- Link Model
- PR-4 Signaling
- AN and Link training
- PR-4 simulation results
  - Adaption simulations
  - MMSE-optimized eye diagrams

IEEE802.3ap Layer Model



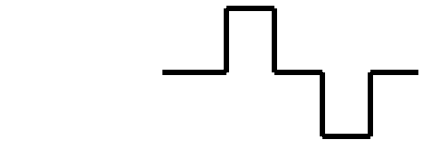
Overview

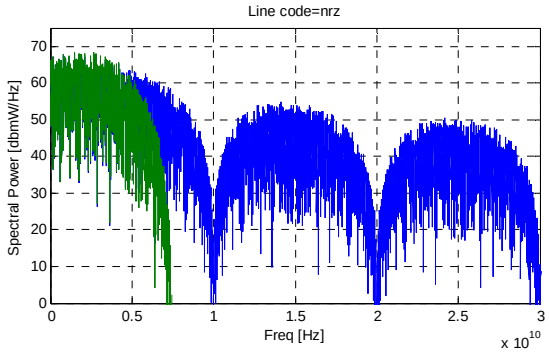
- Use PR-4 signaling for 10Gb serial BP channels
  - PR-4 has spectrum & implementation advantages
  - Requires pre-coding to limit error propagation
- Use existing 802.3 clauses for other functions:
  - PCS (clause 49)
  - PMA (clause 51)
  - MDIO (clause 45)
  - Auto-Negotiation (clause 28)
    - Possible signaling modifications as in brink_01_1104.pdf or thaler_01_1104.pdf)
- Programmable Tx and Rx equalization optimized with training

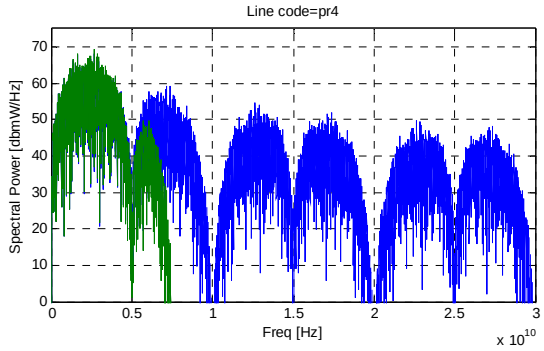
PR-4 Signaling - Background

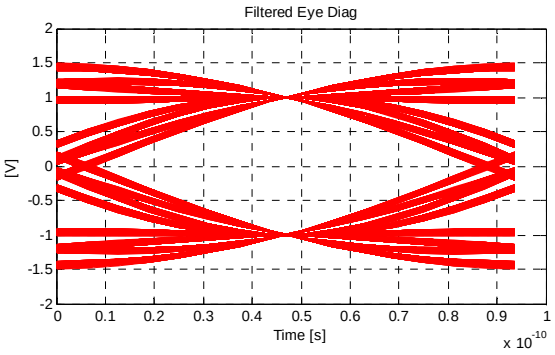
- **Used extensively in disk drive industry**
- **Equalized systems use non-unity target polynomial**

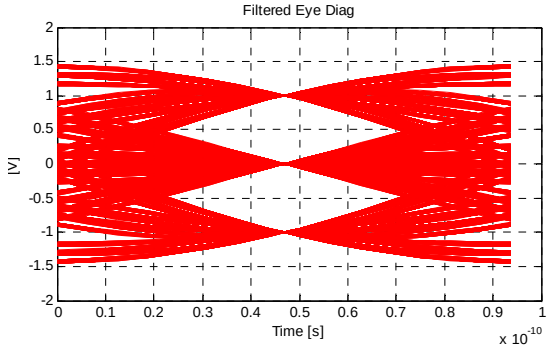
NRZ: Y=X ⇒ **PR4: Y=(1-D²)X**











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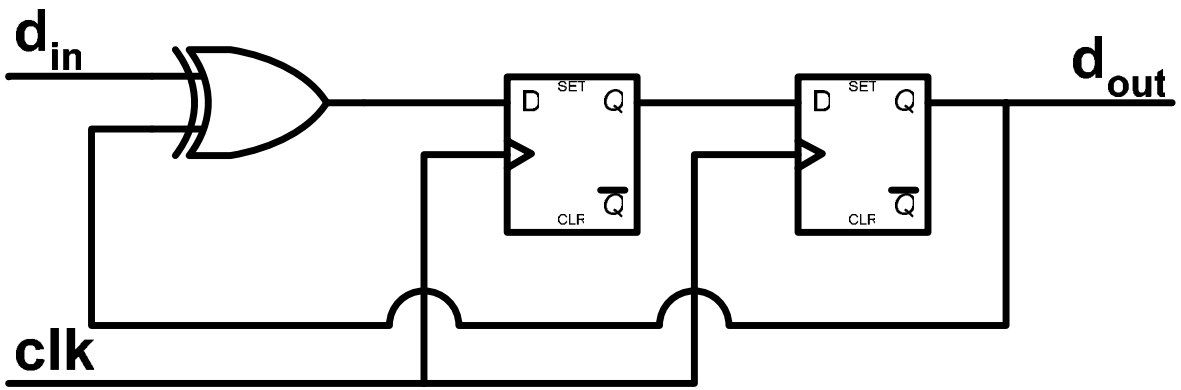
PR-4 Signaling - Background

- Multi-level encoding
  - 2-level NRZ becomes 3-level PR-4 encoded data at Rx
  - Adds coding redundancy which alters the spectrum
    - Nulls at DC and $f_{bit}/2$
  - True Nyquist channel possible for minimum noise
  - Encoding mechanism is combination of Tx Eq, channel, Rx AFE and Eq
- 'Allowable' ISI reduces equalization boost from NRZ
  - See 'altmann_02_0904.pdf'
- Zero crossing between +1, -1 pulses is an excellent timing indicator
  - Enables baud-rate Rx design
  - Reduces sampler complexity by 50%
- PR-4 requirements
  - Requires both Tx and Rx equalization
  - Tx pre-coding to limit error propagation

PR-4 Signaling

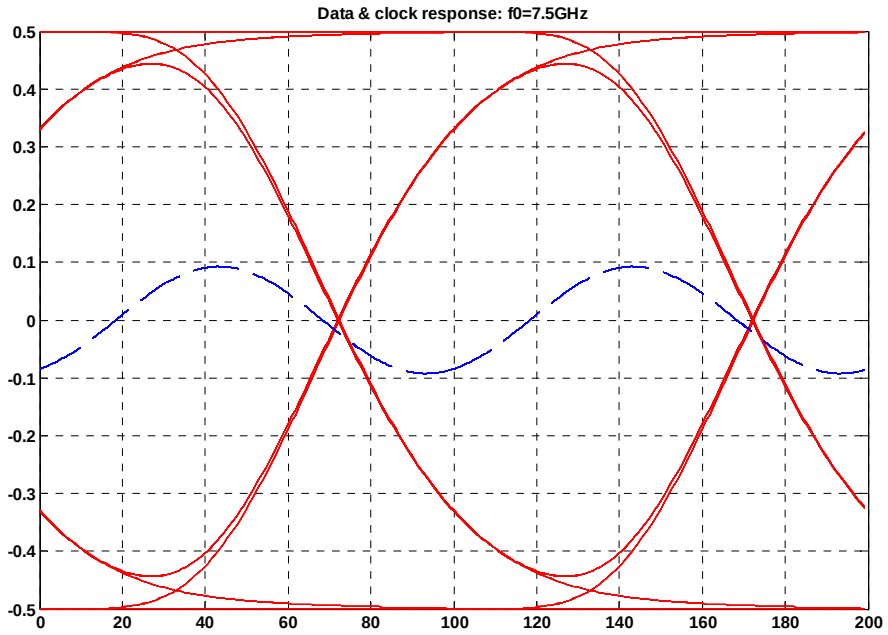
- **Data encoding requirements**
  - Tx pre-coding not explicitly required, however it eliminates error prpoagation from incorrectly decoded bits
- **Data Decoding options**
  - Can use bit-by-bit or optional MLSE (ex. Viterbi) detection
  - Receiver can operate at half-rate, as data stream is intrinsically interleaved
  - Both decoding methods requires a pre-coder to eliminate error propagation.
- **PR-4 Pre-coder**



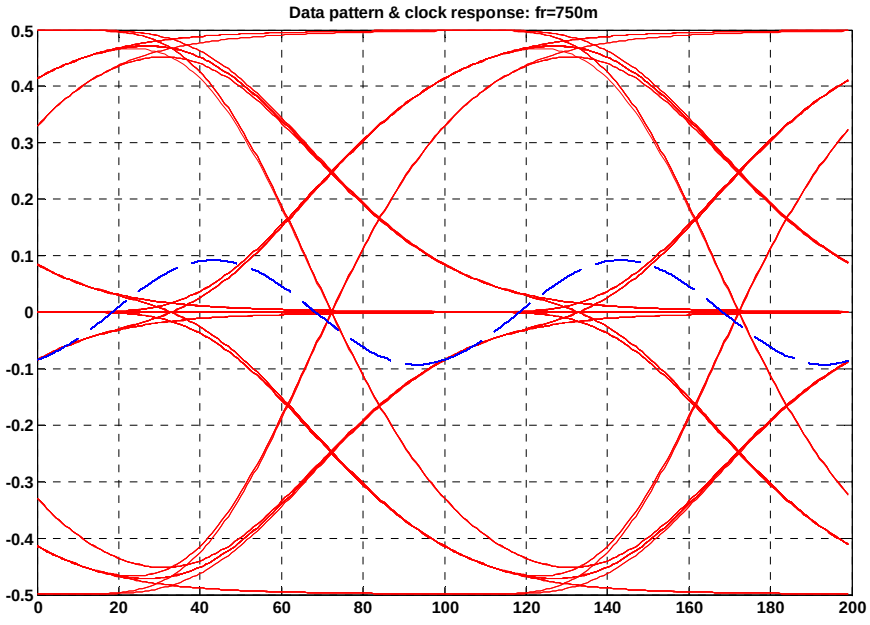
PR-4 Signaling vs NRZ

- Controlled ISI creates 3-level eye diagram
- In BW-limited channels, eye height reduces slower than NRZ
- Jitter is higher due to direct +1 → -1 transitions

Filtered NRZ Eye: ω_0=7.5GHz

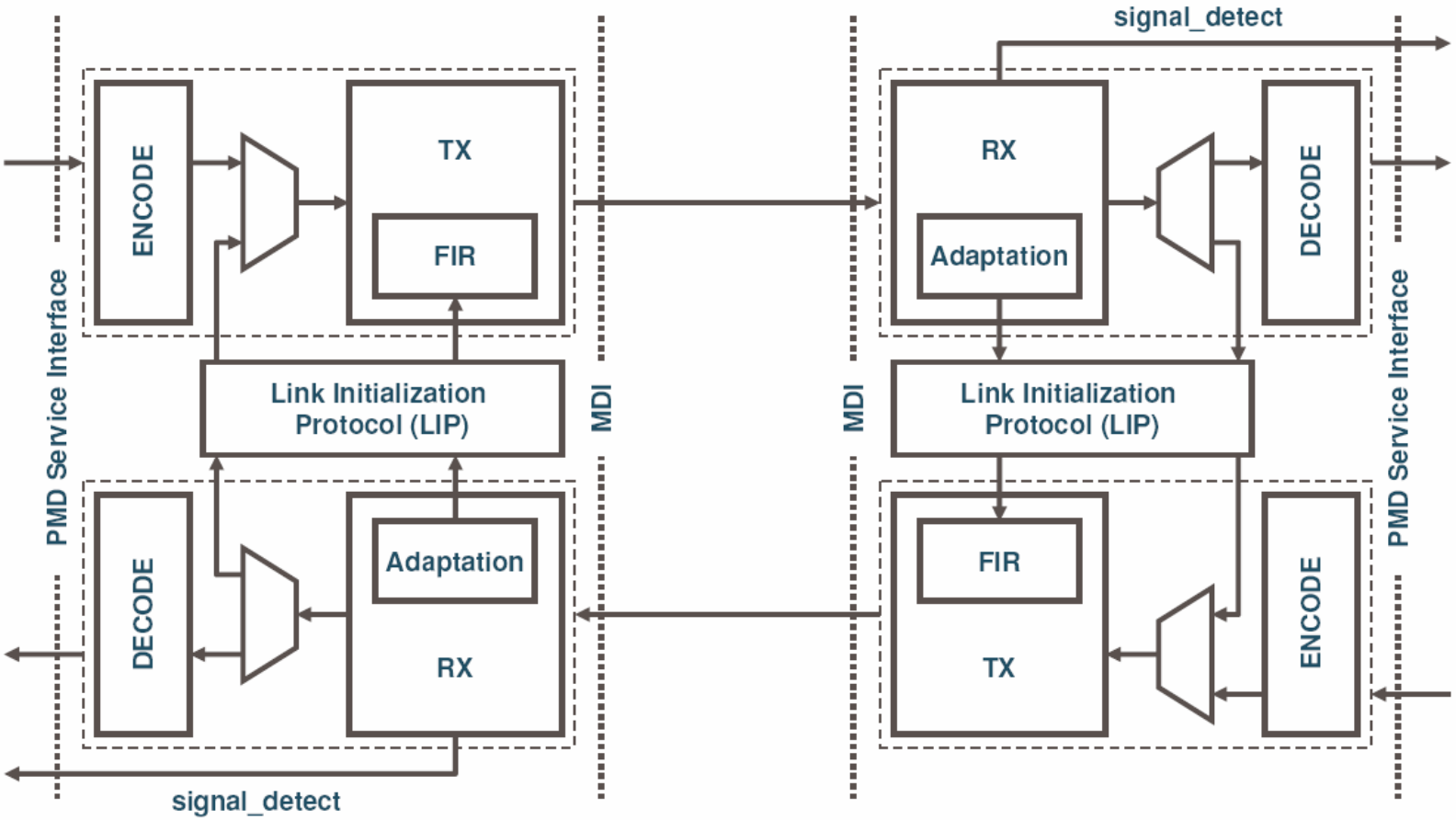


Filtered PR-4 Eye: ω_0=7.5GHz



Link Model (from brink_01_1104.pdf)

Link Model



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November 16, 2004 (r1.2)

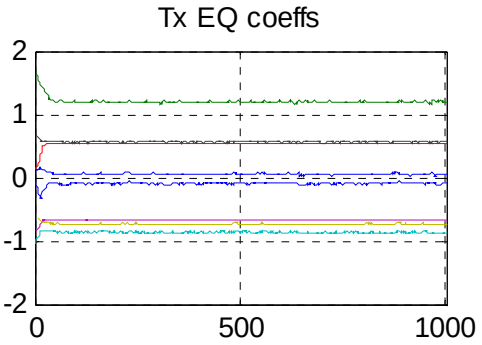
Auto-Negotiation & Eq Training

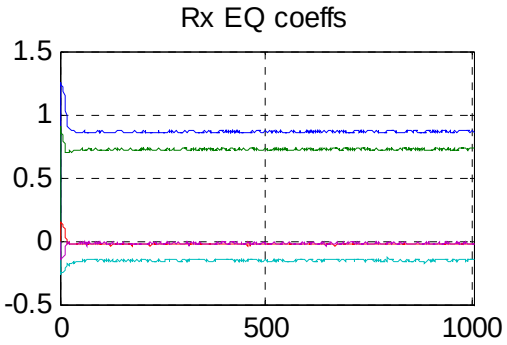
- AN and link training required
  - AN will exchange PHY capabilities and determine bit-rate
  - Follow method similar to thaler_01_1104.pdf or brink_01_1104.pdf
- Timing Acquisition
  - Initial timing acquisition using ¼-rate signal: +1 +1 -1 -1 (approx a clk at PR4 spectral peak) before equalization
  - Rx signal is approximate sine wave
  - Final timing acquisition using simple (TBD) known data patterns
- Equalizer training
  - Initial equalizer training can occur using (TBD) training sequences (altmann_02_1105.pdf)
  - Optimal (TBD) training sequence will be defined for faster PR4 adaption
- After link training, equalizers continuously update with active traffic

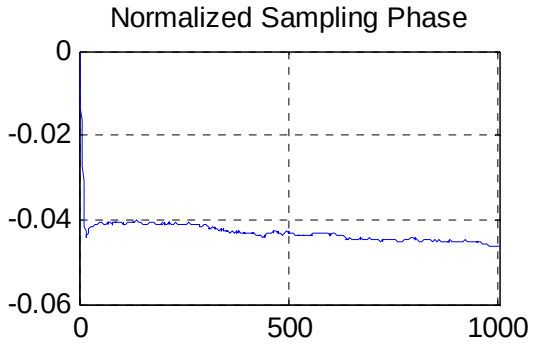
PR-4 Equalizer Adaption Simulations

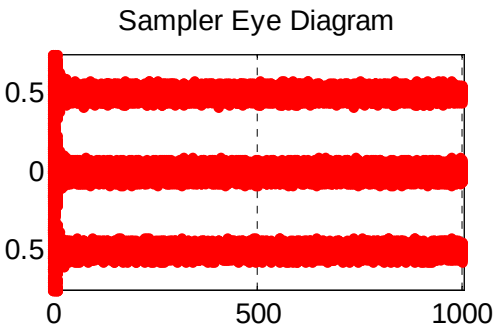
- Simulated results for channels equalized to PR-4 target polynomial
- Initial Eq estimate provided from channel response
  - Substitute for training sequence adaption
- Simulation conditions
  - Data Pattern: PRBS15, 100kbit sim time
  - NEXT/FEXT: off
  - Tx Pulse shaping: 4th Order Bessel Filtering
  - Rx Noise Filtering: None
  - Tx Eq: 8 tap FIR, 10b coeffs
  - Rx Eq: 5 tap DFE, 10b coeffs

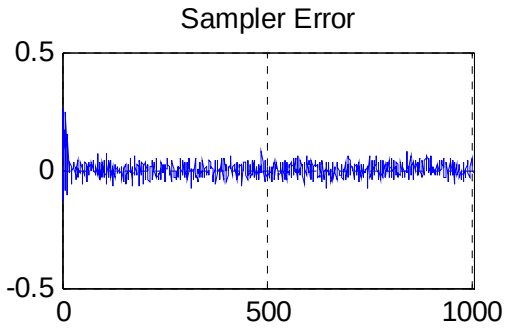
PR-4 Equalization Simulations – Tyco Case 5

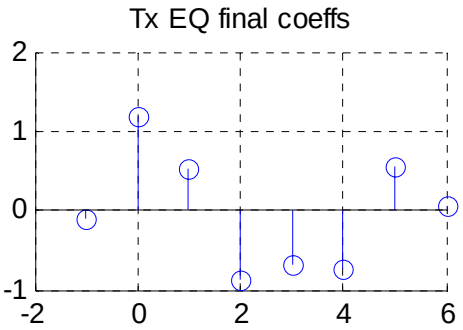


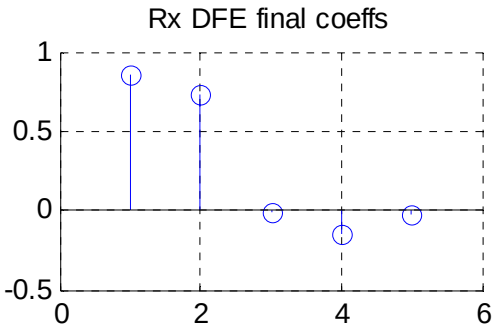






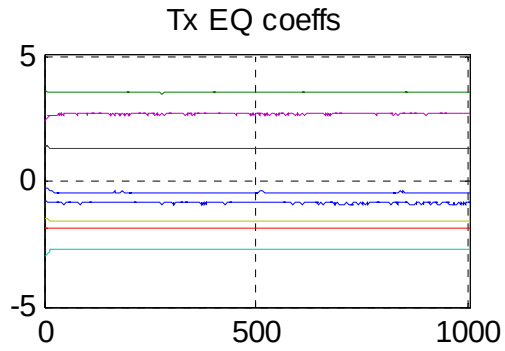


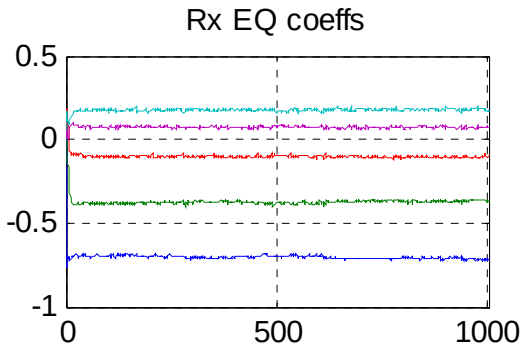


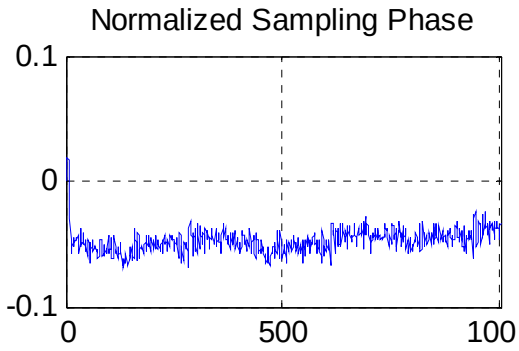


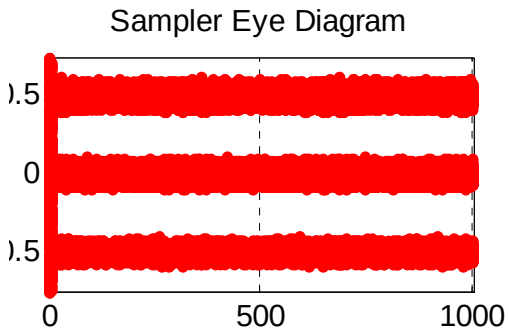
Channel model: tyco: Case5_DS_13_10_T_D13_L6

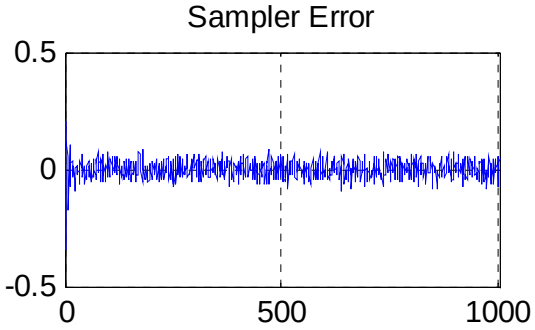
PR-4 Adaptive Eqn Sims – Intel T32

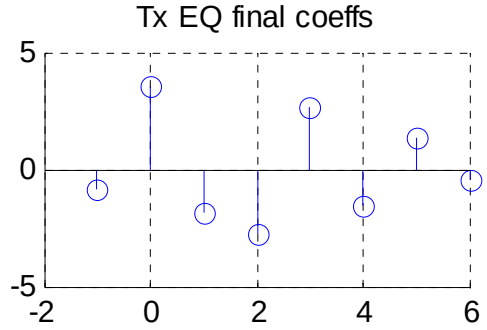


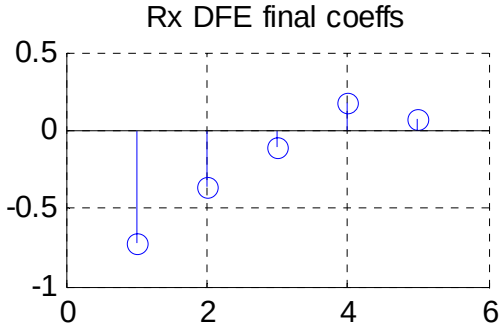








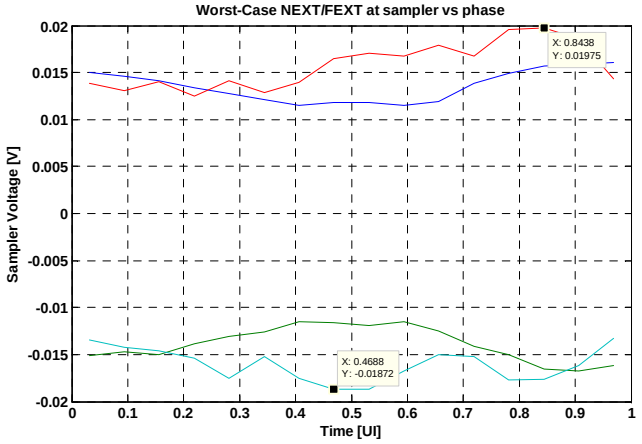


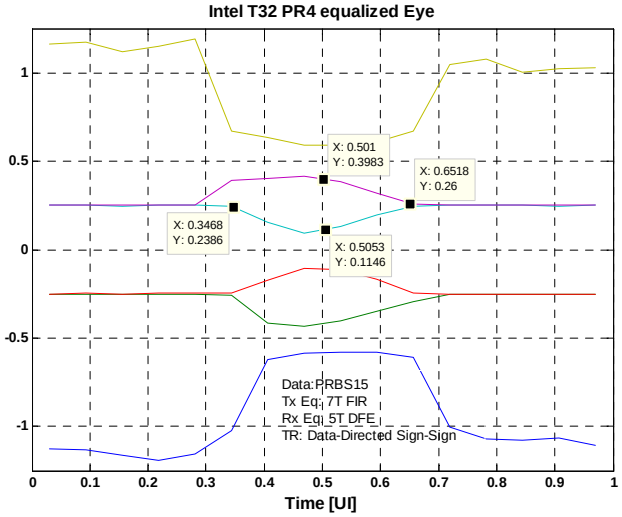


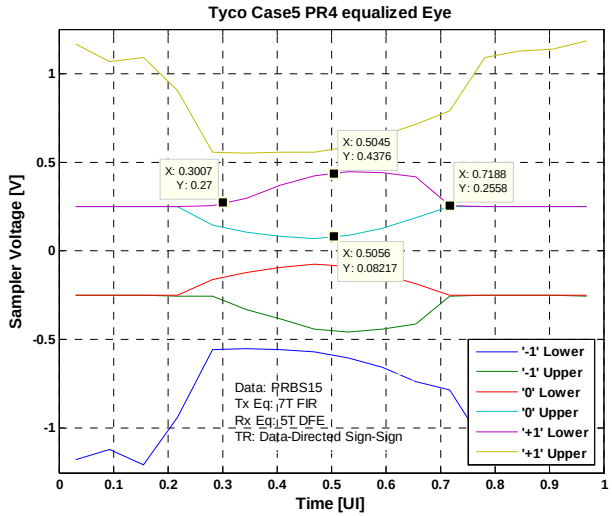
Channel model: Intel T32

PR-4 Equalization Simulations – Eye Diagrams

Channel	Eye width [UI]	Eye Height [V]	Max NEXT/FEXT [V_{p-p}]
Intel T32	0.154	0.205	0.205
Tyco Case #5	0.418	0.355	0.691







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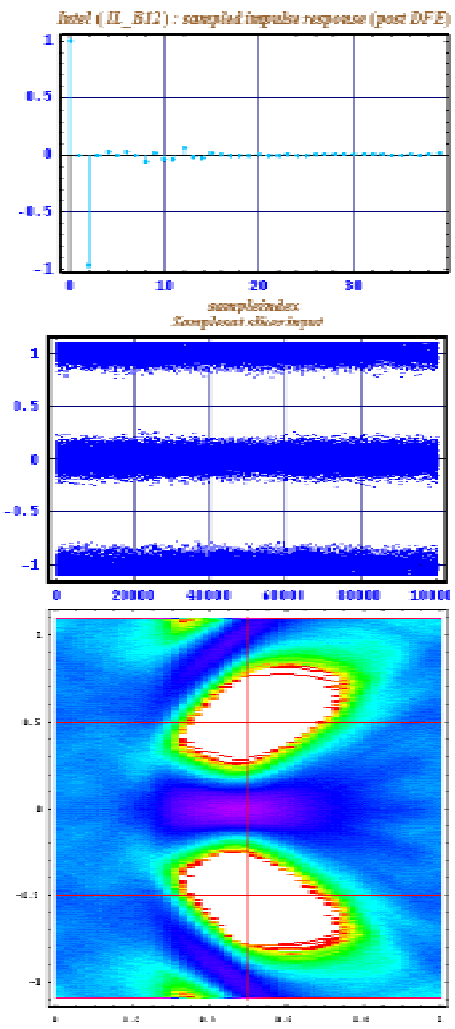
PR-4 Simulation Summary

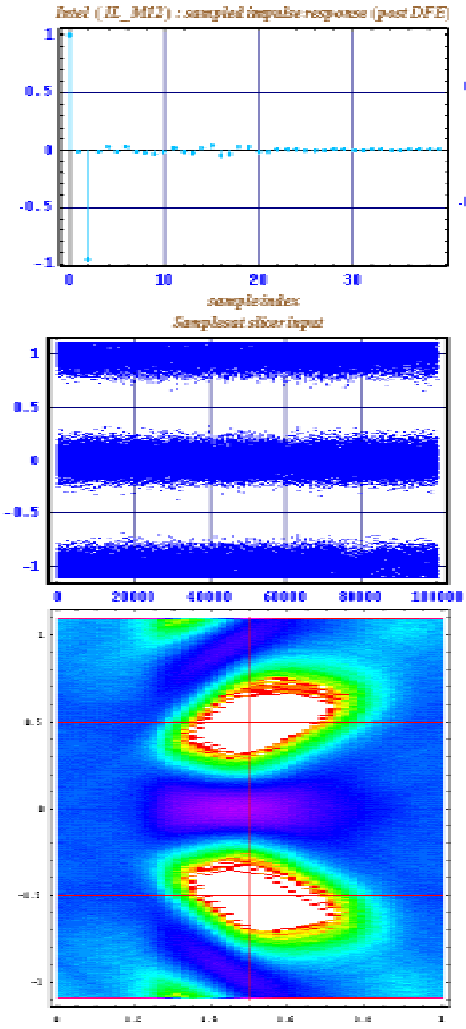
- **Simulation conditions:**
  - **Noise filter: 2nd order linear filter ω_0=6GHz & 10GHz**
  - **NEXT/FEXT & noise: None**
  - **Fixed coefficients, post-MMSE adaption**
  - **Linear tap values (no quantization)**

PR-4 Simulation Summary

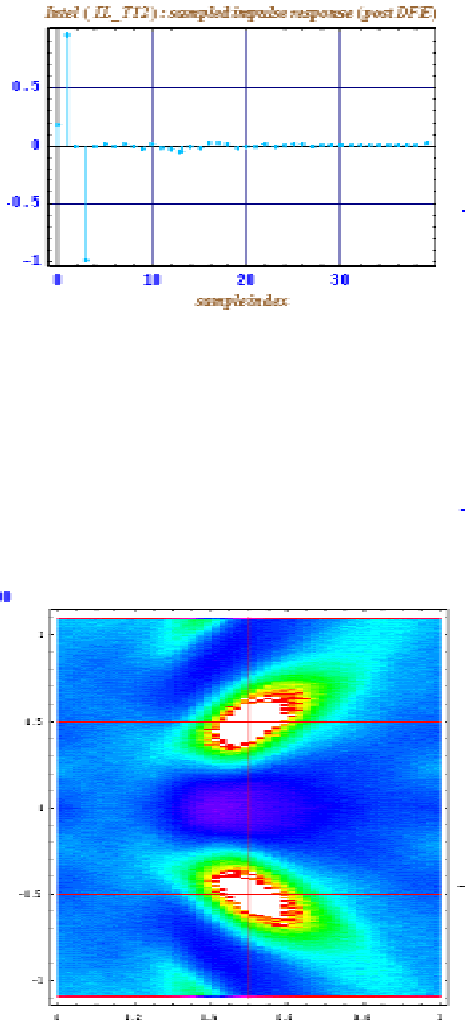
Intel B12



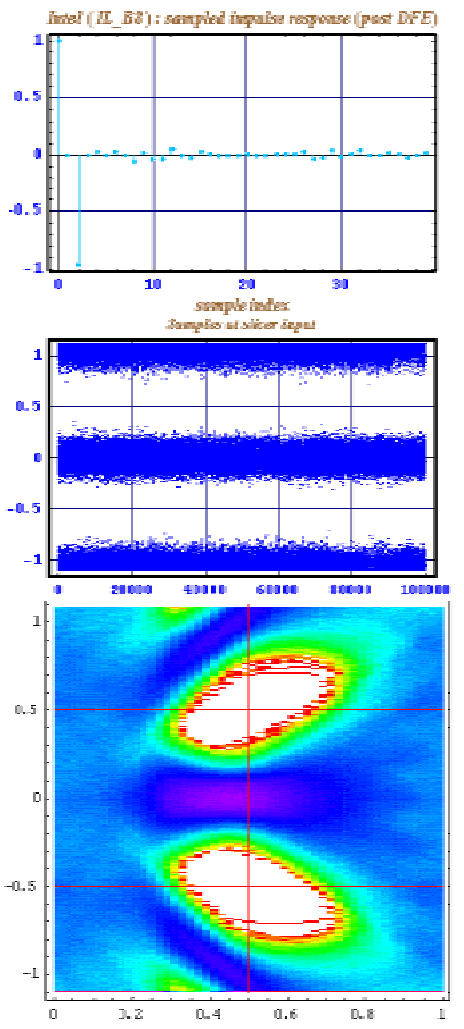
Intel M12



Intel T12

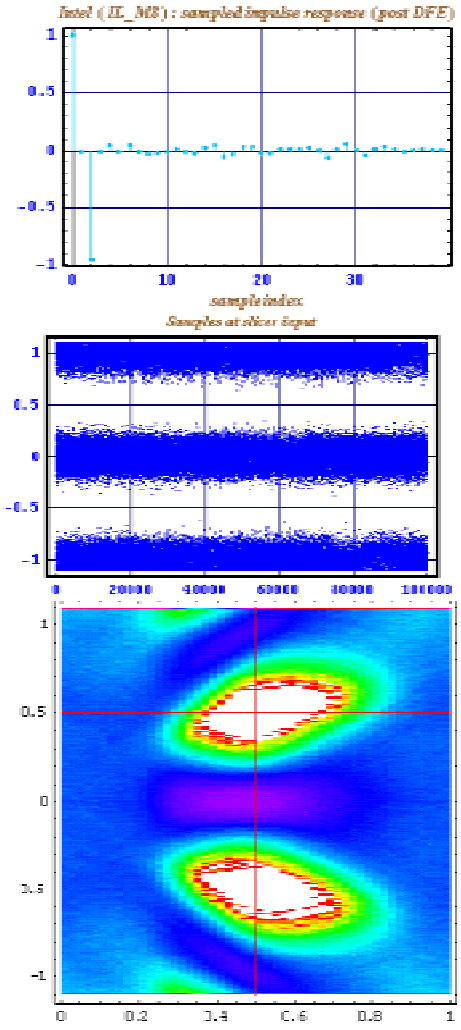


Intel B8

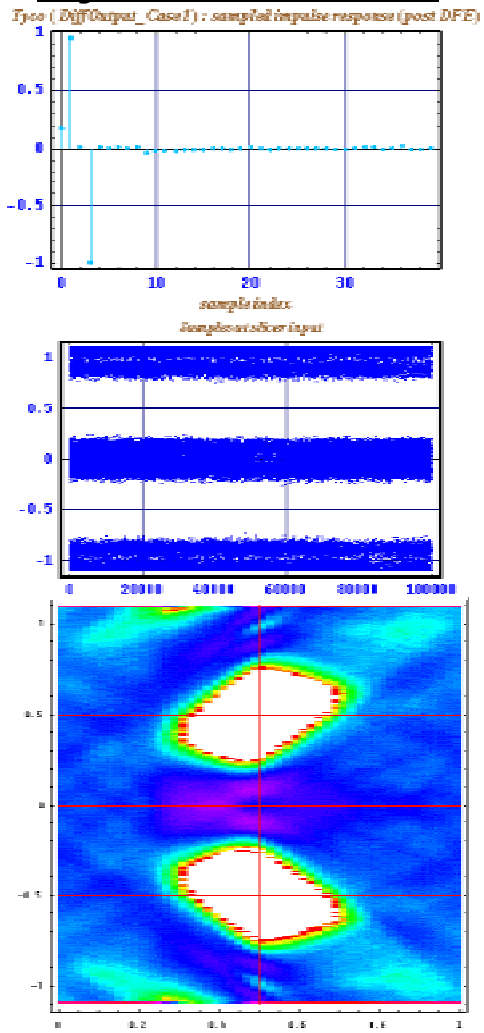


PR-4 Simulation Summary

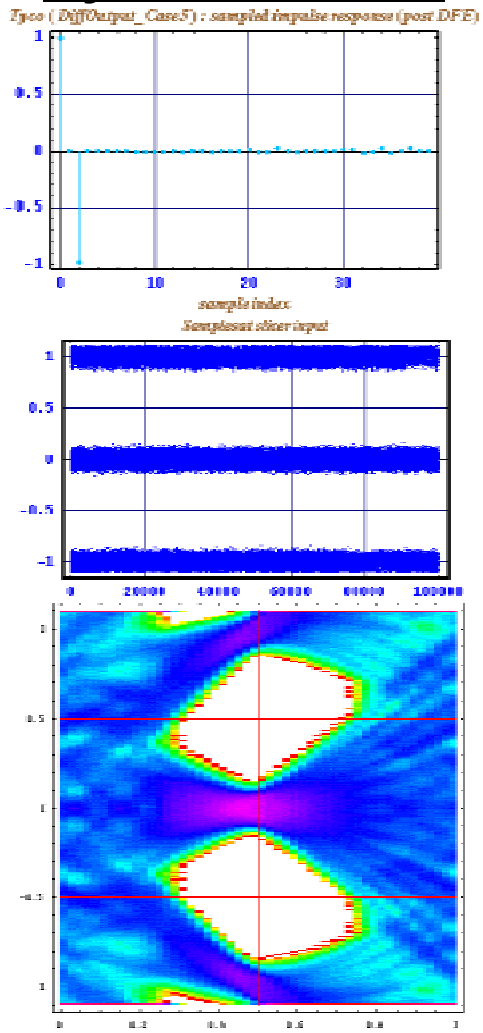
Intel M8



Tyco Case #1



Tyco Case #5



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PR-4 Simulation Summary – Eye Parameters

Channel	Eye width [UI]	Eye Height [V]
Intel Channels (Peters)		
Intel B12	0.314	0.461
Intel M12	0.277	0.341
Intel T12	0.154	0.205
Intel B8	0.264	0.343
Intel M8	0.261	0.288
Tyco Channels (D'Ambrosia)		
Case #1	0.315	0.506
Case #2	0.375	0.691

Summary

- Presented a PR-4 signaling proposal for 10Gbase-KR
- Leverages existing clauses for PCA, PMA and MDIO
- Leverages known PR-4 implementation advantages
- Includes Tx (FIR) and Rx (DFE) adaptive equalization
- Successful adaption simulations shown
- Successfully equalizes a range of Tyco and Intel (ATCA) backplanes