Transmitter Compliance Criteria

Justin Gaither

Xilinx

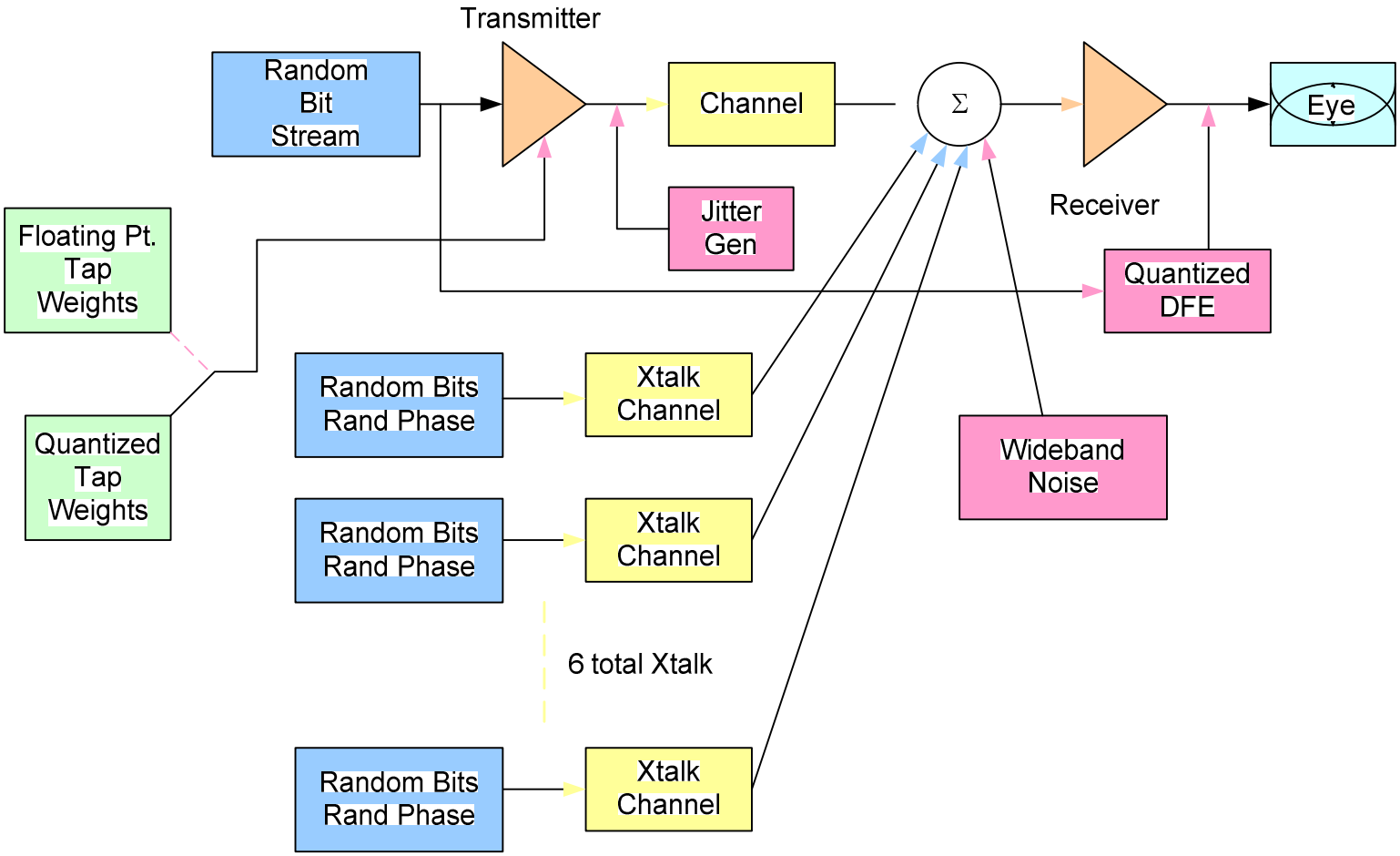
Acknowledgement

- Thanks to Steve Anderson for running a lot of simulations

Objectives

- Determine the sensitivity of the operational channel to small quantizational variation
- Reduce the amount of Transmitter Masks Required to test compliance

Block Diagram



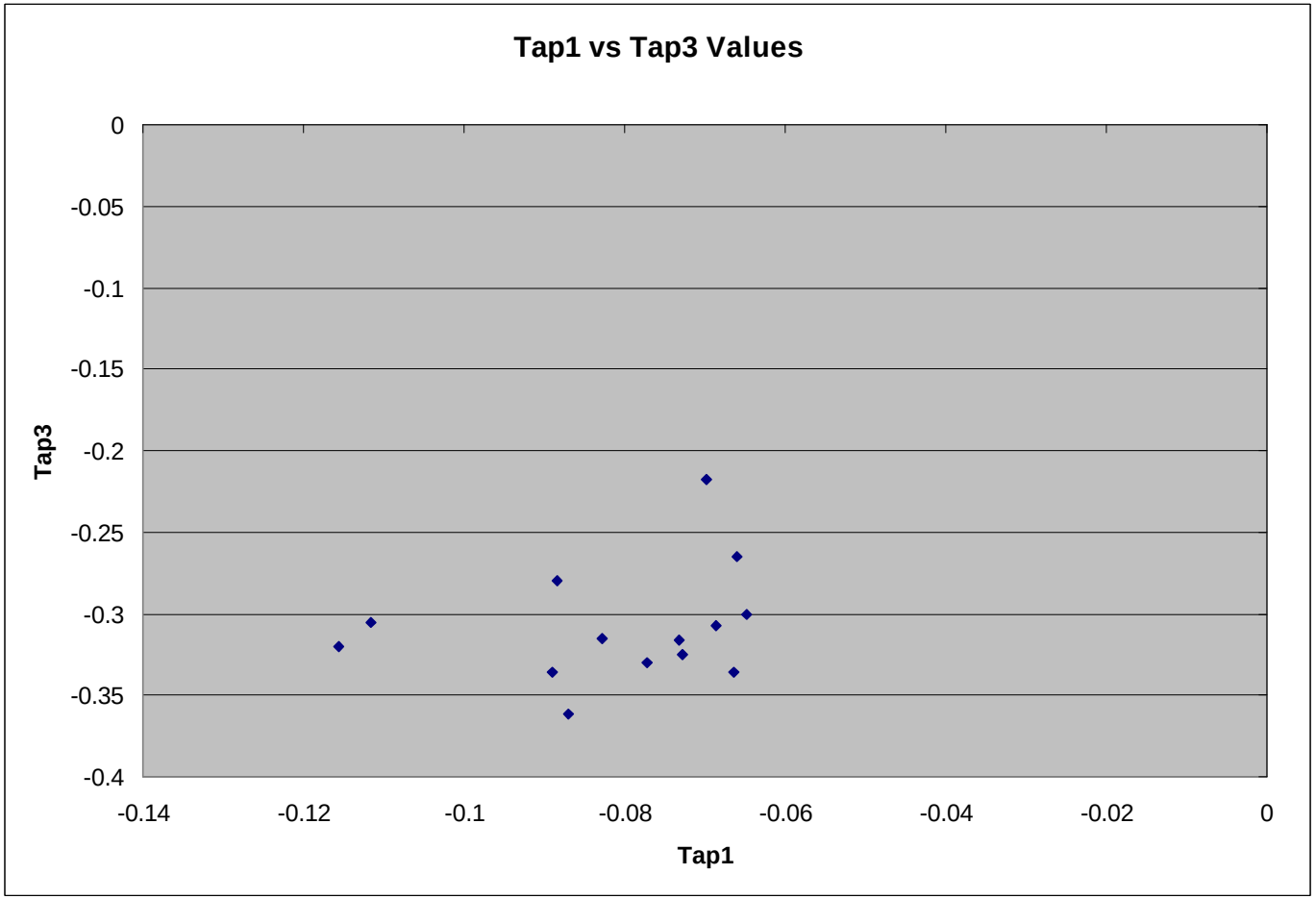
Simulation Conditions

- 1000 Bits, NRZ, 1000 mV ppd Tx, 10.0 Gbps
- Package Effects – 400 femtofarad each pin
- Tx Pulse Shaping – Single pole at 7.5 GHz
- Jitter 0.4UI @ 1.1Ghz phase modulation
- Eye measurements
  - Vert opening mV ppd
  - Horz opening UI pp
- Equalization
  - 3 tap FFE – one set floating point, one set quantized
  - 5 tap DFE, quantized to 32 levels based on min max across 33 channels, 50% guard band added
  - Find optimum FFE → Find DFE → Find quantized FFE & quantized DFE

Normalized Floating Point FFE Tap Values

Channel Name	Tap1	Tap2	Tap3
Intel B1	-0.06983491	0.712814645	-0.217350441
Test Case 5	-0.07326386	0.610075099	-0.316661041
Test Case 6	-0.11153067	0.582845364	-0.305623962
Test Case 7	-0.08834643	0.631636176	-0.280017397
Molex 25in BD	-0.07270781	0.602438885	-0.324853304
Molex 25in	-0.11566817	0.564497304	-0.319834528
Molex 40in BD	-0.08695185	0.551475325	-0.361572821
Intel B20	-0.07713113	0.592743197	-0.330125669
Intel M1	-0.06605248	0.669119083	-0.264828439
Intel M20	-0.08894216	0.57498331	-0.336074528
Intel B12	-0.06487174	0.635047856	-0.300080409
Intel M12	-0.08271189	0.602257237	-0.315030872
ERNI-long	-0.0664855	0.597873786	-0.33564071
ERNI-short	-0.06861709	0.623914941	-0.307467965

Plot Tap1 vs Tap3

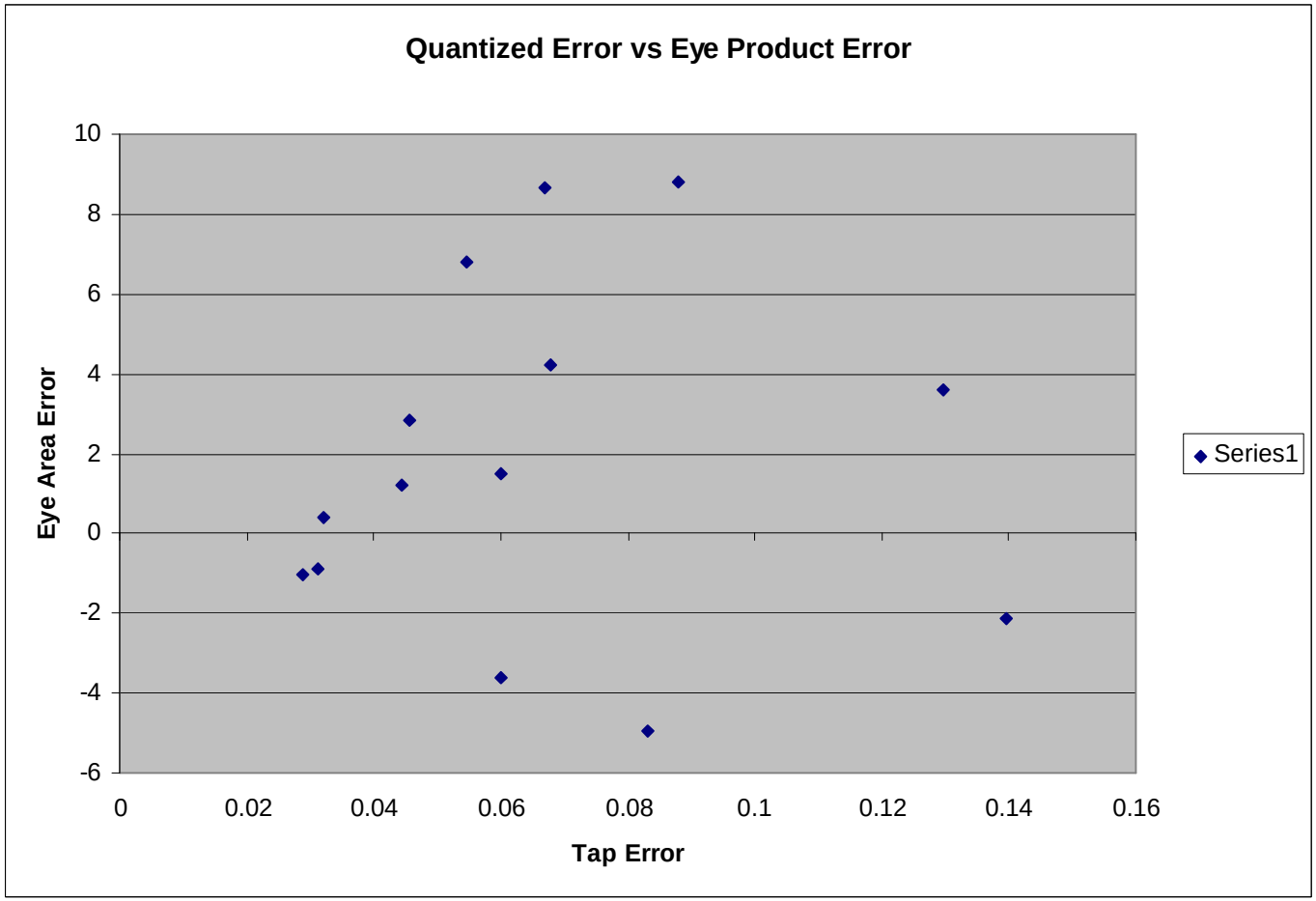


Quantized Tap Values

	Normalized Quantized Values			Error
				DFE Taps
Channel Name	Tap1	Tap2	Tap3	Error
Intel B1	0	0.75	-0.25	0.13967
Test Case 5	-0.1	0.58	-0.32	0.06015
Test Case 6	-0.1	0.58	-0.32	0.028752
Test Case 7	-0.1	0.65	-0.25	0.060035
Molex 25in BD	-0.1	0.58	-0.32	0.054584
Molex 25in	-0.1	0.58	-0.32	0.031336
Molex 40in BD	-0.1	0.58	-0.32	0.083146
Intel B20	-0.1	0.58	-0.32	0.045738
Intel M1	-0.1	0.65	-0.25	0.067895
Intel M20	-0.1	0.58	-0.32	0.032149
Intel B12	0	0.68	-0.32	0.129743
Intel M12	-0.1	0.58	-0.32	0.044514
ERNI-long	-0.1	0.58	-0.32	0.067029
ERNI-short	-0.1	0.58	-0.32	0.08783

	Non-Quantized FFE			Quantized FFE					
	Vertical Eye at Slicer (mV ppd)	Hor Eye at Slicer (UI)	Horz*Vert	Vertical Eye at Slicer (mV ppd)	Hor Eye at Slicer (UI)	Horz*Vert	Vertical Error	Horizontal Error	Product Error
	5	5		5	5				
Channel Name									
Intel B1	145	0.532	77.14	144	0.521	75.024	-1	-0.011	-2.116
Test Case 5	54	0.576	31.104	58	0.562	32.596	4	-0.014	1.492
Test Case 6	30	0.44	13.2	35	0.347	12.145	5	-0.093	-1.055
Test Case 7	79	0.577	45.583	72	0.583	41.976	-7	0.006	-3.607
Molex 25in BD	73	0.581	42.413	79	0.623	49.217	6	0.042	6.804
Molex 25in	39	0.509	19.851	35	0.542	18.97	-4	0.033	-0.881
Molex 40in BD	32	0.607	19.424	29	0.499	14.471	-3	-0.108	-4.953
Intel B20	47	0.551	25.897	54	0.532	28.728	7	-0.019	2.831
Intel M1	60	0.422	25.32	71	0.416	29.536	11	-0.006	4.216
Intel M20	23	0.308	7.084	24	0.312	7.488	1	0.004	0.404
Intel B12	65	0.556	36.14	75	0.53	39.75	10	-0.026	3.61
Intel M12	48	0.49	23.52	51	0.485	24.735	3	-0.005	1.215
ERNI-long	46	0.563	25.898	57	0.606	34.542	11	0.043	8.644
ERNI-short	75	0.637	47.775	100	0.566	56.6	25	-0.071	8.825

Quantizing Error vs Eye Product Error



Proposed FFE Tap Values to Build Masks

Tap 1	Tap 2	Tap 3
0	1	0
0	0.75	-0.25
0	0.68	-0.32
-0.1	0.65	-0.25
-0.1	0.58	-0.32

Conclusion

- Shown that the channel performance is not very sensitive to Quantization of FFE taps
- 3 Mask tests can be generated to verify compliance of TX.
- These 4 values can be used as part of Reference TX as part of the Channel Model
- Simplifies TX compliance testing
- Since most TX will have more granularity, this would only improve interoperability