AN Data Detect Timer Values

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Supporters

- XXXX
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The Issue

In Table 73-6 :

- **The AN *interval_timer* is specified as**
  - 3.2ns ±0.01%
- **Whereas the data detect timers are specified as**
  - *data_detect_min_timer* : min 1.6ns, max 2.4ns
  - *data_detect_max_timer* : min 4.0ns, max 4.8ns
- **So although the Tx'ed center of the DME cell can only vary ±0.01% the timers require that a variation of ±25% MUST be accepted at a Rx'er.**

  - This is an unnecessary burden on implementations

DME cell timing in perspective

- **DME signalling will be parsed from the parallel output of a SERDES**
  - No-one wants to add analog circuitry for DME Auto-negotiation !

- **3.2ns =**
  - 4 baud @ 1.25Gbd (4 bits of a 10bit SERDES output word)
  - 10 baud @ 3.125Gbd (10 bits of a 10bit SERDES output word
  - 33 baud @ 10.313Gbd (33 bits of a 33(?)bit SERDES output word)

- **± 1 rx'ed bit =**
  - 3.2ns ±25% @ 1.25Gbd
  - 3.2ns ±10% @ 3.125Gbd
  - 3.2ns ±3% @ 10.313Gbd

  - 0.01% of 3.2ns = 0.33% of a rx'ed bit at 10.313Gbd
    - Will be swamped by CDR effects (which will be limited to ~ ±1 bit)

- **± 25% @ 10.313Gbd = ± 8bits**
  - Current timer values require an implementation to check for and accept a transition at any one of 2x8+1=17 locations in the SERDES word, when only ±1 (3) locations need be checked.

AN Data detect timer value proposal

- **Change the data detect timers specs to:**
  - *data_detect_min_timer* : min 1.6ns, max 3.2ns-3%
  - *data_detect_max_timer* : min 3.2ns+3%, max 4.8ns
- **This narrows the window in which implementations must guarantee to accept a transition to ±3% from the center of the DME cell versus the current ±25%.**
  - This does not require all implementations to have ±3% detection accuracy – it merely allows a ±3% implementation to be compliant
- **Retaining the same outer limits means implementations that allow the transition to be up to ±50% away from the cell center remain compliant**