Report from TP3 Conference Calls

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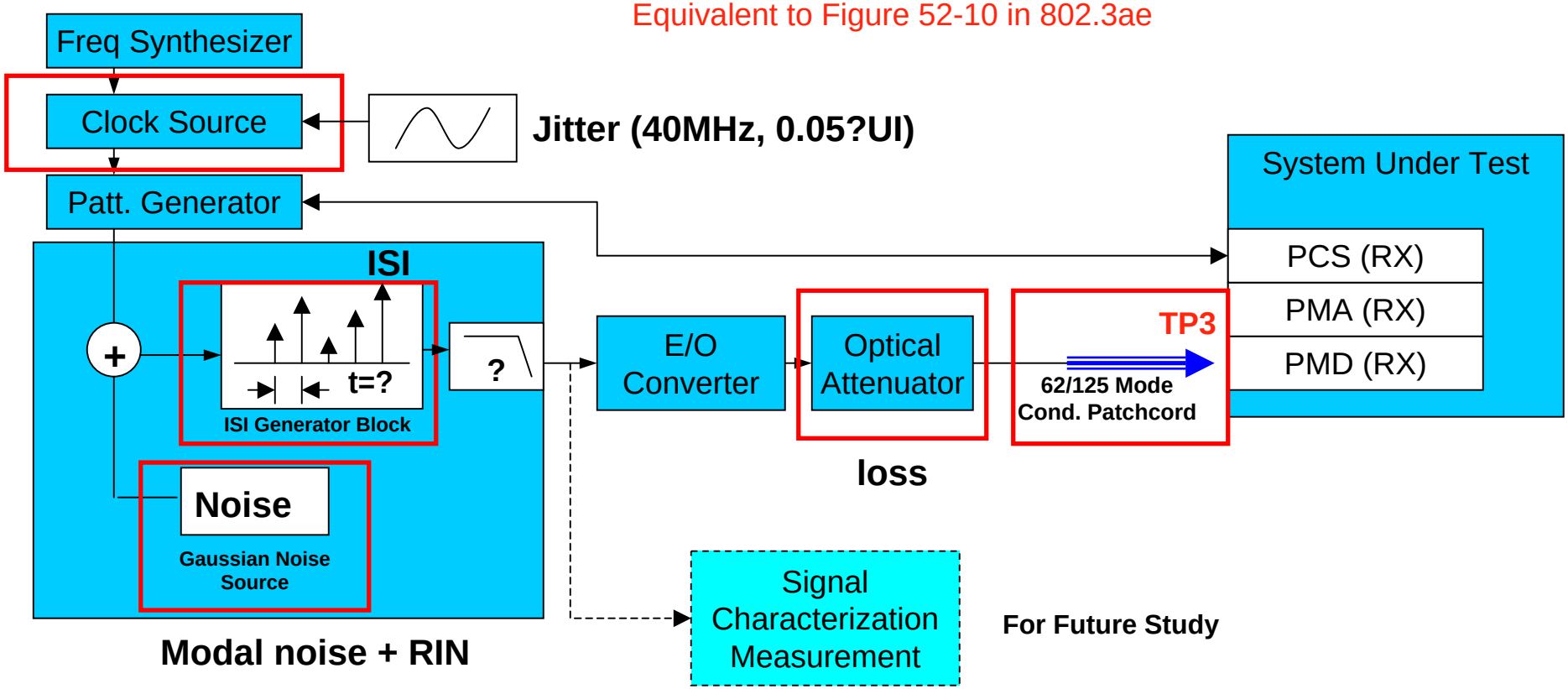
Report from Conference Calls on TP3 Specification

- **Summary diagram for current test**
- **TP2 and the Link Budget**
- **Jitter testing**
- **SNR calculations**
- **Dynamic adaptation test**
- **Conclusions and Further Work**

Latest Stressed Receiver Sensitivity Test Proposal

Equivalent to Figure 52-10 in 802.3ae



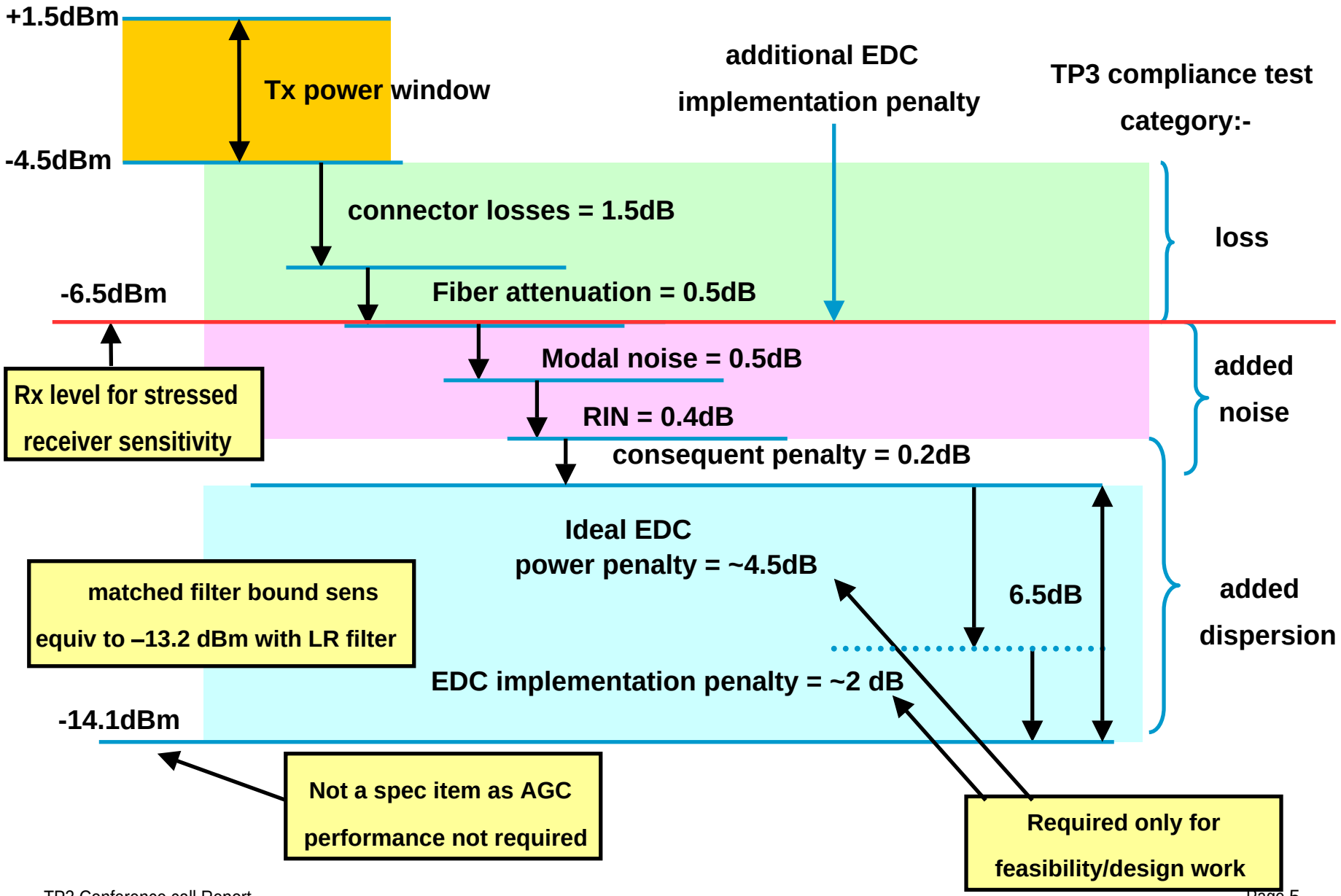
- **Leverages strongly off 10GBASE-LR**
- **Motivated to keep it simple whilst still represent all the key stressors**
- **Motivated to have practical test with reproducible results**

TP2 and the Link Budget
presentation from Tom Lindsay (Oct 19)

- **The TP3 conference call group agreed the following:-**
  - **TP2 and TP3 testing should both be test configurations which seek to represent the relevant aspects within the link budget**
- **We have a link budget from the Oregon meeting.**
  - **http://ieee802.org/3/aq/public/jul04/lawton_1_0704.pdf**

- **The TP3 group has agreed and is working with the following updates to the budget:-**
  - **connector losses can be reduced from 2.0 to 1.5dB**
  - **Fiber attenuation needs to be increased from 0.4 to 0.5dB**
  - **Rx dynamic adaptation penalty incorporated into the EDC implementation penalty**
    - **This now appears below the "waterline"**
  - **Consequent penalty moved below the "waterline"**
  - **Ideal equalizer penalty + implementation penalty = 6.5dB**

Interpreting the EDC Link Budget (OMA)



"Jitter Tolerance for Receiver Stressed Sensitivity Test" presentation from Petre Popescu (Oct 26)

3. Jitter Sources and Impact on the Receiver Test

Jitter Source	Jitter Characteristics	Receiver impact	10GBASE-LRM Receiver
Transmitter clock, random jitter	High peak-to-peak amplitudes at low frequencies	The recovered clock will track the incoming jitter	Needed EDC will not correct
Laser random jitter	Small peak-to-peak amplitudes at low frequencies, uniform distribution at high-frequency	The recovered clock will not track the high-frequency incoming jitter	Needed EDC will not correct
Transmitter, pattern (data) dependent jitter (correlated)	Transmitter bandwidth limitation and phase non-linearities (ISI), high frequency components, (above 10 LB*)	The recovered clock will not track the high-frequency incoming jitter	Negligible compared with the channel contribution. Partially reduced by EDC.
Channel jitter contribution	Small for SMF, not generated in the "stress conditioning", for 10GBASE-L.	Equalizer required for MMF.	Not needed. Jitter generation is included in the "non-quasi-symmetrical stressed signal generator".

*LB - PLL loop bandwidth.

Jitter Testing choices …

1. **Define mask and leave it to the implementer to determine appropriate testing**
2. **Define mask and advise a single frequency for stressed receiver testing.**
3. **Use of a PRBS to simultaneously modulate the Tx source with broadband jitter**

- **Group agreed to define a test in line with option 2:-**
  - **40MHz, 0.05?UI source for stressed receiver normative test**
  - **include a separate low frequency test, 40kHz 5UI**

SNR Calculations
(Contributions from Aronson and Weiner, Nov 2 & 9)

- **The purpose of the work is to establish the SNR required at the Rx given that both Modal noise and RIN are represented by additional noise power penalties**
- **Calculation carried out with 2 techniques:-**
  - **Lew Aronson for non-equalizing case with ISI**
  - **Nick Weiner for a channel with ISI and a perfect equalizer**

- **Both techniques were in close agreement and yielded a figure of 11dBo SNR for Modal noise and RIN power penalties totaling 0.9dB**
  - **RIN power penalty figure (0.4dB) is directly calculated from –128dB/Hz spec**

- **Also agreed to define S/N with the ISI OFF:-**
  - **consistent with TP2**
  - **avoids issues with different channels having different “gains”**

TP3 Dynamic Adaptation Test (Contribution from Lew Aronson, Nov 9)

- **Current position: Draft 0.2 has a Dynamic Adaptation Penalty Test**
  - **The channel adhoc (Task 2) has determined that the rate of change for the time varying nature of the channel is slow … of the order of 10Hz**
  - **The EDC vendors believe this rate of change will not represent an issue**
- **Proposal**
  - **For the link budget incorporate adaptation penalty within EDC implementation penalty**
  - **For the TP3 testing replace existing penalty test with a dynamic adaptation test designed to ensure the equaliser can transition between states without error floors**
    - **Test to be done with channel changing at 30 Hz between pre-cursor and post-cursor channels**
    - **Test to be kept as simple as possible**
      - **No jitter or noise loading**
      - **ISI limits to be challenging but simpler than static test (3 peak vs 5)**

Conclusions and Further Work

- **Key Progress since last meeting:-**
  - **Agreed parameters for jitter testing**
  - **Determined approach for representing power penalties with reduced SNR**
- **Further Work items:-**
  - **Select appropriate channels for compliance testing**
  - **Determine methodology for measuring OMA**
  - **Work with TP2 to refine link budget (primarily above the “waterline”)**
  - **Finalize simplified normative and informative tests**
  - **Finalize dynamic adaptation test**
  - **Build and validate tests**