TP2 Impairments and tests

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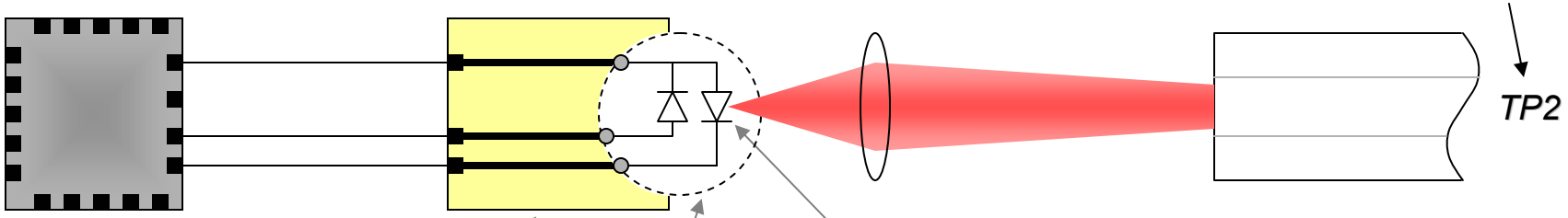
9/9/04

TP2 components & impairments

Specification defined only at TP2
(everything else is implementation detail)



Clock
- Crystal
- Synth

Driver
- III-V
- SiGe
- CMOS

Interconnect
- Rogers, etc.
- FR-4

Attach
- Flex
- Leads

Package
- Microwave
- TO-can

E/O
- EML
- DFB
- FP
- VCSEL

Optics
- Isolator
- Lens

MMF
- *Launch conditions outside scope*

Decreasing cost

Clock
- RJ
- Other jitter

Driver
- Edge rates
- Overshoot and ringing
- RJ & other jitter
- DDJ
- DCD
- Additive noise

Electrical coupling
- Frequency loss
- Reflections and resonances
- Crosstalk pickup

Laser
- Edge rates
- Overshoot and ringing
- DCD
- *Difference* in rising and falling edges rates
- *Difference* in overshoot and ringing
- RIN on logic 1
- RIN on logic 0
- Spectrum (λ dispersion)

Optics
- Geom dynamics?
- λ dynamics?

Original drawing by John Ewen, JDSU

Categorization of impairments

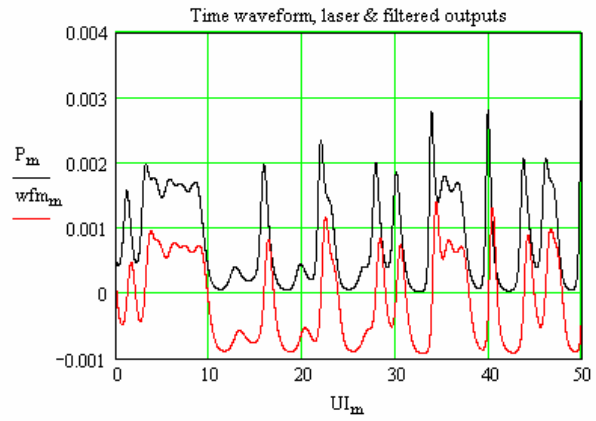
		Correlated	Uncorrelated	Correctable	Uncorrectable
Clocking					
	RJ		X		X
	Other contributed jitter		X		X
Driver					
	Edge rates	X		X	
	Overshoot and ringing	X		?	
	Contributed RJ & other jitter		X		X
	Contributed DDJ	X		X	
	DCD	X			X
	Additive noise		X		X
Electrical coupling					
	Frequency loss	X		X	
	Reflections and resonances	X		?	
	Crosstalk pickup		X	?	
Laser	Edge rates	X		X	
	Overshoot and ringing	X		X	
	DCD	X			X
	Difference in rising and falling edges rates	X			X
	Difference in overshoot and ringing	X			X
	RIN on logic 1		X		X
	RIN on logic 0		X		X
	Spectral dispersion	X		X	
Optical coupling					
	Geometric dynamics?				
	Spectral dynamics?				

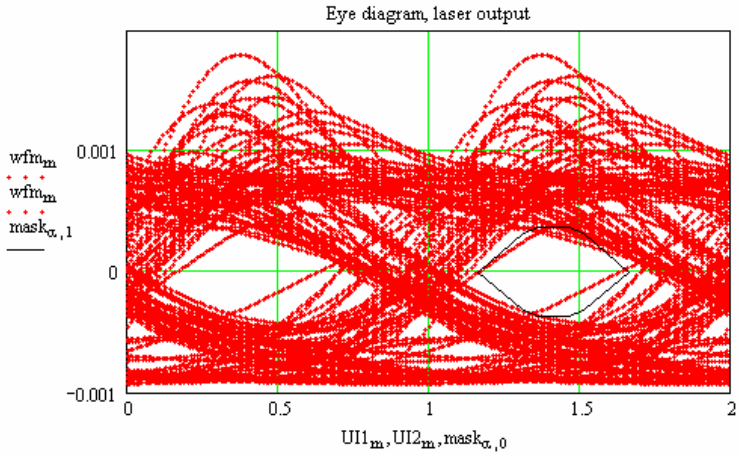
Categories require different tests?

- Proposal for correctable
  - Use scope averaged waveform capture for data dependent effects
  - Run waveform through simulated channel and simulated “standard” EDC Rx to determine power penalty vs. spec/limit
    - Easier than LR – does not HW dispersion, reference Rx, or reference Tx
    - Penalty vs. “perfect” Tx, same simulate channel
    - Relative test, so does it matter which channel? Is a channel even required?
    - Standard EDC Rx TBD
  - Use some portion of intermediate pattern per 802.3ae
    - TBD, penalty limit would be a function of exact pattern used
  - Requires pattern trigger (& perhaps sub-pattern recognition?)
  - Impose penalty back onto transmitter OMA (per TDP)?
- Proposal for uncorrectable
  - Use mask test
    - Similar complexity as for LR
    - Start with –LR mask?
  - Use square wave pattern per 802.3ae to avoid data dependent effects
  - Requires clock recovery trigger
  - Tighten X1 for uncorrelated jitter?
- Budget must account for both; specs/tests must align with budget

Examples

- PRBS pattern, penalty unknown





- Mask test with square wave, barely passes…