Implications of Finite Equalizer Penalties for TP3 Sensitivity Testing

Comments on the "sieve" method adopted in Vancouver for selecting IPRs for the normative receiver sensitivity test

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Summary

- Points on which there is no disagreement:
  - ➢ The use of PIE-D as the basic metric to rank order impulse responses is fine. This respects the fact that chip designers may employ various equalizer architectures and cannot disclose this information publicly.
  - ➢ It is not the place of the standard to specify the architecture of the equalizer, but rather to test and validate that an equalizer works for IPRs near the 99th %-tile level.
  - ➢ The "sieve" for selecting one IPR for the stressed sensitivity test from each of three categories (pre- and post-cursor and quasi-symmetric) is a good method.

- Previously, I raised the concern on the reflector on 11/30-12/1 that the selection of IPRs for receiver testing should be guided in some way by the realities of finite equalizer performance. Opinions were expressed by several (Vivek Telang, Martin Lobel, Lars Thon) in favor of including finite equalizer performance in some way, but others argued strongly against it.

- It is proposed here that the IPR selection procedure (sieve) outlined in mcvey_1_0105, page 3 should include an additional step. After selecting IPRs within a given range of PIE-D (step2) but before sorting (step3), we should rank order the IPRs by the finite equalizer penalty incurred by a relatively "short" DFE [e.g. 8(T/2)+3] and retain only those in the top quarter of difficulty.

- We suggest this additional step is necessary to justify retaining only one IPR from each of the three categories (pre-, post-cursor, and quasi-symmetric).

Basic Concerns

- It should be agreed by all that, in general, PIE-D correlates better with the ideal, finite equalizer penalty for a DFE with a large number of taps as compared to a DFE with a smaller number of taps. ("Large" and "small" are relative to the widths of the IPR's in the set under consideration.)

- For a given set of IPRs characterized by similar PIE-D values, the difference between PIE-D and an ideal finite equalizer is smaller – on average – and more tightly distributed for a "longer" DFE than for a "shorter" DFE.

- For example, in the next slides, it will be shown that, for a set of IPR's having similar PIE-D values:
  - The dispersion power penalty for a "longer, ideal DFE" such as 12(T/2)+5 ranges from ~ 0.1-1dB in excess of PIE-D.
  - The disperion power penalty for a "shorter, ideal DFE" such as 8(T/2)+3 ranges from ~ 0.2-2dB in excess of PIE-D.

- This implies that any one of many IPRs with similar PIE-D will adequately test the capabilities of a "longer" equalizer. However those IPR's are not all equivalent with respect to testing a "shorter" DFE, given a limited implementation penalty for finite lengths in the link budget.

Methodology

- Total dispersion penalty limits:
  - ➢ The total penalty allowed is 6.5dBo (this includes connectors)
  - ➢ PIE-Ds are computed assuming an allocated dispersion penalty of 6.5dBo

- Use TP3 compliance test pulses defined in section 68.6.9

- For each of the IPRs specified as sums of four components in the TP3 set
  - ➢ Compute PIE-D's
  - ➢ Determine the dispersion penalty for different finite-length equalizer configurations

- Determine the minimum complexity equalizer that will result in total penalty < 6.0dBo for the TP3 set, allocating 0.5 dB of the implementation penalty to hardware as an example.

- For the large-scale 1998 fibers from balemarthy_1_0105, assess additional penalty due to finite-length equalizers

Minimum Complexity Equalizer for the TP3 Test Pulses
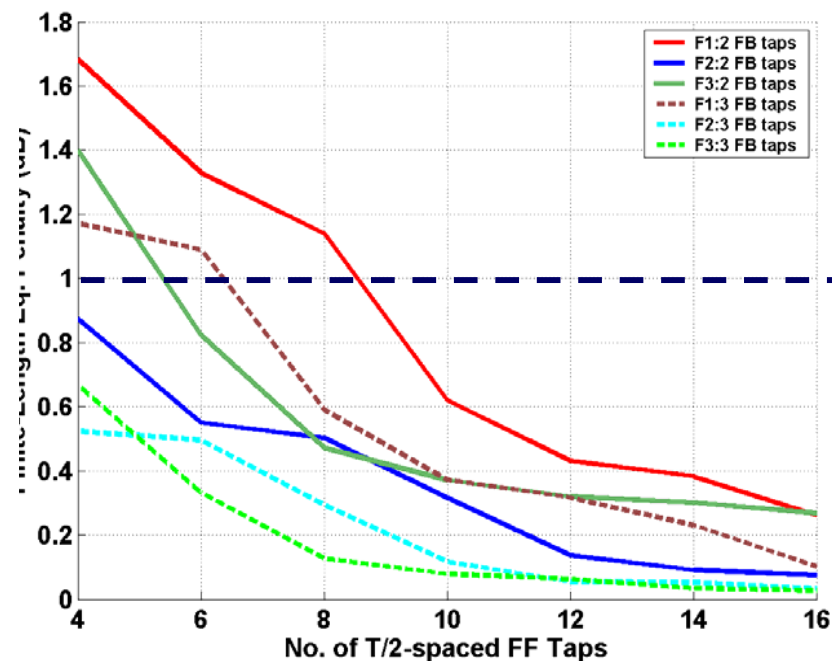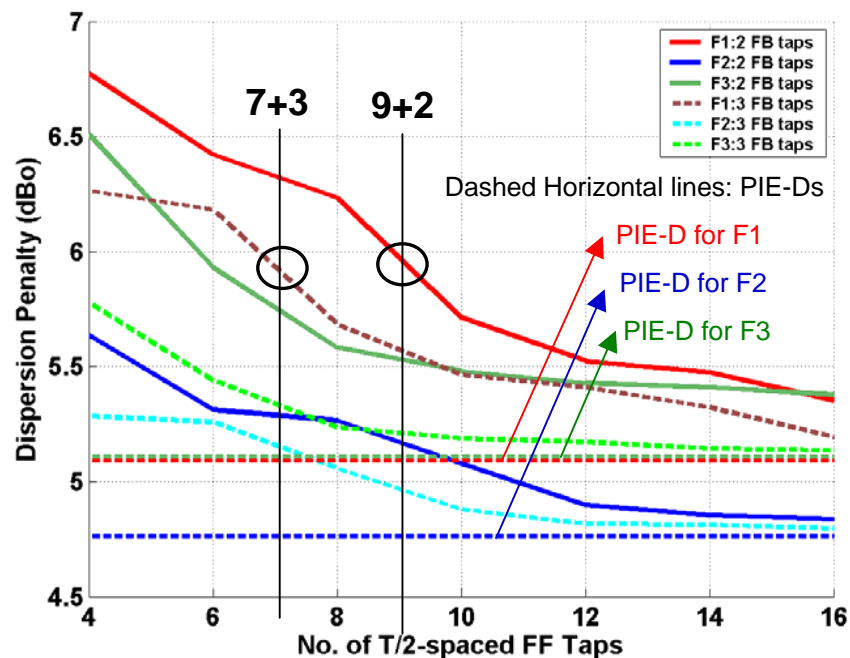
- Fiber nomenclature and corresponding PIE-Ds:
  - Fiber F1: pulse with pre-cursor ISI, PIE-D curve is red dashed, horizontal line
  - Fiber F2: symmetric pulse, PIE-D curve is blue dashed, horizontal line
  - Fiber F3: pulse with post-cursor ISI, PIE-D curve is green dashed, horizontal line

- Minimum complexity finite-length DFEs that satisfies total penalty < 6.0dBo (see left panel) for TP3 test impulse responses:
  - Allocates 0.5 dB to hardware penalty alone, leaving 1.5dB for finite length effects
  - **7 FF taps (T/2-spaced) + 3 FB taps** (interpolated) (has a ~0.1dB margin from 6.0dBo)
  - **9 FF taps (T/2-spaced) + 2 FB taps** (interpolated) (has a ~0.1dB margin from 6.0dBo)

- Note that the finite-length portion of the implementation penalty (y-axis of right panel) for these configurations is approx. 1dB for fiber F1 for the minimum complexity equalizers (interpolating for odd # of FF taps) and approx. 0.5dB for F2 and F3
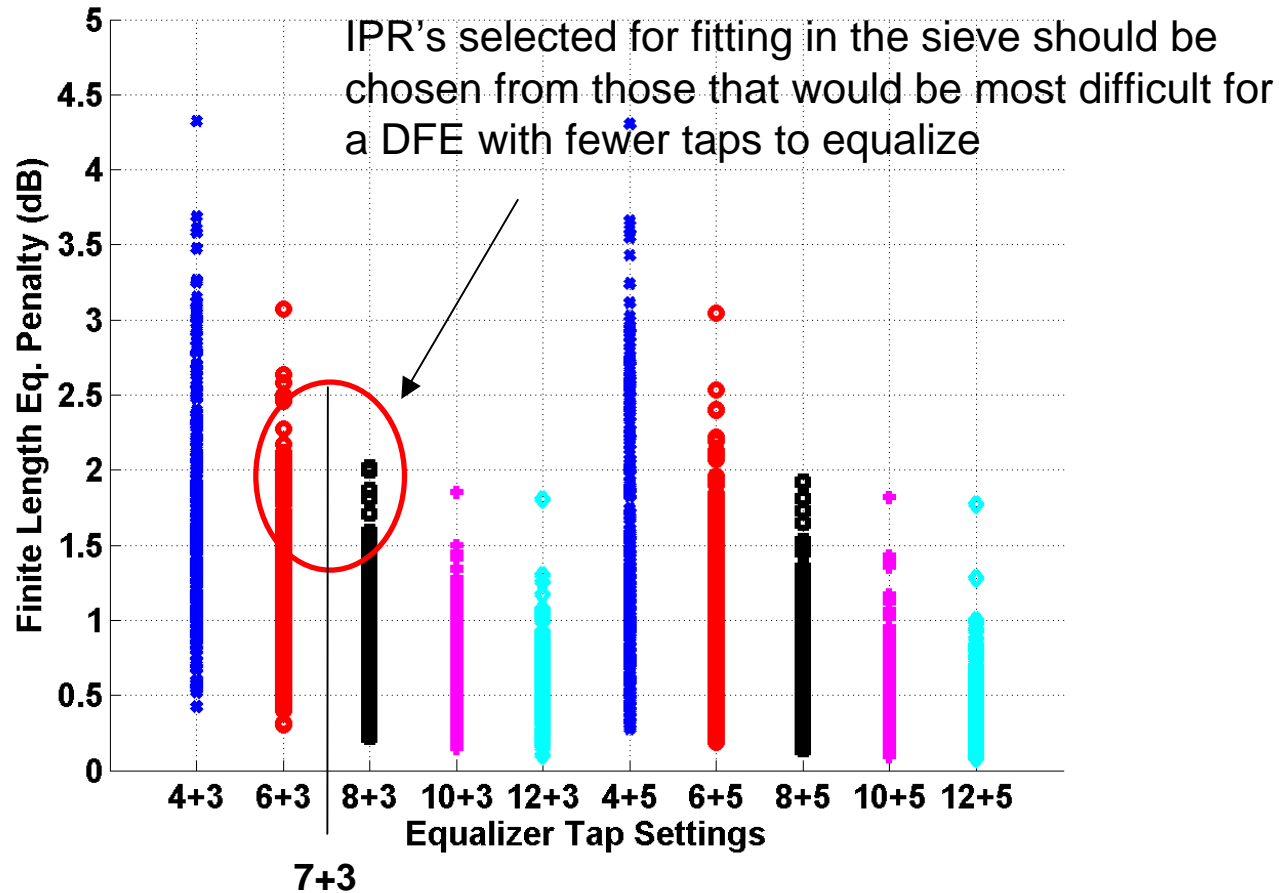
Explanation of Results Presented

- The following slides reference the large 1998 fiber set from balemarthy_1_0105 where DMD data from measured fibers was used to estimate PIE-D coverage of the installed base.

- In order to compare with the TP3 sieve method in bhoja_1_0105, only IPRs which give PIE-D in the range of 4.5 to 5.0 were selected.

- It does not matter much which fiber set we use here, since we are only trying to illustrate a point about finite equalizer penalties vs. PIE-D. (The same analysis on the Monte Carlo set with connectors should yield a similar conclusion.)

- The chart on the next slide (page 7) shows the *spread* in finite-length implementation penalty for various DFE cases. The range in PIE-D is selected to be 4.75+/- 0.25 dB. The spread in the finite-length implementation penalty is at least 1dB (e.g. 12(T/2)+5 case) and much larger if DFE has smaller number of taps.

- The chart on slide 8 quantifies that the minimum complexity equalizer for the TP3 IPR set (ideal 7(T/2)+3 DFE) – applied to the 1998 fiber set – will show finite-length implementation penalties > 1dB over and above PIE-D 50% of the time, ranging above 2dB ~5% of the time. A "long" 12(T/2)+5 DFE has penalty within 1dB of PIE-D almost 100% of the time.

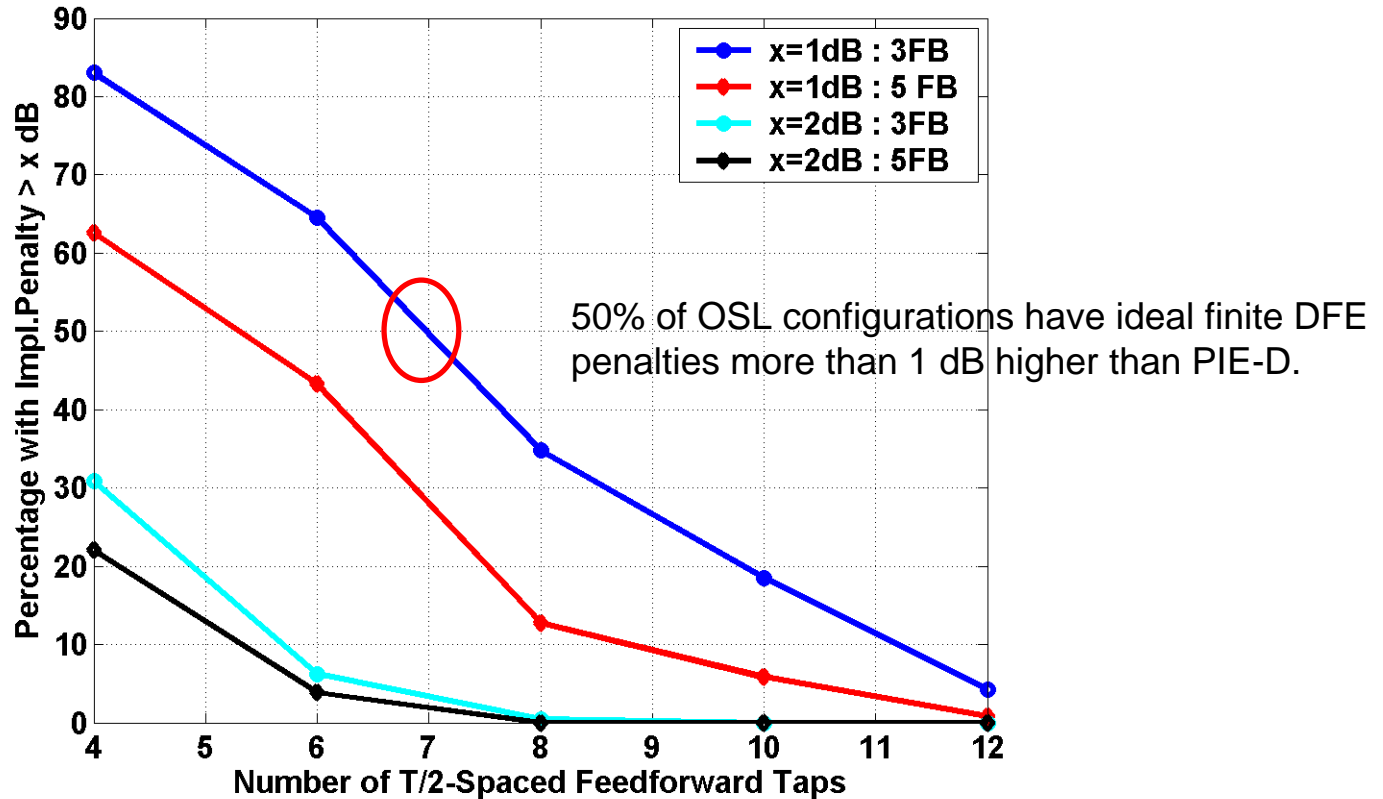# Select only IPR's from 1998 fiber set for which 4.5dBo <= PIE-D <= 5.0dBo

IPR's selected for fitting in the sieve should be chosen from those that would be most difficult for a DFE with fewer taps to equalize

- For a shorter DFE, such as the $7(T/2)+3$ minimum complexity equalizer for TP3 test impulses (slide 5), it is possible for the finite DFE power penalty to exceed PIE-D by 2dB or more, *prior* to considering the hardware implementation penalty.
- Ranking IPRs for TP3 testing by PIE-D alone will not sufficiently test short DFEs
- In fact a $7(T/2)+3$ DFE would succeed on the TP3 IPRs, while failing on a number of the IPRs represented above. This eventuality should be prevented.

Percentage Finite-Length DFE Penalty above 1 and 2dB,
where $4.5dBo <= PIE-D <= 5.0dBo$

50% of OSL configurations have ideal finite DFE penalties more than 1 dB higher than PIE-D.

- Compute percentage of fibers/offsets with "implementation penalty" > x dB
  - Where x is either 1dB or 2dB
  - Percentage of the fibers/offsets with PIE-D in the 4.5-5.0dB range; not of the entire set
  - Where "implementation penalty" = finite-equalizer penalty - PIE-D

Summary

- Implementation penalty due to finite-length equalizers – and hence total dispersion penalty – can vary widely for IPRs with similar PIE-Ds

- Clearly, IPRs which are judged to be of similar difficulty (within +/- 0.25dB penalty) w/r/t PIE-D may not be very similar when presented to a shorter DFE

- The minimum complexity equalizer (DFE) required to handle the TP3 stressed sensitivity IPRs is insufficiently long to handle the diversity of IPR's that can and do occur within the selected PIE-D range for actual fiber populations.

- This is a consequence of the practical necessity of retaining only one IPR in the sieve for each of the four symmetry cases (pre-, post, quasi-symmetric, gaussian), but it can be fixed.

- **Proposal**: the finite equalizer penalties for the Monte Carlo set with connectors should be studied and published for both center and offset launch regions.
  - ➢ We are in the process of doing that, but encourage others to do so also
  - ➢ Preliminary results indicate that center launch IPRs are less well-behaved w/r/t finite equalizers than offset launches IPR's for Gen67YY and Cambridge 2.1.

- **Proposal**: if such studies confirms these findings on the 1998 set, we should add a criterion to the sieve which retains only IPRs that adequately challenge shorter DFE designs. Otherwise the test will pass receivers that will not work in practice.