Cl **00** *SC* *P* *L* # 280

NoName

Comment Type **E** *Comment Status* **X**

SuggestedRemedy

Proposed Response *Response Status* **O**

Cl **00** *SC* *P* **2** *L* **1** # 205

Thompson, Geoff Nortel

Comment Type **E** *Comment Status* **A** *ez*

Add note to balloters to indicate that this material will be added by the publications editor

SuggestedRemedy

Add note:
[Note to balloters to be removed before publication.]
[The abstract will be added during the preparation for publication process.]

Response *Response Status* **C**

ACCEPT.

Cl **00** *SC* *P* **2** *L* **2** # 206

Thompson, Geoff Nortel

Comment Type **E** *Comment Status* **A** *ez*

Add note to balloters to indicate that this material will be added by the publications editor

SuggestedRemedy

Add note:
[Note to balloters to be removed before publication.]
[The keywords will be added during the preparation for publication process.]

Response *Response Status* **C**

ACCEPT.
duplicate of 205

Cl **00** *SC* *P* **3** *L* **51** # 207

Thompson, Geoff Nortel

Comment Type **E** *Comment Status* **A** *midloc*

The text: "Midspan PSEs shall use Alternative B when used in 10BASE-T or 100BASE-TX systems. Midspan PSEs may support either Alternative A or B, or both when used in 1000BASE-T systems."

is incorrect. We will have no control of the "use" at the time a system is designed. This needs to be rephrased

SuggestedRemedy

Change to: "Midspan PSEs whose use is limited to 10BASE-T or 100BASE-TX systems shall use Alternative B. Midspan PSEs designed to support 1000BASE-T systems may support either Alternative A or B, or both."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolved by comment 158

Cl **00** *SC* **0** *P* *L* # 169

Law, David 3Com

Comment Type **TR** *Comment Status* **X**

The objectives state that we will support ISO/IEC 11801-1995 Class D cabling. This cabling is specifies with a maximum loop resistance of 40 Ohms [http://www.ieee802.org/3/at/public/nov06/3n807.pdf] although as stated in this liaison, a high proportion of the 1995 Class D channels are expected to meet the 25 Ohms. DC loop resistance.'.

I believe we have been using a loop resistance of 25 Ohms has been used in our calculations therefore we cannot absolutely claim that we can support ISO/IEC 11801-1995 Class D cabling.

SuggestedRemedy

Options are either:

[1] Change the objectives to state that we support ISO/IEC 11801-1995 Class D with the exception of the 40 Ohm loop resistance, update the draft as appropriate.

or:

[2] Ensure that we have used a 40 Ohm loop resistance in all calculations.

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 222

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A** *ez*

Please make the page numbers at the bottom on the page (printed) and the pdf numbers the same. This will eliminate confusion in commenting.

SuggestedRemedy

I would be happy to wokr with the Chief Editor to make this happen using Framemaker

Response *Response Status* **U**

ACCEPT.

Cl **00** *SC* **0** *P* *L* # 233

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

Im assuming that we will modify Clause 30 as well for management

SuggestedRemedy

Need specific suggested remedy or editorial instructions. Someone will need to take on the task to edit Clause 30.

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 248

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

All values in this table that are dependent on the underlying maximum current should be stated as such until we have a final resolution there.

SuggestedRemedy

Please state all parameters that are dependent on the DC current as a percentage of that.

Proposed Response *Response Status* **W**

what table, what page #, what line

Cl **00** *SC* **0** *P* *L* # 245

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

Where is the statement and what sections are covered by the resolution to comment 80 which stated

"Editor to incorporate Hugh's text as an addition to 33.6 and recirculate with next draft. Also, add note before section stating that text has not been accepted by 75% of TF."

SuggestedRemedy

Please clarify what text is new and NOT adopted by 75% at beginning of meeting and if we do not get around to adopting this text or a version of it for next draft, please include editor's note per resolution to comment 80 from D0.8

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 252

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

There is a subtle inconsistancy between the classification baseline we adopted and the draft. Specifically, the PD can only expect to see a maximum of 12.95W from the PSE while it waits for the L2 mechanism to come up. The issue in the draft is in several places describing this process it says that the PSE will treat a class 4 PD as it would under HW classification until the L2 engine is up. If I look at the power tables for HW classification they say 36W not 15.4W!

SuggestedRemedy

Please correct the following:
- In describing what a Type-2 PSE that is L2 capable does please specifically call out the limits to the power to be 15.4W consistant with the adopted baseline
- Please qualify the HW power tables with a footnote to explain when these apply for a Type 4

I will try to point out the descrepencies in other comments and specific locations but if I miss something please use this commeny

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 257

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

The deleted diagrams Figs Figure 33–9a and Figure 33–12b are useful illustrations of how link layer works even though they are not normative state diagrams.

SuggestedRemedy

Create an informative annex showing these diagrams as example of link layer behavious

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 262

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **R** *rej*

I am troubled that we are losing comments that we do not review between subsequent drafts

SuggestedRemedy

Either

(a) Hold off on creating a new draft until all comments have been reviewed in comittee

OR

(b) Input comments that were not reviewed into the comments database for the next draft. We can give them numbers that start at 2000 and address them as appropriate.

Response *Response Status* **U**

REJECT.

This is not a comment against the draft and result in no changes to the text. This is a comment against procedure and should be brought up with the chair.

CE original comment:
This an informal review not a formal review. In the interest of making progress, the chair and editors have decided to handle unresolved comments this way. It is the commentors responsibility to ensure the comment was addressed in the text and to reenter it at the next draft.

Once we move to the formal review, we will not distribute a new draft until all comments are resolved.

Cl **00** *SC* **0** *P* *L* # 265

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

I believe that w emay be adding new difinitions and references.

For example Type 1 and Type 2 PSE and PDs. Also, Is ANSI/TIA 1057 already referenced in Clause 1?

SuggestedRemedy

Please add additions and changes to Clause 1

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 269

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

We need to have a section that discusses PoE+ operation over cable of categories less than Class D

SuggestedRemedy

Insert a section that says something to the effect of

"Operation over cabling systems of Class D or lower is not guranteed"

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* **i** *L* **22** # 2

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Mispelling: 'Equipement'

SuggestedRemedy

Spell 'Equipment'

Response *Response Status* **C**

ACCEPT.

Cl **00** *SC* **0** *P* **v** *L* # 3
LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Header of symbols page, table of contents, list of tables, list of figures indicates D0.8.

SuggestedRemedy

Correct header on future draft revisions.

Response *Response Status* **C**

ACCEPT.

Cl **00** *SC* **3.5.4a** *P* **44** *L* **31** # 30
Patoka, Martin TI

Comment Type **E** *Comment Status* **A** *ez*

"the transient current drawn by the PD shall not exceed 15 mA/îs in either polarity."

THis presumes a static PSE voltage

SuggestedRemedy

change to:
"the transient current drawn
by the PD, with static PSE voltage, shall not exceed 15 mA/us in either polarity.

Response *Response Status* **C**

ACCEPT.

CE Note: comment type was blank, set to E by default.

Cl **33** *SC* *P* **74** *L* # 220
Diab, Wael Broadcom

Comment Type **E** *Comment Status* **A** *ez*

The line numbers appear on the wrong side of the page. This may be a problem with something else as it appears midstream in the clause

SuggestedRemedy

Please correct and watchout for on the next draft

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* *P* **81** *L* # 21
LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Header incorrect in all Annexes for draft version.

SuggestedRemedy

Update header for next draft.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **1** *P* **1** *L* **13** # 72
Dove, Daniel ProCurve Networking

Comment Type **E** *Comment Status* **R** *rej*

This line is too assertive as to the amount of power required

SuggestedRemedy

Insert "which may be used" between the words "power" and "to"

Response *Response Status* **C**

REJECT.

This is the existing introductory text.

Cl **33** *SC* **1** *P* **1** *L* **22** # 223
Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **D**

Please delete the words "An optional". The mechanism to do .3at allows for either L1 or L2 on the PSE, optional is not the correct indication.

SuggestedRemedy

Please delete the words "An optional".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 4

Cl **33** *SC* **1** *P* **1** *L* **22** # 4

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **D**

(1) Data Link Layer classification is only semi-optional. It is optional for PSEs, but not optional for PDs. Item (f) may imply more than it should.

(2) Also, (f) and (e) should be swapped for better logical flow of feature definitions.

SuggestedRemedy

(1) Delete 'optional' in (f).

(2) Swap (e) and (f) for better structure.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 223

Cl **33** *SC* **1** *P* **23** *L* **10** # 156

Law, David 3Com

Comment Type **TR** *Comment Status* **D**

I don't believe the draft states anywhere that for Type 2 operation ISO/IEC 11801:1995 Class D cabling or better is required. In addition we need to provide place holders in the draft for the cabling ambient operating temperature derating as well as the bundle size limitation. In respect to these I propose that we choose the third option in [http://www.ieee802.org/3/at/public/may06/law_1_0506.pdf], a fixed derating value.

SuggestedRemedy

Add a new subclause 33.3a 'Cabling system characteristics for Type 2 PSE and PD operation'

Type 2 PSE and PD requires Class D cabling as specified in ISO/IEC 11801:1995. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5e components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995. Additionally:

a) Type 2 PSE and PD operation requires the maximum ambient operating temperature of the cabling to be derated by TBD C.
b) The maximum number of cables in a bundle supporting Type 2 PSE and PD operation is limited to TBD.

Type 2 PSE and PD operation on cabling worse than Class D ISO/IEC 11801:1995 may result in intermittent operation at maximum requested power and is beyond the scope of this standard.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 169

Cl **33** *SC* **1.1** *P* **1** *L* **36** # 224

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

These objectives do not include the ones from .3at.

SuggestedRemedy

Please add the 802.3at objectives

Proposed Response *Response Status* **W**

Elaborate. What text specifically?

Cl **33** *SC* **1.1** *P* **1** *L* **46** # 73

Dove, Daniel ProCurve Networking

Comment Type **T** *Comment Status* **R** *rej*

I believe the term "without modification" may no longer be accurate. It depends on whether 8ma/350uH is left as-is.

SuggestedRemedy

Depending on the status of the 8ma/350uH determination, strike this and the word "and" behind it.

Response *Response Status* **C**

REJECT.

Nothing has changed yet. This comment will be appropriate if 8mA/350uH changes.

Cl **33** *SC* **1.1** *P* **15** *L* **45** # 157

Law, David 3Com

Comment Type **T** *Comment Status* **X**

In the case of Type 2 PSE and PD operation it is no longer correct to state that 'adds no significant requirements to the cabling.' since it will [1] require the use of ISO/IEC 11801:2002 Class D or better base on the objectives, [2] require a limit on the ambient operating temperature of the cabling below that of the cable specification and [3] a limit on the maximum bundle size based on the current liaison information.

SuggestedRemedy

Delete the text 'adds no significant requirements to the cabling.'.

Proposed Response *Response Status* **W**

see 213

Cl **33** *SC* **1.1** *P* **15** *L* **46** # 213

Thompson, Geoff — Nortel

Comment Type **TR** *Comment Status* **X**

The text:
"Compatibility—Clause 33 utilizes the existing MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification and adds no significant requirements to the cabling."
...is not quite true. To get the full power delivery capabilities of 802.3at the user MUST have a 5e or better cabling system. The difference between that system (25 ohm) and a legacy Cat 5 system can result in as much as a 7% difference in the worst case power available at the PD.

SuggestedRemedy

I do not have remedial text prepared at this point but the draft must make explicit the differences in performance expected from 25 vs. 40 ohm cabling systems.
-OR-
Must do the design entirely based on the worst case cabling (40 ohm) and take the 7% hit on delivered power.

Proposed Response *Response Status* **W**

see 157

Cl **33** *SC* **2** *P* **17** *L* **33** # 159

Law, David — 3Com

Comment Type **TR** *Comment Status* **X**

It is not correct to state that all PSEs have to classify the PD. A Type 1 PD can still, optionally, choose not to do this.

SuggestedRemedy

Change '.. classify the PD ..' to read '.. optionally classify the PD ..'.

Proposed Response *Response Status* **W**

see 251

Cl **33** *SC* **2** *P* **3** *L* **33** # 251

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

Deleting the word optional makes the functionality requirement of classification ambigious for Type 1 vs. Type 2

SuggestedRemedy

Append the following sentence to the end of the paragraph: ""The classification function may be optional depending on the Type of PSE""

Proposed Response *Response Status* **W**

see 159, 154

Cl **33** *SC* **2.1** *P* **17** *L* **51** # 158

Law, David — 3Com

Comment Type **TR** *Comment Status* **A** *midloc*

The text states that 'Midspan PSEs shall use Alternative B when used in 10BASE-T or 100BASE-TX systems'. It then states that 'Midspan PSEs may support either Alternative A or B, or both when used in 1000BASE-T systems'. There is no definition of what a 10BASE-T, 100BASE-T or 1000BASE-T 'system' is, so in the following I will assume that simply it means that the link is operating with that type of PHY at each end.

Many ports these days are 10/100/1000BASE-T capable. Based on this, take the case of a 10/100/1000BASE-T non-PSE switch port that is connected to a Midspan. The Midspan connected to this port will have to be a 1000BASE-T capable Midspan or the link will never be able to operate at 1000BASE-T. The port however may not actually be operating at 1000BASE-T so this would seem to force the Midspan to be Alternative B to meet the mandatory requirement for 10BASE-T and 100BASE-T operation. In fact unless you can guarantee that the link the 1000BASE-T Midspan is connected in will only ever operate at 1000BASE-T, which I do not believe the Midspan has any way to force, the Midspan will have to be Alternative B.

The option of being able to build an Alternative A Midspan therefore seem unusable.

SuggestedRemedy

Either (i) mandate that all Midspans have to be Alternative B or (ii) allow 10BASE-T and 100BASE-T Midspans to be Alternative A as well as Alternative B. I suggest the second option on the basis that if it has been proved that 1000BASE-T Alternative A Midspans can be built while maintaining the link segment requirements they should be permitted for 10BASE-T and 100BASE-T operation as well. If this has not been proved then my first option has to be used.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change text "Endpoint PSEs may support either Alternative A or B, or both. Midspan PSEs shall use Alternative B when used in 10BASE-T or 100BASE-TX systems. Midspan PSEs may support either Alternative A or B, or both..."

to:
PSEs may support either Alternative A or B, or both.

see 207, 154

vote:

Y:20, N:0

Cl **33** SC **2.1** P **19** L **38** # 154

Law, David 3Com

Comment Type **TR** *Comment Status* **A** *midloc*

We seem to now have defined two 'types' of Midspan PSEs which are not interchangeable, a 10/100BASE-T Midspan which does not provide continuity on the spare pairs (see Figure 33-4), and a 1000BASE-T Midspan that does (see Figure 33-4a). Combine that with Types of PSE defined in 33.2.2a and we have a total of four types of Midspan:

10/100BASE-T Type 1 Midspan PSE
1000BASE-T Type 1 Midspan PSE
10/100BASE-T Type 2 Midspan PSE
1000BASE-T Type 2 Midspan PSE

Now I note that there is a statement in subclause 33.4.8 that 'A Midspan inserted in a channel shall provide continuity for the signal pairs'. I'm not sure if that is a contradiction to Figure 33-4 10/100BASE-T Midspan PSE Alternative B which shows no continuity on two of the four pairs.

SuggestedRemedy

Add a new subclause that clearly defines that where each type of Midspan can and cannot be used. Suggest a new subclause 33.2.1a as follows:

33.2.1a Midspan PSE types

There are two types of Midspan PSE defined.

10/100BASE-T Midspan PSE
A Midspan that will result in a link that can only support 10BASE-T and 100BASE-T operation (see Figure 33-4). Note that this limitation is due to the presence of the Midspan regardless if it is supplying power or not.

1000BASE-T Midspan PSE
A Midspan that will result in a link can support 10BASE-T, 100BASE-T and 1000BASE-T operation (see Figure 33-4a)

Response *Response Status* **C**

ACCEPT.

see 158, 207

Cl **33** SC **2.1** P **21** L **4** # 155

Law, David 3Com

Comment Type **TR** *Comment Status* **A** *fig33-4*

I can see no difference between the Alternative A and Alternative B shown in Figure 33-4b. Both alternatives show (incorrectly) all four pairs connected to the PSE.

SuggestedRemedy

Correct the figure so that only two pairs on each alternative are connected to the PSE. Following the convention we seem to be using in Figure 33-4, the outer two pairs are used for Alternative A and the inter two pairs are used for Alternative B. The Figure will however require some additional annotation to indicated which is which pair, since the 1000BASE-T PHY uses all four pairs, and without this annotation the figure will effectively be content free.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Resolved by 250

Cl **33** SC **2.1** P **3** L **52** # 279

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *midloc*

There is nothing to prevent a 100BASE-TX device from being plugged into a midspan that implements Alt. A. Implementations of an Alt. A midspan may interfere with a 100BASE-TX PHY implementation that rely on the link partner's output inductance as required by the specification.

SuggestedRemedy

Either disallow implementations of Alt A OR Insert the following statement: "Midspans implementing Alternative A shall not interfere with the data performance of a 100BAE-TX link, specifically as it relates to the output inductance requirement. This shall apply regardless of power being applied (i.e. when power is privisoned and when it is not).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add this text:
Note - Midspans implementing Alternative A are not allowed to interfere with the data performance of a 100BASE-TX link. This applies regardless of power being applied. Refer to Clause 25 for 100BASE-TX compatability requirements.

Cl **33** *SC* **2.1** *P* **3** *L* **53** # 243

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **R** *midloc*

Please delete the word both. We have not voted on doing 4-pair power yet. Further, Please show technical feasability that midspans can support both A and B working together on the same link.

SuggestedRemedy

Please delete the word both.

Response *Response Status* **U**

REJECT.

This is text copied from AF. There is not shall, there is no requirement. Having 'both' doesn't imply simultaneous operation.

see 207, 158

Y: 12, N: 4

Cl **33** *SC* **2.1** *P* **6** *L* **6** # 90

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **A** *ez*

Draft0.9
Figure 33-4a:
1. The data transformer in Midspan is one way to combine power with data.
Other implementations are possible.

SuggestedRemedy

1. Replace the data transformer in the Midspan with a black box which indicates implementation independent data and power interface.
See attached drawing.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Note added in D0.9 draft page 4, line 8 showing drawings are informative.

Cl **33** *SC* **2.1** *P* **7** *L* **1** # 70

Patoka, Martin — TI

Comment Type **TR** *Comment Status* **A** *fig33-4*

Figures 33-4b
Figures are drawn showing the PSE connecting power to all 4 pairs, even though figures are labelled alternative A andd B.

SuggestedRemedy

Remove connections within PSE block to show only one pair powered.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolved by 250

Cl **33** *SC* **2.1** *P* **7** *L* **50** # 214

Vetteth, Anoop — Cisco

Comment Type **T** *Comment Status* **A** *fig33-4*

Figure 33-4b
There is no differece between the figures for Alternative A and B implementations.

SuggestedRemedy

Refer to clause 40.8.1 "MDI Connectors" for 1000 Base-T. Connect only the center taps for contacts 1-2 and 3-6 to the PSE for Alternate A implementation. Connect only the centertaps for contacts 4-5 and 7-8 for Alternate B implementation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolved by 250

Cl **33** *SC* **2.10.1.2** *P* **32** *L* **10** # 33

Patoka, Martin — TI

Comment Type **E** *Comment Status* **D**

Figure 33-11. The resistor value is 2(Omega)EG.

SuggestedRemedy

value should be 1.98MEG

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See 17

Cl **33** *SC* **2.10.1.2** *P* **32** *L* **11** # 17

LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **D**

Resistor value is not printed correctly. The spec. in Table 33-6 says the impedance should be greater than 1980k, not a std. resistor value and tolerance.

SuggestedRemedy

Resistor value should be " >1980 kohms"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See 33, should the number not be there and just a reference to the table?

Cl **33** *SC* **2.2** *P* **8** *L* **50** # 116

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

The standard should not preclude implementations that are using both alternative A and B due to the following reasons:
a) It is out of scope of the standard to limit implementations.
b) There are no interoperability issues if PD gets power from two 2 pairs power source. It is the load responsibility (PD) to meet the 2P specification for each 2P. Implementation methods are out of scope of the standard.
c) It is economically feasible as shown in numerous presentations
d) It is technically feasible as shown by the same presentations.
e) There are products in the market that already is using the 2 x 2P implementation e.g. High power Midspan that is using 2 x 2P and applications that are using 2P power coming from the Switch and additional power delivered from Midspan.
f) There is huge market for higher power then 30W over 2P.
g) There is no additional cost issue. The $/watt cost is even lower then in 2P system as shown in previous meeting presentations.
h) For outdoor applications, temperature rise issues of the cables when using 60degC cabling system grade can be solved if the same power is delivered over 2 x 2P which is an easy solution for outdoor applications.
i) Users will do it any way to utilize the full capability of the existing infrastructure.
J) In previous meeting switch and PHY vendors wanted the ability to use the same cable which consists of 4 pairs to support two PDs that each one of them is connected to a 2P system. The current text precludes using this feature.

SuggestedRemedy

Change from:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.2** *P* **8** *L* **50** # 273

NoName

Comment Type **E** *Comment Status* **X**

CommenterName: Ostrovski Shlomo
CommenterEmail: shlomo@advice.ci.il
CommenterPhone: +972-39000-900
CommenterCo: Advice LTD

There is no technical, economical or interoperability which prevents powering all 4 pairs.

If a PD gets power from multiple 2P system which is independent in their functionality i.e. each 2P has its own detection, classification, and power on functionality

and if the responsibility of the PD is to meet the 2P specifications in any of its inputs due to the fact that any 2P port should meet the specification of this standard

then if many 2P outputs connected to the same PD, then it is OK.

In addition this is the objective of this standard to seek for the maximum practical power. The minimum was 30W.

There are applications that require more then 30W.

Actually the question of market size for this applications is not relevant due to the fact that there is no additional effort required in the standard work to allow it if each 2P system requirements is kept by the PD.

There are 4pairs systems in the market already that utilize this simple concept of delivering independent two x 2P power sources to the PD.

SuggestedRemedy

Allow to implement both alternatives simultaneously. Delete the text that precludes this option.

In page 33 line 42 revise the text to allow feeding PD with any number of independent 2P systems as long as each 2P specification is compliant to this standard.

Proposed Response *Response Status* **W**

see 116, identical comment

Cl **33** *SC* **2.2** *P* **8** *L* **51** # 275

NoName

Comment Type **E** *Comment Status* **X**

CommenterName: Aasher Biton
CommenterEmail: asherb@advice.co.il
CommenterPhone: +972-39000-900
CommenterCo: Advice LTD

According to the current text, the standard precludes to use the following applications:

1. Two PSE ports that are utilizing the same cable to operate two separate PDs.

2. Two different PSE ports, an End point PSE port and a Midspan port each may delivering max. 2P power to a single PD which contains two types of load e.g. security cameras with static and dynamic loads.

3. Smart home applications that are using actuators with high peak current on one power channel and control circuitry on the 2nd channel.

4. a PD that requires more then 2P system allowed to provide.

5. Patch panel Midspans that would like to utilize the maximum capabilities of the infrastructure as allowed by the cabling manufactures and TIA reports.

There is no relevant reason to preclude these specific applications and more generally, for the IEEE standard it is out of scope to preclude implementations as long as the implementation is meeting the 2P requirements for each 2P system.

SuggestedRemedy

Replace "shall not operate" with "may operate" at line 51.

Scan PD specification as well and delete text that prohibits a PD system to accept and work with multiple 2P inputs.

(The note in page 33 line 41 etc.)

Proposed Response *Response Status* **W**

see 116, identical comment

Cl **33** *SC* **2.2** *P* **8** *L* **51** # 271

NoName

Comment Type **T** *Comment Status* **X**

CommenterName: Prof. Dr. Christian Kargel
CommenterEmail: christian.kargel@unibw.de
CommenterPhone: +49 89 6004-3741
CommenterCo: Institute for Measurement and Automation, Bundeswehr University Munich

One large market of PoE is the smart home technology which we are currently investigating in our own smart home and we have found that PoE technology is highly suitable for powering sensors, actuators and other smart home components in addition the communicate with them.

In order to reduce the amount of cabling installation to these components we have found that using all 4 pairs for this purpose provides an optimized way in terms of the power required to operate a group of sensors and the number of cables needed to connect these sensors.

The current text in 802.3 precludes the simultaneous use of Alternative A and B. We are not aware of any technical, economical or reasons.

As far as we know there are already systems available that deliver power over all 4 pairs while at the end of each 2P is a "PD" connected or even a single PD gets two 2P systems for higher power applications.

Those systems seem to be working well due to the fact that each 2P is independent in its functionality and orthogonal in behavior to the other 2P output. It is similar to the concept of having a multi-port system with port A working independently from port B and port_i in general.

SuggestedRemedy

Change the text in line 51 to allow the PSE to operate both Alternative A and Alternative B on the same link segment simultaneously.

Add a text in the PD specification (33.3.1) that requires the PD to meet the specifications of 2P system for any number of 2P system connected to it.

Proposed Response *Response Status* **W**

see 116, identical comment

Cl **33** *SC* **2.2** *P* **8** *L* **51** # 276

NoName

Comment Type **E** *Comment Status* **X**

CommenterName: Levy Avinoam
CommenterEmail avinoam@solarpower.co.il
CommenterPhone: +972-9-8654904
CommenterCo: SolarPower LTD

In 802.3af the standard precluded feeding both alternatives A and B simultaneously due to the need to limit the scope of the project to done with it on time.

Since then it was shown in many products in the market that there is a need and there is no technical limitation from implementation point of view and/or interoperability issues with existing compliant 802.3af devices.

One of the reasons of the success of such implementations e.g. 4 pairs implementations was due to the fact that the PSE maintain the same functionality for each 2P output and the PD accept the power as two independent power sources so everybody was kept happy.

Today we know that the cable is capable of powering all pairs.

In addition there are more and more applications that requires more power

And also having support for more power doesn't mean that we have to pay more for power or having bigger power supply etc. due to smart use of power management as shown in early stages of this project and will be even smarter and more appealing with the layer 2 power management capabilities.

The cost for the standard development to allow Alternative A and B simultaneously on the same PI segment is zero due to the fact that we are defining 2P system that can be used N times for multiple PDs or for the same PD as long as the application (PD) meets the 2P requirements of each 2pairs.

SuggestedRemedy

Adopt the text changes at lines 50-51 as proposed in draft D0.8.

Delete the note in page 33 regarding PD having power from both alternatives.

Proposed Response *Response Status* **W**

see 116, identical comment

Cl **33** *SC* **2.2** *P* **8** *L* **51** # 272

NoName

Comment Type **TR** *Comment Status* **X**

CommenterName: Daniel Feldman
CommenterEmail: dfeldman@microsemi.com
CommenterPhone: 14084062639
CommenterCo: Microsemi Corp.

The standard should not preclude implementations that are using both alternative A and B. Rationale:

a) It is out of scope of the standard to limit implementations.

b) There are no interoperability issues if PD gets power from two 2-pairs power source. It is the load responsibility (PD) to meet the 2-Pairs specification for each 2-Pairs. Implementation methods are out of scope of the standard.

c) It is economically feasible as shown in numerous presentations.

d) It is technically feasible as shown by the same presentations.

e) There are products in the market that already is using the 2 x 2-pairs implementation e.g. High power Midspan that is using 2 x 2-pairs and applications that are using 2-pairs power coming from the PoE Switch and additional power delivered from a Midspan.

f) There is huge market for higher power then 30W over 2-pairs, including Fiber-to-the-Home and WiMAX CPE's

g) There is no additional cost issue. The $/watt cost is even lower then in 2-pairs systems, as shown in previous meeting presentations.

h) For outdoor applications, temperature rise issues of the cables when using 60degC cabling system grade can be solved if the same power is delivered over 2 x 2-pairs, which is simple solution.

i) Users will do it any way to utilize the full capability of the existing infrastructure.

J) In previous meeting switch and PHY vendors wanted the ability to use the same cable which consists of 4 pairs to support two PDs that each one of them is connected to a 2-pairs system. The current text precludes using this feature.

SuggestedRemedy

Change from:

"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:

"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **W**

see 116, identical comment

Cl **33** *SC* **2.2.a** *P* **9** *L* **25** # 94

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **R** *rej*

According to a motion made at July 2007 meeting, A Type 2 PSE when it powers Type 1 PD, may use Type 2 PSE current limit specification.

The text says that Type 2 PSE fully supports Type 1 and type 2 PDs which may be not accurate since to fully support type 1 PD means also to support the same level of protection required by Type 1 PSE.

SuggestedRemedy

Change from:
"Table 33–5 specifies the electrical characteristics of Type 1 and Type 2 PSEs. When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the electrical requirements of a Type 1 PSE."

To:
"Table 33–5 specifies the electrical characteristics of Type 1 and Type 2 PSEs. When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the electrical requirements of a Type 1 PSE. Short circuit and overload protection functions parameters of PSE type 2 may be used as well in this case."

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

This comment is on deleted text.

Cl **33** *SC* **2.2a** *P* **9** *L* **25** # 5

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

The NOTE does not appear to be set in the correct paragraph format.

SuggestedRemedy

Make sure the paragraph is set properly.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.2a** *P* **9** *L* **3** # 160

Law, David 3Com

Comment Type **TR** *Comment Status* **D**

While I guess that the text 'fully supports Type 1 PDs' is used in the case of the Type 1 PSE definition to indicate that a Type 1 PSE may partially support a Type 2 PD I think this is too subtle. In addition the text 'NOTE—A Type 2 PSE is a superset of a Type 1 PSE.' doesn't seem to add any information, that can be seen from the definition to Type 1 and Type 2 PSEs above.

SuggestedRemedy

Suggest that the word 'fully' be deleted from both the Type 1 and Type 2 PSE definitions and that the note is changed to read 'Note - A Type 1 PSE may support limited operation of a Type 2 PD.'.

Proposed Response *Response Status* **O**

See 56

Cl **33** *SC* **2.2a** *P* **9** *L* **8** # 56

Patoka, Martin TI

Comment Type **T** *Comment Status* **D**

The definition of type 1 and 2 seem circular, and may cause confusion in general readers.

SuggestedRemedy

Add further clarification, perhaps as a note, similar to: Type 1 PSE and PD were defined in IEEE 802.3-2005. A type 1 PSE provides detection, optional 1 event hardware classification, and provides a maximum of 15.4W. A type 1 PD provides detection, hardware classification, and consumes less than its declared classification power to 12.95W maximum. A type 2 PSE performs detection, and may provide up to 36W. It must provide either a 2 event hardware classification, or a data layer classification. A type 2 PD provides detection, hardware classification, and consumes less than its declared classification power to 29.5W maximum. A type 2 PD must support 1 event hardware classification, 2 event hardeare classification, and data layer classification.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Text needs cleaned up. Also, see 160 and resolve together.

Cl **33** *SC* **2.3.1** *P* **10** *L* **6** # 179

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X**

The phrase "This ensures that a PSE performing detection using Alternative A will complete a successful detection cycle priot to a PSE using ALternative B that might also be present..." is inconsistent with the previous sentence that states that and Alternative A PSE "should complete a second detection attempt within 2 seconds...". Nothing is "ensured" here because the requirement on the Alternative A PSE is worded with "should", not "shall".

SuggestedRemedy

Either: Change "should" to "shall" - this would be disruptive to exising PSE's however.

Or: Change the phrase to-

"For Alternative A PSE's that complete a second detection cycle within 2 seconds, this ensures...."

Proposed Response *Response Status* **W**

see 6

Cl **33** *SC* **2.3.1** *P* **10** *L* **6** # 6

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **D**

Final sentence in paragraph is too long and reads choppily.

SuggestedRemedy

Replace sentence with:

This ensures that a PSE performing detection using Alternative A will complete a successful detection cycle prior to a PSE using Alternative B that might also be present on the same link section and causing the invalid signature.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 179

Cl **33** *SC* **2.3.4** *P* **10** *L* **29** # 106

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft0.9
During "Short Circuit" Condition i.e. when PSE and PD are no longer at their operating voltage range, there is no technical need to keep PSE port on for TLIM.
It creates many problems such:
1. Prevents meeting item 21 in table 33-5, Ted (Time delay between consecutive start ups.
2. Excessive heat.
See more details in MR #1167.

SuggestedRemedy

To allow the PSE to turn the port to OFF mode when Vport <> Normal operating range at any t<TLIM_MIN.
Remedy steps:
1) Add new variable option_vport_lim to 33.2.3.4. It will be an optional variable.

option_vport_lim
This variable is indicating If PSE port voltage is out of operating range during normal operating mode.
Values:
False: Vport is within the Vport normal operating range as defined by table 33-5.
True: Vport is not within the Vport normal operating range as defined by table 33-5.
3) Add the following text to 33.2.8.8 after item e. Items d and e are resereved for maintanance request 1162).
"f) During short circuit condition, for PI voltages below or above Vport normal operation range as specifiied in table 33-5 the PSE may turn to IDLE state at any time t < TLIM_MIN.
"

4) Change state diagram (figure 33-6) per the attached drawing.

Using this optional variable in the state diagram will fix the problem by changing the inputs to ERROR_DELAY_SHORT state
from: tlim_timer_done
to: Tlim_timer_done + !tlim_timer_done*option_vport_lim*power_applied)

Effect on legacy equipment: None since the variable is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.3.6** *P* **26** *L* **47** # 165

Law, David 3Com

Comment Type **T** *Comment Status* **D**

See previous comment on default behavior, a Type 1 should default to Class 0, a Type 2 to Class 4.

SuggestedRemedy

Change the text 'Class 0 is returned if an invalid classification signature is detected.' to read ' If an invalid classification signature is detected Class 0 is returned by a Type 1 PSE, Class 4 is returned by a Type 2 PSE.'

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.3.7** *P* **13** *L* **11** # 101

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **A** *fig33-6*

See 33.2.3.7 State Diagram figure 33-6.
In test mode among other conditions that leads to the "Test Error" state, there is also the "power_not_available" condition that may end with "Test Error" state and shutting off the port again. It is similar to the conditions leading to the state "Power Denied" in normal operation mode.
The current state flow doesn't allow to shut off the port in case of "power_not_available".

SuggestedRemedy

Change the input conditions set to the TEST_ERROR state from:
(tlim_timer_done+tovld_timer_done)*(mr_pse_enable=force_power)

to :
(power_not_available+tlim_timer_done+tovld_timer_done)*(mr_pse_enable= force_power)

No impact on existing equipment. It is just "OR" and fix the error in the state diagram.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.3.7** *P* **13** *L* **22** # 75

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **A** *fig33-6*

the variable pd_Requested_power is not defined in the variable definitions.

SuggestedRemedy

Define it and search for any other variables that are undefined and fix them too.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Editor to define this variable. Comment review should find any other undefined variables.

Cl **33** *SC* **2.3.7** *P* **13** *L* **4** # 125

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *fig33-6*

It is not clear from the PSE state diagram that detection phase always starts form IDLE state in which the PSE is at OFF mode.
OFF mode is the PSE mode were the average voltage at the PI is <=2.8V.

Any other possibility may end with invalid detection even if the PD has valid signature elements.
e.g.: The PSE did detection and for some reason system decided to not power the port and to issue additional detection phase.
In this case the port voltage may be >2.8V which may cause invalid detection results this loop can go forever and the port may never be ON.

SuggestedRemedy

Add text that requires the following:

Between two consecutive detection attempts, the PI shall gone through OFF mode as defined by table 33-5 item 13b.

Equivalent wording is possible.

Add text that requires the following:

Between two consecutive detection attempts, the PI shall gone through OFF mode as defined by table 33-5 item 13b.

Equivalent wording is possible.

The task force members are encourage to check if the proposed fix may reduce implementation flexibility.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The text does not match the state diagram.

Change 33.2.8.10:

from:
"The PSE enters the IDLE state when VPort drops 1 V below the steady-state value after…"

to:
"Toff starts when VPort drops 1 V below the steady-state value after…"

add new sentence following above change:
"Toff ends when Vport <= Voff."

Cl **33** *SC* **2.3.7** *P* **13** *L* **54** # 129

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **A** *fig33-6*

Figure 33-6

Need to call existing PSE state diagram, "Type 1 PSE state diagram"

and add a Type 2, Physical Layer PSE state diagram

and add a Type 2, LLDP PSE state diagram
.

SuggestedRemedy

Figure 33-6 title:

IS:
PSE state diagram

SHOULD BE:
Type 1 PSE state diagram

Response *Response Status* **C**

ACCEPT.

See 130

Cl **33** *SC* **2.3.7** *P* **14** *L* **27** # 130

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **A** *fig33-6*

Figure 33-6

Add a Type 2, Physical Layer PSE state diagram

Add a Type 2, LLDP PSE state diagram

SuggestedRemedy

Add 2 state diagrams per attachments.

Response *Response Status* **C**

ACCEPT.

See 129, drawings were attached

Cl **33** *SC* **2.5** *P* **16** *L* **25** # 57

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

Table 33-2. Calculation of the signature is not provided (as in 33.3.3), therefore a tolerance is not applicable. Current tolerance is bounded to 0uA, however this is not true of the PD (no minimum, could be -infinite). Since PDs theoretically have a NEGATIVE current intercept, bounding PSE to 0 causes a consistensy problem. Note that Fogure 33C-20 indicates a negative current offset. Current offsetts are cancelled out by the computation methed anyway.

SuggestedRemedy

Recomment setting the PSE tolerance to +/-50uA. Recommend moving figure 33C-20 to this section of normative text, including method of computation, and annotating the current offset on the figure.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.5.1** *P* **16** *L* **31** # 202

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

The existing section on PD detection requires specific design requirements that are not necessary to ensure interoperability. Other detection methods have been disclosed:
http://www.ieee802.org/3/poep_study/public/sep05/naegeli_1_0905.pdf
The IEEE specification should ensure requirements for interoperability are in place.

This comment may also affect text in section 33.3.3.

SuggestedRemedy

Reference the PD model shown in figure 33-10, and require that the PSE detect values of Rpd_d for all permissible values of Cpd_d as specified in table 33-2.

Remove the text requiring two values but continue to provide guidance for designs that use the two probe method.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7** *P* **17** *L* # 102

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X** *33.2.7*

It is not clear to the user if a delay between detection and classification is required.
It is logically understood that if the standard is not precluding to do something then it is allowed to do it however due to the fact that in PSE type 2 classification there is importance to the fact if PSE is at reset range or not, I find it usefull to explicitly determine what is allowed to do.

SuggestedRemedy

Add a note that says:

Time delay between the end of detection phase to the start of classification phase is not required by the standard. Spcifically, classification may start from any level of the detection voltage.

The task force members are encourage to check if the proposed fix cause problems to existing equipment or to Type 2 systems.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7** *P* **17** *L* # 226

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

33.2.7 can be made into the intro section for PSE classification per my next comment. This comment addresses the contents of the introductory section:

There needs to be an introduction that details what a Type-2 PSE can do. Specifically, that it can do either a Dat-Link or Physical Layer classification. It is required to do one or the other. The section can then point to a section (a) that details the Physical Layer Classification and a section (b) that details Data-Link Layer Classification.

Currently, there is no mention of the Link Layer Classification in the openning section. Further it is confusing to get to the Link Layer option

SuggestedRemedy

One way to do this is to retain the paragraph starting at line 43 as teh opening paragraphe. Then:

Please append the following sentence after the current sentence that reads "A Type 2 PSE may* perform hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

"A Type 2 PSE may perform Data Link Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2b."

Please insert the following sentence as the last sentence in the section: "Type 2 PSEs Shall perform either Physical Layer or Data Link Layer Classification"

* Please note that I have asked for a seperate change to the retained paragrpah to include the word "may" in a seperate comment.

Proposed Response *Response Status* **W**

see 227, 49

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 49

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X** *33.2.7*

LL classification was moved to the management section. In order to make the requirements clear, we need to pull together the endspan and midspan requirements. I believe that we should use this paragraph as an overview. Paragraph 33.3.7.2a text (p18 line 34 & ff) should be moved to 2.7. The equivalent of stnaford_1_0707 page 16 should be included as a guide.

SuggestedRemedy

A Type 1 PSE may optionally classify a PD. If a Type 1 PSE successfully completes detection of a PD, and the PSE does not classify the PD using hardware Physical Layer classification, then the PSE shall assign the PD to Class 0.

Type 2 PSEs shall classify to determine the PD type. Endspan PSEs shall perform either Type 2 physical layer classification, or Type 1 Physical Layer classification and Type 2 Link Layer Classification per 33.6. Midspan TYpe 2 PSEs shall perform Type 2 Physical layer classification per 33.2.7.2a.

If a type 2 PSE classifies a type 1 PD, the PSE need only perform the first type 2 hardware classification event. Type 2 Physical Layer and Type 2 Link Layer classification permit mutual classification.

A successful classification of a PD requires:
a) Successful PD detection, and subsequently,
b) Successful Type 1 or Type 2 Class 0–4 hardware Physical Layer classification.
A PSE may remove power to a PD that exceeds the maximum power limit for its advertised class.
A Type 1 PSE performs optional hardware Physical Layer classification of a PD by applying voltage and
measuring current, as specified in 33.2.7.2. A Type 2 PSE performs hardware Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a.
The PSE hardware Physical Layer classification circuit should have adequate stability to prevent oscillation
when connected to a PD.

Proposed Response *Response Status* **W**

see 226,227

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 227

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

This section is very confusing. We dive into Physical Layer classification and then do Data-Link Layer Classification. I would suggest that we make 33.2.7 a general introduction to classification. We then take 33.2.7 and 33.2.7a and make them subclauses of this new geenral section.

For the content of the general section on classification, I will submit a seperate comment (my previous comment in the .csv file).

SuggestedRemedy

I would suggest that we make 33.2.7 a general introduction to classification. We then take 33.2.7 and 33.2.7a and make them subclauses of this new geenral section.

Proposed Response *Response Status* **W**

see 226, 49

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 161

Law, David 3Com

Comment Type **TR** *Comment Status* **X** *33.2.7*

[a] It is difficult to follow the various different types of classification we now have, and there is no overall introduction to guide the reader to what options there are and what features each option provides. There should be a broad introduction to all types of classification, and introduction to each specific type of classification then finally the details of the operation.

[b] Subclause 33.2.7 PSE Hardware classification of PDs' currently states that 'A PSE may remove power to a PD that violates the maximum power required for its advertised class.' which implies this only applies to hardware classification and that if a PD violates the maximum power it advertised through Link Layer classification it isn't permitted to do this. I don't believe this is correct and it is just as valid to do this for Link Layer classification. This text should therefore be moved so that it applies to all classification methods. See also other comment on this text.

SuggestedRemedy

Suggest that:

[1] Subclause 33.2.7 become an introductory clause that reads:

33.2.7 PSE classification of PDs

The ability of a PSE to classify a PD allows features such as load management to be implemented. There are two forms of classification, hardware classification and optional link layer classification. Hardware classification allows a PSE to classify a PD into one of a limited number of granular classes, this classification occurs once after a PSE successfully completes detection of a PD. Link layer classification allows a more granular classification that the initial hardware classification, this classification occurs continuously and provides the ability for the PD classification to change.

A PSE may remove power from a PD that violates the maximum power it has advertised it requires. This maximum power is initially derived from the advertised class during hardware classification and then, if implemented, subsequently updated by link layer classification.

[2] A new subclause 33.2.7.1a be inserted that reads:

33.2.7.1 PSE hardware classification of PDs

There are two types of hardware classification dependant of the PSE type, Type 1 hardware classification and Type 2 hardware classification.

A Type 1 PSE may optionally perform hardware classification. If a Type 1 PSE does perform hardware classification it shall use Type 1 hardware classification (see 33.2.7.2). If a Type 1 PSE does not classify the PD using hardware classification, then the Type 1 PSE shall assign the PD to Class 0.

A Type 2 PSE shall perform hardware classification and shall use Type 2 hardware classification (see 33.2.7.2a). This is to ensure that a Type 2 PSE implementing only hardware classification can indicate its presence and identify the Type 2 PD's power requirements.

A successful hardware classification of a PD requires:

a) Successful PD detection, and subsequently,
b) Successful Type 1 or Type 2 Class 0-4 hardware classification.

The PSE hardware classification circuit should have adequate stability to prevent oscillation when connected to a PD.

Proposed Response *Response Status* **W**

Cl **33** *SC* **2.7** *P* **17** *L* **28** # 164

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *33.2.7*

On the long standing basis that we should be conservative on what we send but liberal on what we receive I think we should state what should be done if classification fails for some reason for both a Type 1 PSE and a Type 2 PSE.

In IEEE Std 802.3-2005 we state 'If a PSE successfully completes detection of a PD, and the PSE does not classify the PD in Class 1, 2, 3, or 4, then the PSE shall assign the PD to Class 0.' Now this text does not state the reason why the PSE does not classify the PD so this seems to apply to [a] a PSE that doesn't perform classification and [b] a PSE that does perform classification but when the classification cycle occurs the values return do not match a value. I believe this is confirmed by the State Diagram (figure 33-6) which states in the do_classification function that definition (subclause 33.2.3.6) that 'Class 0 is returned if an invalid classification signature is detected'.

One approach would seem to be to apply the same approach to IEEE P802.3at, if hardware classification fails regardless of Type treat the PD as a class 0. There is however one edge case if a Type 2 PD has a fault such that a PSE cannot detect it as a Type 2 yet it is still capable of detecting a Type 2 PSE. In this case the PSE would treat it as Class 0 and possibly limit it to 15.4W while the PD having detected a Type 2 PSE will operate as if 36W is available. Based on this I guess the default has to be Class 0 for Type 1 and Class 4 for a Type 2.

SuggestedRemedy

Change the text to read 'If a PSE successfully completes detection of a PD, but the PSE fails to classify the PD as a Class 1, 2, 3, or 4 using hardware classification, then the a Type 1 PSE shall assign the PD to Class 0 a Type 2 PSE shall assign the PD to be a Class 4.'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7** *P* **17** *L* **31** # 170

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *33.2.7*

The draft is in conflict with the folowing motions:

March 2006

The IEEE 802.3at Task Force affirms that a PD requiring more than 12.95W will support a Layer-1 Classification extension and a Layer-2 Classification mechanism. Endpoint PSEs must support Layer-2 classification or Layer-1 classification extension for PDs requiring more than 12.95W.

November 2006

Relevant page from diab_schindler_1106_1.pdf:
Simple Classification Baseline
PSE
- AT L2: Detects and classifies class 4. Communicates with PD in L2. Mutual ID achieved.
- AT L1: Detects and classifies class 4. Repeats classification ("dumb ping-pong"). Mutual ID achieved.
- AT PSEs shall choose the classification extension used.
- Legacy PSEs: Unchanged PD
- AT PD: Use class 4 for all 802.3at PDs. After 1st classification, either
- L2 communication which identifies 802.3at endspan
- Second classification ("dumb ping-pong"). Identifies 802.3at midspan
- Power-on after one classification cycle. Identifies legacy PSE
- Legacy PDs: Unchanged
Power Limits after classifying a Class 4 PD
- AT L2 PSEs enforce legacy limit until L2 is up
- AT L1 PSEs enforce maximum power limit per 802.3at objective
- AT PDs operate under class 0 limits until either L2 is up or second class and power-on
- Legacy PDs and PSEs Unchanged

SuggestedRemedy

Update the draft as follows:

Subclause 33.2.7, page 31, line 31.
Change 'A Type 2 PSE shall perform classification using Type 2 Physical Layer classification and may optionally perform Data Link Layer classification.' to read 'A Type 2 Midspan PSE shall perform classification using Type 2 Physical Layer classification and may optionally perform Data Link Layer classification. A Type 2 Endpoint PSE shall perform classification using either Type 2 Physical Layer classification or Data Link Layer classification.'

Subclause 33.2.7, page 31, line 44
Change 'A Type 2 PSE performs Physical Layer classification of a PD ..' to read 'A Type 2 PSE that performs Physical Layer classification of a PD does so ..'.

Subclause 33.2.9, page 43, line 21
Change 'Where a PSE does not provide either of the Physical Layer classification functions specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs.' to read

Where a PSE does not provide Physical Layer classification functions (see 33.2.7), all PDs are treated as Class 0 Type 1 PDs until successful layer Data Link Layer classification is performed.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7** *P* **17** *L* **31** # 180

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **D** *33.2.7*

A PSE does not have to perform Type 2 Physical Layer classification in order to ensure mutual identification with a type2 PD.

SuggestedRemedy

Replace the sentence on line 31 with:

A Type 2 PSE shall perform type 2 Physical Layer classification and/or Data Link Layer classification.

Proposed Response *Response Status* **O**

see 71

A Type 2 PSE shall perform Physical Layer classification or Data Link Layer classification or both.

A Type 2 PSE may implement PL or DLL classification or both.

A Type 2 PSE that does not perform DLL classification shall implement PL classification.

Question:
Should a Type 2 PSE be required to implement PL classification?

Y: 6, N: 9, A: 2

.3 only:

Y: 3, N: 7, A: 1

Question:
Do we reject the comment?

Y: 8, N: 8, A: 2

Cl **33** *SC* **2.7** *P* **17** *L* **31** # 31

Patoka, Martin TI

Comment Type **E** *Comment Status* **D** *33.2.7*

A Type 2 PSE shall classify a PD to allow mutual identification with a Type 2 PD.

This is commentary that I recommend we strike.

SuggestedRemedy

Strike the sentence.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Classification is PL or DLL and is required and testable.

[pulled out of the 33.2.7 bucket]

Cl **33** *SC* **2.7** *P* **17** *L* **32** # 71

Patoka, Martin TI

Comment Type **TR** *Comment Status* **X** *33.2.7*

"A Type 2 PSE shall perform classification using Type 2
hardware Physical Layer classification and may optionally perform link layer Data Link Layer classification."

We had a motion November 2006 that a type 2 PSE may choose its extension, which I interpret to mean that an endspan need only perform L2 class. This was recorded in the motion aggregator.

SuggestedRemedy

An Type 2 endspan PSE must perform classification using Type 2
Physical Layer classification or Type 2 Data Link Layer classification. A midspan PSE must perform Type 2 Physical Layer classification.

Proposed Response *Response Status* **W**

see 180

Cl **33** *SC* **2.7** *P* **17** *L* **33** # 172

Jones, Chad Cisco

Comment Type **ER** *Comment Status* **X** *33.2.7*

This sentence is the first appearance of Data Link Layer classification in the text and it is not defined.

SuggestedRemedy

Add the sentence: "Data Link Layer classification is a layer 2 protocol. Details can be found in section 33.6." after the paragraph.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7** *P* **17** *L* **35** # 117

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *33.2.7*

Draft0.9:
It is not clear from the text that A Type 2 PSE must do at least Type 1 Physical Layer classification in order to read Class 4 PDs that are Type 2 PDs by definition.
Class 4 IS THE UNIQUE IDENTIFICATION MEANS as required by the 5 Criteria.
Therefore:
PSE Type 2 must do at least 1st finger Physical layer classification to read if it class 1,2,3 or 4.
PSE Type 2 may omits the 2nd finger if it is using Layer 2 classification.
A type 2 PDs must implement both Layer 2 AND Physical layer classification.

SuggestedRemedy

Add the following text at line 35:

"Type 2 PSE shall implement at least one classification event of the Physical Layer Classification as per table 33-4a, to uniquely identify if PD is Type 1 or Type 2. Type 2 unique signature is Class 4 and represents PD max. Power.
If PSE is equipped with Layer 2 classification, it may later communicate with PD type 2 for lower PD power requirements"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Class 4 is the unique identifier required for midspans and that is why PDs are required to display class 4, but an endspan PSE can choose to not class the PD at all and use L2 as the mutual identification method. Since PDs are required to do both, the outcome will be full power in both cases.

[pulled out of the 33.2.7.bucket]

Cl **33** *SC* **2.7** *P* **17** *L* **39** # 167

Law, David 3Com

Comment Type **T** *Comment Status* **D** *33.2.7*

There is no such thing as Type 1 or Type 2 Class 0-4, instead there is Type 1 or Type 2 Physical Layer classification.

SuggestedRemedy

Change the text 'Successful Type 1 or Type 2 Class 0-4 hardware Physical Layer classification.' to read 'Successful Class 0-4 hardware Type 1 or Type 2 Physical Layer classification.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7** *P* **17** *L* **44** # 58

Patoka, Martin TI

Comment Type **T** *Comment Status* **D** *33.2.7*

"A Type 2 PSE performs Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

GIven that an endspan PSE may prefer to do L2 classification, this sentence should be ammended.

SuggestedRemedy

"A Type 2 PSE performs optional Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

Proposed Response *Response Status* **W**

PROPOSED REJECT.

See 216

[pulled out of the 33.2.7.bucket]

Cl **33** *SC* **2.7** *P* **17** *L* **44** # 216

Diab, Wael Broadcom

Comment Type **T** *Comment Status* **D** *33.2.7*

Second sentence needs to have the word may.

SuggestedRemedy

Please rewrite sentence from "A Type 2 PSE performs hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

"A Type 2 PSE may perform hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

Proposed Response *Response Status* **W**

PROPOSED REJECT.
CE Note: this comment was missing a Comment Type. Deemed to be T by CE.

I disagree that the word may adds any value. See 117 for reasoning. See also 58

[pulled out of the 33.2.7.bucket]

Cl **33** *SC* **2.7** *P* **17** *L* **47** # 249

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X** *33.2.7*

There is a should statement here without a PICs. Specifically, the sentence "The PSE hardware Physical Layer classification circuit should have adequate stability to prevent oscillation when connected to a PD."

SuggestedRemedy

One of the following 3 suggestions:
- Either delete the statement all together OR
- Make this a note and remove the word should
- Add a PICs and test associated with this

Proposed Response *Response Status* **W**

see 131

Cl **33** *SC* **2.7** *P* **17** *L* **47** # 131

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **X** *33.2.7*

PSE MUST have stability during classification.

SuggestedRemedy

IS:
The PSE Physical Layer classification circuit should have adequate stability...

SHOULD BE:
The PSE Physical Layer classifciaton circuit shall have adequate stability....

Proposed Response *Response Status* **W**

The shall statement implies a PICS test. What is this test? Cannot approve this comment without the test procedure.

See 249

Cl **33** *SC* **2.7.1** *P* **18** *L* **1** # 48

Patoka, Martin TI

Comment Type **ER** *Comment Status* **D**

"Type 2 PDs are required to implement hardware Physical Layer classification so that a Type 2 PSE implementing
only Type 2 hardware Physical Layer classification may simultaneously indicate indicates its presence
and identify identifies the Type 2 PD's power requirements."

This text places a PD requirement in a PSE requirement section.

SuggestedRemedy

Either turn this text into an informational note or strike.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Make it a note - no shall as this is the PSE section. There is a corresponding shall in the PD section.

See 162

Cl **33** *SC* **2.7.1** *P* **18** *L* **1** # 162

Law, David 3Com

Comment Type **ER** *Comment Status* **X**

The text describing the need for Type 2 hardware classification to be mandatory is a duplication of the text in 33.2.7 (page 31, line 32).

SuggestedRemedy

Delete the text found on lines 1 through 4.

Proposed Response *Response Status* **W**

see 48

Cl **33** *SC* **2.7.1** *P* **18** *L* **11** # 9

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

Table 33-3 is a bit confusing and could be restructured to provide more informational content.

SuggestedRemedy

Replace Table 33-3 with attached table.

P802d3at_D0p9_table_33d3.fm
P802d3at_D0p9_table_33d3.pdf

Proposed Response *Response Status* **W**

see 163, 244

Cl **33** *SC* **2.7.1** *P* **18** *L* **16** # 163

Law, David 3Com

Comment Type **T** *Comment Status* **X**

There are Type 1 and Type 2 PSEs, Type 1 and Type 2 PDs, and there is Type 1 and Type 2 hardware classification. It is therefore unclear what the Type values in the 'Usage' column in Table 33-3 is in reference to. It looks like it is meant to refer to PSE type but Type 1 isn't correct in 0 to 3 as classification is optional.

SuggestedRemedy

Consider removing 'Usage' column.

Proposed Response *Response Status* **W**

see 9, 244

Cl **33** *SC* **2.7.1** *P* **18** *L* **27** # 113

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft0.9:
According to the classification base line concept and associated motions the text should explicitly note that PD that asks more power then advertised in L1 hardware classification is not compliant.

The rational for this was to prevent interoperability issues when a Type 2 PD is connected to end span and get service while if connected to Midspan it will not work due to the fact that Midspan cant support L2.
As a result we mandate PD type 2 to support both L1 and L2 classification and specify that hardware classification results are max. Power values.

In addition it is already specified in the 802.3 specification that all numbers of class power are maximum numbers.

SuggestedRemedy

Add the following text right after Table 33:
"PD that asks more power then advertised in L1 hardware classification is not compliant to this standard".

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2** *P* **18** *L* **31** # 1

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Sentence structure in paragraph could be improved.

SuggestedRemedy

Replace first sentence with:

The Type 1 PSE shall provide to the PI VClass with a current limitation of IClass_LIM, as defined in Table 33-4a. Polarity shall be the same as defined for VPort in 33.2.2 and timing specifications shall be as defined by Tpdc in Table 33-5. The Type 1 PSE shall measure the resultant IClass and classify the PD based on the observed current according to Table 33-4. Measurement of IClass shall be taken after 1ms to ignore initial transients. If the measured IClass is greater than or equal to 51mA, the Type 1 PSE shall classify the PD as Class 0.

Response *Response Status* **C**

ACCEPT.

CE Note: comment had no assiciated comment type. Set as E by default.

Cl **33** *SC* **2.7.2** *P* **18** *L* **31** # 95

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Draft0.9:
From the current specification it is understood that the classification voltage at the PSE is between 15.5V to 20.5V from t=0 to the end of the classification time duration.
To increase design flexibility it is better to allow higher peak voltage then 20.5V for limited time as long as it is well below 30V.
It is suggested to use 28V max peak voltage for 1msec max. which is 10% margin from the 30V minimum PD disconnection voltage.

SuggestedRemedy

Add the following normative text to the classification voltage requirements which is applicable for Type 1 and 2 PSEs:
"During classification voltage turn on, a transient voltage up to 28V for time duration of 1msec max. is allowed."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2** *P* **19** *L* **44** # 91

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **D**

"Undefined" is not clear enough in this case.
It is suggested that in this case it will be explicitly noted that it is a system decision.

SuggestedRemedy

To add .."and subject to system decision"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7.2a** *P* **18** *L* **40** # 225

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

This section needs to be restructured so we can write PICs around this. The baseline allows a Type 2 PSE to do HW or Data Link Layer classification. The way this is worded basically says that HW is the mandatory classification technique and there may be an exception to do Data Link Layer. This does not work well with doing PICs.

This will apply throughout this section.

SuggestedRemedy

The statement "Type 2 PSE shall do Physical Layer or Data Link Layer classification." can be inserted into the introductory section for PSE Classification of PDs.

A self contained description of what the requirements are of a Type 2 Data Link Layer Classification engine looks like (including the supporting underlying Physical Layer state machine --- Type 1 HW) and a similar set for Type 2 Physical Layer requirements are necessary. Individual statements in each section stating that a Type 2 PSE May Classify Type 2 PDs using the respective technique is necessary.

This translates better to PICs I believe than writing one as an exception of the other.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **18** *L* **42** # 59

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

"The Type 2 PSE shall provide to the PI VClass as defined in Table 33–4a."

H/W L1 class is optional.

SuggestedRemedy

"The Type 2 PSE may optionaly provide an enhanced hardware classification to the PI which consists of the following sequence where levels are defined in Table 33–4a. The PSE provides strong sourcing current and weak sinking current.
* Apply Vclass
* Allow settling time
* Measure Iclass
* Apply Vmark
* Allow settling time
* Apply Vclass
* ...

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **19** *L* **22** # 132

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D**

Text allows PSE to drop port voltage to reset during 2-event classification. Text should disallow PSE from dropping port voltage during classfication.

SuggestedRemedy

IS:
If at any point during the classification sequence the PSE allows the voltage at the PI to enter the VReset range as defined in Table 33–4a, the PSE shall classify the PD as Class 0.

SHOULD BE:
The Type 2 Physical Layer PSE shall complete Physical Layer classification and transisiton to the POWER-ON state without allowing voltage at the PI to go below Mark Event Voltage (VMark). If at any point prior to POWER-ON, the PI voltage drops below VMark, the classification is invalid. Subseqent behavior is undefined.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 194, 103

Cl **33** *SC* **2.7.2a** *P* **19** *L* **22** # 194

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

The intent of the sentence is not clear: "If at any point the classification sequence the PSE allows the voltage at the PI to enter the VRESET range as defined in Table 33-4a, the PSE shall classify the PD as Class 0."

The intent appears to require that the PSE and PD remain synchronized. If the PSE causes a reset the PSE should assume the PD has been reset. It takes time for the PSE/PD to sense the reset condition.

SuggestedRemedy

Clear outline the requirements and purpose.

Proposed Response *Response Status* **W**

see 132, 103

Cl **33** *SC* **2.7.2a** *P* **19** *L* **23** # 103

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft D0.9:

If PSEs PI voltage enters to Reset range prior to powerup then PD may lost its indication data

SuggestedRemedy

To add the following text after line 23:
"1. PSE shall maintain 7V minimum across the PI after classification phase is done until startup phase. If port voltage falls below 7V after classification phase is ended and PSE is starting up, the PSE may classify the PD as class 0."

Proposed Response *Response Status* **W**

see 132, 194

Cl **33** *SC* **2.7.2a** *P* **19** *L* **25** # 119

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Drfat0.9:
According to the current text the PSE is required to measure the class current and the mark current.
It looks that it is not cost effective and not technically required to measure it twice over the time domain with short time intervals.
It is sufficient to measure Iclass and check its value if it match one of the values of the class current or if it is > Iclass-_lim.
It is not important if I>Imark_lim due to the following reasons:
1. It is not cost effective to measure Imark_lim with in 6-12msec time frame just after that Iclass has been measured.
2. At the worst case if Imark_lim is wrong and cause Vmark to be out of range, then it will be reflected to a bad class reading which will be handled by the PSE anyway so it is redundant measurement and technically difficult one.
3. Imark timing is PD dependent and PSE will have difficulties to guess where and when to measure especially in multi-port systems where many operations are done in parallel to others.
4. And most important the need for measuring Imark is not required by the concept for we choose proper operation.

SuggestedRemedy

1. Delete the need for measuring Imark from the PD state diagram and the normative text in page 19 lines 24-29.
2. Use the parameter of Iclass_lim_max for the entire classification period with the same max. value i.e. 100mA max for the class and mark time duration.
3. Set Imark_lim_min to 5mA (to have margin from Imark_max=2mA)

Proposed Response *Response Status* **W**

see 133

Cl **33** *SC* **2.7.2a** *P* **19** *L* **25** # 134

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **X**

.af treated any PDs that classed with too much current (>51mA, ie. >class 4) as class 0.

Should .at treat such PDs as class 0 or class 4?

Today, the draft treats them as class 0. I would suggest they be treated as class 4.

Corrected text as follows:

SuggestedRemedy

IS:
If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0.

SHOULD BE:
If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 4.

Proposed Response *Response Status* **W**

see 166

Cl **33** *SC* **2.7.2a** *P* **19** *L* **26** # 133

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **X**

In the 8/29/07 Classification Ad Hoc meeting, it was generally agreed that the PSE does not need to measure PI current during the Mark Event. Remove text to this effect.

SuggestedRemedy

IS:
If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0. If any measured IMark is greater than or equal to IMark_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0. Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.

SHOULD BE:
If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0.
DELETE REST OF PARAGRAPH

Proposed Response *Response Status* **W**

see 119

Cl **33** *SC* **2.7.2a** *P* **19** *L* **28** # 118

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft 0.9:

When PSE classify the PD after Icalls_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to adress this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset=5 to 30msec (TBD).

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **19** *L* **35** # 201

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D**

A PSE can legally detect and power on a PD without classifying a PD. This allowance should continue.

SuggestedRemedy

Replace the sentence at line-34 with:
If classification is not performed or the result of the first classification event is class 4, …

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7.2a** *P* **19** *L* **35** # 166

Law, David — 3Com

Comment Type **T** *Comment Status* **X**

Make it clear what classification a PD should have from a single class even that returns Class 4. The text currently says it should be treated as a Type 1 PD, but doesn't say of what class. I believe the PD should be classified as Class 0.

SuggestedRemedy

Suggest that the text 'In this case, the Type 2 PSE shall assume it is powering a Type 1 PD until successful link layer classification is performed.' be changed to read 'In this case, the Type 2 PSE shall classify the PD as Class 1'. (CE NOTE: should this be class 0?)

Proposed Response *Response Status* **W**

see 134

Cl **33** *SC* **2.7.2a** *P* **19** *L* **40** # 181

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X**

A PD should be able to ask for the power it requires.

Three independent classification mechanisms exist: type 1 and 2 Physical layer and type 2 Data Link Layer. Interoperability is ensured when a PD requests power from a PSE that can interpret the request. A type 2 PD can use type 1 Physical layer classification to request power.

SuggestedRemedy

Replace the sentence on line 40 with,
If the result of the first classification is any classes 0, 1, 2, 3, the PSE may omit the subsequent mark …

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **19** *L* **45** # 253

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

I like the note. I would suggest that we have a default in case this case happens for some error in the system. Undefined behaviour is scary

SuggestedRemedy

I would suggest that the whole detection process is restarted and no power is applied if the 2 results are different.

Proposed Response *Response Status* **W**

see 91

Cl **33** *SC* **2.7.2a** *P* **20** *L* **11** # 135

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **A** *t33-4a*

In the 8/29/07 Classification Ad Hoc meeting, it was generally agreed that current limit during Mark Event should be 5mA minimum, 100mA maximum.

SuggestedRemedy

IS:
2b Mark Event Current Limitation IMark_LIM mA 2(min) 5(max)

SHOULD BE:
2b Mark Event Current Limitation IMark_LIM mA 5(min) 100(max)

Response *Response Status* **C**

ACCEPT.

see 27

Cl **33** *SC* **2.7.2a** *P* **20** *L* **12** # 27

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **TR** *Comment Status* **A** *t33-4a*

IMark_LIM is unnecessarily restrictive. It should encompass both classification circuit and detection circuit current limitations for maximum implementation flexibility.

SuggestedRemedy

Change to IMark_LIM min 5mA, IMark_LIM max 100mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. see 135

Cl **33** *SC* **2.7.2a** *P* **20** *L* **19** # 136

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **A** *t33-4a*

In the 8/29/07 Classification Ad Hoc meeting it was discussed that setting a 2nd Mark Event Timing maximum time (currently 30ms) forces the PSE to quickly perform power allocation calculations and power the port. This was not the intent and there is no need to set a maximum time. The maximum specification should be blank. Note that the PSE is required to power the port (if it chooses) within 400ms (tpon) of completion of detection.

SuggestedRemedy

IS:
6 2nd Mark Event Timing TME2 ms 6(min) 30(max)

SHOULD BE:
6 2nd Mark Event Timing TME2 ms 6(min) (blank max)

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.7.2a** *P* **20** *L* **19** # 100

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **A** *t33-4a*

table 33-4a.:
According base line, 1st and 2nd mark event duration should be the same i.e. 12msec max. 30msec was inserted in item 6 table 33-4a.

On the other hand we have discussed that the 2nd mark event time may last until power on per Tpon in table 33-5.

My recomendation is to extend 2nd mark event until power up within Tpon max due to the fact that if PSE decides to power the port after classification, it required to maintain 7V minimu anyway until power on otherwise classification data may be lost.

SuggestedRemedy

Change item 6 to Tpon_max per table 33-5 as the max. value.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. see 136

Cl **33** *SC* **2.7.2a** *P* **20** *L* **20** # 203

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **A** *t33-4a*

In the 8/29/07 Classification Ad Hoc meeting, it was generally agreed that timing should be added to define Class Event 3

SuggestedRemedy

Add to Table 33-4a

3rd Class Event Timing TCLE3 ms blank(min) 30(max)

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.7a** *P* **21** *L* **3** # 246

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

We still need to have a section on Link Layer here. I believe the material in 33.6 is intended to complement 33.2.7a (or whichever way we end up renumbering it) even if it is a reference to a later section. Otherwise its confusing.

For example, the timing relation between the data-link layer and the Type 1 physical layer needs to be defined and described

SuggestedRemedy

See Comment. We need to have a control section in addition to the management section.

Proposed Response *Response Status* **W**

page number does not correspond to comment. What page?

Cl **33** *SC* **2.8** *P* **24** *L* **4** # 228

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X**

The statement on what the PSE can meet seems a bit confusing. I think that the intention is that a Type 2 PSE powering a Type 1 PD has a set of parameters it needs to meet. Of these, a subset has to be met under Type 1 and a subset may be met by either Type 1 or Type 2.

I believe the statement should be more clear with the optional parameters being stated seperately.

SuggestedRemedy

When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the electrical requirements of a Type 1 PSE for the following list of parameters (All parameters except 4, 8 and 10).

When a Type 2 PSE powers a Type 1 PD, the PSE may meet the electrical requirements of a Type 1 PSE or a Type 2 PSE for the following list of parameters (4, 8 and 10).

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8** *P* **24** *L* **4** # 76

Dove, Daniel — ProCurve Networking

Comment Type **TR** *Comment Status* **X**

Lines 4-6: This sounds like a recipe for disaster. Allowing a Type 2 PSE to apply currents to a Type 1 PD that exceed its specifications means that if it has a fault which would normally cause an over-current event, it will not. This has a strong chance of causing the magic smoke to leak out of the PD rendering it red and excessively hot.

SuggestedRemedy

Remove this.

Proposed Response *Response Status* **W**

Cl **33** *SC* **2.8** *P* **25** *L* **15** # 107

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-5*

Draft0.9:

Table 33-5 item 10:
Replace TBDs with numbers or figure 33-9a data.

SuggestedRemedy

1) ILIM_MAX=SOA curve.
2) ILIM_MIN=Icable * (400/350)

3. Add the following text to 33.2.8.8 after line 45:
"Minimum ILIM for Type 2 PSE when implementing constant current limit shall be 870mA minimum in order to support the scenario of positive PSE dv/dt which cause to PSE to be at ILIM simultaneously when PD is consuming 820mA for up to 50msec.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

1) ILIM_MAX= (blank).
2) ILIM_MIN=(Pport/Vport) * (400/350)

Cl **33** *SC* **2.8** *P* **25** *L* **15** # 187

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A** *t33-5*

The specification requires that a PSE remove power based on ILIM and TLIM thresholds. The selected levels are not required to ensure interoperability or meet the safety specifications, and therefore, are unnecessarily restrictive.

SuggestedRemedy

A PSE system needs to operate within the region between PD current needs (TBD) and SOA current limits (current limit and duration).

Allow existing ILIM requirements or current requirements derived from figure 33-9a SOA requirements.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.8** *P* **25** *L* **16** # 109

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **R** *t33-5*

Draft0.9:

Table 33-5 item 11.

Type 1 and Type 2 PSEs may have different TLIM_MIN and TLIM_MAX.

SuggestedRemedy

1. Split item 11 to type 1 and type 2 PSE.
Updated numbers/curves will be supplied by the Vport ad hoc.

2. Update 33.2.8.9 accordingly.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Will recomment after section is updated in next draft.

Cl **33** *SC* **2.8** *P* **25** *L* **18** # 92

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **A** *t33-5*

Draft0.9:
Table 33-5 item 12:
Add test condition for Tr. It is not clear how to measure it as PSE alone.

SuggestedRemedy

Option 1:

To delete this requirement due to the fact that this parameter is controlled by other standards such as EN50022 (EMI).
Tr has no effect on data due to low common mode channel bandwidth and due to the fact that it is not a repetitive signal at the data frequency domain. It may occure once every 750msec min. at the worst case.

Option 2:
To add test condition:"At minimum capacitive load of 50A*15usec/44V=17uF
Iport_transient= Iport at the time range of 15usec.
Iport value at 15usec is define by the SOA curve.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

add test condition:"with minimum capacitive load of TBDuF", change to TBD dV/dt specification.

Cl **33** *SC* **2.8** *P* **25** *L* **23** # 182

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A** *t33-5*

All references requiring a PSE to provide 15.4 W/(TBD AT power) minimum do not match the state diagram shown in figure 33-6. Also see p26, l31 and 32; p70, PSE37.

SuggestedRemedy

In all cases, the PSE provides the power the PD requests or it does not power the PD. The power provided is Pport.

table 33-5, item 14 can be deleted;

33.2.8.4, p26, l31-32, and p26, l49-50, replace numerical value with Pport;

P70 PSE36, replace numerical value with Pport. This assumes the PSE can provide only Pport and not provide the maximum allowed by the standard.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

replace table 33-5, item 14 with Pclass
Pclass is the power defined in 33.2.7 or the result of DLL class as defined in 33.6.

33.2.8.4, p26, l31-32, and p26, l49-50, replace numerical value (15.4W and 36W) with Pport;

Cl **33** *SC* **2.8** *P* **25** *L* **38** # 105

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-5*

Draft0.9:
1. Classification time Tpdc for type 1 and 2 PSE's are different.

SuggestedRemedy

Split item 20 in table 33-5 for type 1 and type 2 PSEs:

Add the following data for type 2 PSE:
Tpdc min. = 12mesec for PSE using layer 2 which uses only single finger.
Tpdc max.= per the max. values in table 33-4a.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Split item 20 in table 33-5 for type 1 and type 2 PSEs:

Leave type 1 as is.
Add the following data for type 2 PSE:
point to table 33-4a.

Cl **33** *SC* **2.8** *P* **25** *L* **7** # 32

Patoka, Martin TI

Comment Type **E** *Comment Status* **A** *t33-5*

Clause 33.2.8.6 ammends the value in item 8 to Pclass / Vport.

PSE operation would be more easily understood if this limit was shown in the table.

SuggestedRemedy

Suggest adding lines 8a & 8b with the limits of (Pclass * 1000)/Vport with the note "Optional limit see 33.2.8.6" aligned with them.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change minimum entries on line 8 with the limits of (Pclass * 1000)/Vport with the note "Optional limit see 33.2.8.6" aligned with them.

Delete P_class in the note in 33.2.8.6 and use Pclass defined in comment 182.

Cl **33** *SC* **2.8** *P* **7b** *L* **49** # 143

Johnson, Peter Sifos Technologies

Comment Type **TR** *Comment Status* **X** *t33-5*

Tmps, Table 33-5 Item 7b, is presented from the perspective of a PD, not a PSE, it seems. 60 msec is the Minimum Valid Load Current Time that a PD must sustain to assure the PSE will keep it powered. From the PSE's perspective however, Tmps is the MAXIMUM allowed Valid (Imin2) Load Interval over which the PSE does not have to reset its Tmpdo timer (and therefore delay a shutdown). Since this parameter is expressed as a minimum, it can be (and has been) interpreted as the Minimum Valid Load Time required to re-start shutdown timing.

SuggestedRemedy

Title the Parameter in 33-5, 7-b, "Valid DC MPS Signature Time Required to Restart Disconnect Shutdown Timing". "60 msec" should then become a MAXIMUM limit, not a MINIMUM limit.

Proposed Response *Response Status* **W**

Need to clarify text.

Cl **33** *SC* **2.8.1** *P* **25** *L* **50** # 178

Johnson, Peter Sifos Technologies

Comment Type **T** *Comment Status* **X**

The requirement that "A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the Vport specification" essentially negates the broader purpose of specifying Iinrush, Tlim, and Ilim elsewhere in the specification. PSE's that enter a current limiting state, as defined by Iinrush, Ilim, and Tlim will in all likelihood drop below the Minimum Vport level since they are funtioning as current sources (400 to 450mA), not voltage sources in this mode. This behavior is time-bounded by Tlim, of course.

Since Iinrush, Ilim, and Tlim provide robustness within PoE to handle marginally compliant transient overload conditions, it seems unwise to undermine those requirements with this clause. Also, 33.2.8.8 now adds further criteria ("SOA" Type 2 PSE's) for removing power based upon transient overload current designed to protect PSE's and interconnect integrity. The relevance of that criteria would be undermined by this particular clause.

Finally, this clause is simply inconsistent and contradictory with 33.2.8.8 b).

SuggestedRemedy

Revise 33.2.8.1 as follows:

Replace:

"A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the Vport specification"

With:

"The Minimum Vport specification in Table 33-5 shall not apply to PSE's operating in a current limiting condition over the period Tlim as defined in 33.2.8.5 and 33.2.8.8."

Proposed Response *Response Status* **O**

Cl **33** SC **2.8.1** P **25** L **51** # 137

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **X**

A new statement is added:

"A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the VPort specification."

This is inconsistant with many other entries in the specification, for example Table 33-5, item 11, Short Circuit Time Limit, TLIM, 50ms minimum.

SuggestedRemedy

Remove the statement:

"A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the VPort specification."

Proposed Response *Response Status* **O**

Cl **33** SC **2.8.12** P **29** L **1** # 188

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A**

The current imbalance requirements need to be reevaluated for PoE plus levels. For example, the main source of imbalance is connector resistance. This same resistance is now over a much lower channel resistance and this will cause a larger than 3% current imbalance.

Millions of PoE ports are in use with cable lengths significantly less than 80 m (the value used to determine the legacy 3% imbalance value). A short cable length increases the current imbalance to levels where many transformers can not guaranty the 350uH inductance requirement of IEEE 802.3 yet ports continue to operate as expected. Therefore, assumptions made by the IEEE should be re-evaluated.

SuggestedRemedy

A transformer ad hoc should be formed to create system requirements for Ethernet transformers that ensure compliant systems are acceptable to the broader market.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

AdHoc will be created. Fred will chair the AdHoc.

Cl **33** SC **2.8.12** P **29** L **5** # 79

Dove, Daniel — ProCurve Networking

Comment Type **T** *Comment Status* **A** *t33-5*

If the line is true about 3%, then why is the table entry for type 2 PSE's a TBD?

SuggestedRemedy

Not sure..perhaps filling in the TBD will solve it.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

AdHoc formed as a reasult of 188

Cl **33** SC **2.8.2b** P **26** L **17** # 10

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **T** *Comment Status* **X**

Text implies voltage transient specification applies to all PSEs, when it really only applies to Type 2 PSEs.

SuggestedRemedy

Change sentence to read:

"A Type 2 PSE shall maintain..."

Proposed Response *Response Status* **O**

Cl **33** SC **2.8.2b** P **26** L **18** # 77

Dove, Daniel — ProCurve Networking

Comment Type **TR** *Comment Status* **X**

The part "Transients less than 30uS...may exceed this spec" has no limit. While its unlikely, a billion amps for 29uS would be allowed. There should be a limit.

SuggestedRemedy

Either strike the sentence, or apply an absolute maximum limit.

Proposed Response *Response Status* **W**

There is a limit, what is it? If we add a shall, we have to test it…

Cl **33** *SC* **2.8.3** *P* **26** *L* **24** # 85

Darshan, Yair — Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Draft0.9

Ripple and noise should be met with 0.44W minimum load up to Pport max.

SuggestedRemedy

Change from 0.4 4W to 0.44W

Proposed Response *Response Status* **W**

is this two comments (what is the Pport max reference)?

Cl **33** *SC* **2.8.4** *P* **26** *L* **36** # 183

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X**

The statements are not clear: is "a" or "b" required?
Option "b" has no time or duty cycle constraint provided. These comments also apply to the new section 33.2.8.4a.

SuggestedRemedy

Allow options "a" or "b."
Have one statement for duty cycle and time that applies to both "a" and "b".

The same comments apply to section 33.2.8.4a and table 33-12.

See a related comment on section 33.3.5.4.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.4** *P* **26** *L* **37** # 195

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X**

The formula for IPEAK ensures a constant PSE power of 17.6 W. To ensure interoperability the PSE needs to provide what the PD can demand.

The PD may demand 14.4 W. When the PSE is providing 44 V, the PSE must provide 17.6 W. However, when the PSE is providing 57 V, the PSE only needs to provide 16.0 W to support the same PD demand. This unnecessary power requirement increases when using PoE plus power levels. These requirements place an unnecessary burden on the PSE.

These comments also apply to 33.2.8.4a.

This comment is related to other comments on this same section and the PD table 33-12 and 33.3.5.2.

SuggestedRemedy

If the PD is a constant power load that can demand 400/350Iport more, then determine the PSE power for a given PD demand, divide this PSE power by the PSE voltage to get IPEAK. This is a quadratic equation.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.4a** *P* **26** *L* **49** # 120

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-5*

The behavior of Type 1 PSE should be similar to the behavior of type 2 PSE in terms of supporting ac current waveforms parameters (Similar PDs environment just more power, similar application load accuracies, similar circuit tolerances and margins..).

The concept in type 1 is working well and do not increase the burden on PSE Power Supply due to the fact that the specification requires that the average current and the rms current will be the same number which is equal to the max. DC operating cable current i.e. 720mA which is the same concept used in Type 1.
Therefore no additional power is required from the PSE PS hence no additional cost. We just improved system robustness for PD load dynamic changes which exceeds max. DC current for limited time duration and duty cycle.

The above is a physical fact.

See 802.3af documentations/presentations more details.
See contribution sent to 802.3at task force for September 2007 meeting which summarize this issue again.

SuggestedRemedy

In 33.2.8.4a:
Change TBD in item a line 49 to 823mA. (or 820mA)
Change TBD in item b LINE 50 to 36*0.4/0.35=41.14W

Table 33-5:
Item 10 for type 2 minimum value: Change TBD to 820mA min.

Table 33-12 item 4:
Change TBD max. value to 820mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In 33.2.8.4a:
Change TBD in item a line 49 to Icable * (400/350).
Change TBD in item b LINE 50 to Pport* (400/350)

Table 33-5:
resolved by 107.

Table 33-12 item 4:
Change TBD max. value to Icable * (400/350).

Cl **33** *SC* **2.8.5** *P* **26** *L* **52** # 60

Patoka, Martin — TI

Comment Type **T** *Comment Status* **X**

Startup mode not defined. Requirement is uncertain.

SuggestedRemedy

"Startup mode occurs between the PSE transition to powerup (application of voltage >42V) and the lesser of Tlim or the conclusion of PD inrush currents."

Remove item a) and renumber. Startup is an isolated event and I see no reason why there is a duty cycle associatred with it.

I sugest that we move items d) & e) into 33.2.8.8. Commented separately.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.5** *P* **27** *L* **7** # 110

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft 0.9:
There is no definition of the requirements for ILIM between 0V to 10V.
The proposal below was part of maintenance request 1162.

SuggestedRemedy

Change 33.2.8.5 item e from:

e) During startup, for PI voltages between 10V and 30V, the minimum IINRUSH requirement is 60mA.
See Figures 33C.4, 33C.6.

To:
e) During startup, for PI voltages between 10V and 30V, the minimum IINRUSH requirement is 60mA.
During startup, for PI voltages between 0V and 10V, the max IINRUSH requirement is as specified by Table 33-5, item 10.
See Figures 33C.4, 33C.6 and 33C.6.1.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.5** *P* **27** *L* **9** # 121

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft0.9:
In many ocasions the normative text send the reader to see figures 33C.4 and 33C.6 which contains valuble data.
These drawings should be at the normative text as it was in early drafts of 802.3af and were moved to the informative section due to editing considerations.

SuggestedRemedy

Move figures 33C.4 and 33C.6 to the normative section at the location where they are mentioned for the first time.

Proposed Response *Response Status* **W**

see 50

Cl **33** *SC* **2.8.6** *P* **27** *L* **11** # 50

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X**

Overload is used in a particular way, and the requirement is difficult to understand. Also, confusion persists about the relationship of the ranges.

SuggestedRemedy

add definition:
"Overload is defined as the load current range between the maximum current defined in 33.2.8.4 and the short circuit current defined in 33.2.8.8"

Move figure 33C-6 from the informative into this section to support the normative text.
Create a second figure to support .at.

Proposed Response *Response Status* **W**

see 121

Cl **33** *SC* **2.8.6** *P* **27** *L* **11** # 186

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X**

The specification requires that a PSE remove power based on maximum ICUT and Tovld thresholds. This does not ensure interoperability or meet the safety specifications, and therefore, forces a design requirement.

SuggestedRemedy

Allow the existing requirement or figure 33-9a SOA requirements to specify what is required for compliance.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.6** *P* **27** *L* **17** # 7

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Extra space between paragraph and equation unnecessary. More space needed after list of variables.

SuggestedRemedy

Remove space before equation. Add space after variable list.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.8.8** *P* **27** *L* **33** # 185

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X**

This section needs to be modified in order to permit PSE to reach current levels just below the SOA described in figure 33-9a.

SuggestedRemedy

If a PSE provides current that meets system safe operating (SOA) requirements, IEC 60950, and PD minimum power needs, then safety and interoperability are met with fewer design requirements imposed. Within the region between PD current needs and SOA current limits, a PSE system selects the design (current limit, current cut-off, and duration) that meets its markets needs. See Vport ad hoc current limit presentations for the latest proposed system current vs time limits.

Suggested remedy:
Type-1 PSE can power as described in this section.

Add, Type-2 PSEs
Remove the requirement to remove power within TLIM, and require that the PSE meet the SOA limits.
Remove the sentence "Measurement to be taken after 1 ms to ignore initial transients."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **27** *L* **33** # 61

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

The term "short circuit" is not defined, arising to much confusion about table 33-5. Also, there has been much discussion about the foldbacl of 33.2.8.5. Many veterans believe that the inferred foldback applies to short circuit as well as startup.

SuggestedRemedy

Add definition: "The short circuit condition occurs when the PSE output is loaded beyond the overload range (Icut_max) and some form of hardware limiting occurs to keep the maximum output current below Ilim_max."

I have suggested 33C-6 be move to normative text, so the reference should change.

I recommend that the foldback limits of 33.2.8.5 be moved here and an output I/V curve be provided. These have been discussed in maintenance.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **27** *L* **41** # 108

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft0.9:
The specification allows foldback current limit implementations in startup mode as defined by 33.2.8.5.
MR request 1162 material and maintenance group attached drawing shows that the intent of the specification was to allow the same implementations during short circuit condition as well. However items d and e of 33.2.8.5 was not copied to 33.2.8.8 as should have done.

SuggestedRemedy

1. Move drawing 33C.4 or its updated version as a result of the Vport ad-hoc work to the normative section as it was in the early drafts of the IEEE802.3af.
2. Move drawing 33C.6 or its updated version as a result of the Vport ad-hoc workto the normative section as it was in the early drafts of the IEEE802.3af.
3. Add drawing 33C.6.1 to 33.2.8.8

4. Replace the following text:

The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC input voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
See Figure 33C.4 and Figure 33C.6.

With the proposed text: (items d and e are additions to previous text)
The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC output voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
d) During short circuit condition, for PI voltages above 30V, the ILIM requirement is as specified in Table 33-5, item 10.
e) During short circuit condition, for PI voltages between 10V and 30V, the minimum ILIM requirement is 60mA as long as system decides to keep the port ON, and the maximum requirement is as specified in Table 33-5, item 10.
During short circuit condition, for PI voltages between 0V and 10V, the minimum ILIM requirement is 0mA and the maximum requirement is as specified in Table 33-5, item 10.
See Figures 33C.4, 33C.6 and 33C.6.1."

5. Add the following notes after 33.2.8.8-e:

Notes:

1. Items d and e in 33.2.8.8 allows implementation of foldback
current limit type in which ILIM requirement is decreased if Vport is

decreased below pre specified value.

2. Short circuit condition definition in IEEE802.3af is a case in which the port voltages is dropped below normal operating voltages as defined by table 33-5 items 1 and 2 due too load fault conditions that exceeds table 33-5 item 8"

6. Add the following note text after 33.2.8.5-e:

Note: items d and e in 33.2.8.5 allows implementation of foldback current limit type in which Iinrush requirement is decreased if Vport is decreased below pre specified value.

Foldback current limit is optional in the standard.

IMPACT ON EXISTING NETWORKS:

No impact. It is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **27** *L* **43** # 96

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Power can not tremoved "immidiatly" this term is not well defined.

SuggestedRemedy

Change to "Power shall be removed within 1msec from the PI of Type 2 PSE...."

Proposed Response *Response Status* **W**

see 78

Cl **33** *SC* **2.8.8** *P* **27** *L* **43** # 28

LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **X**

Is there any reason not to make SOA curve applicable to Type 1 PSEs as well as Type 2 PSEs? All safety and existing peformance studies obviously made use of Type 1 equipment. Further, the SOA curve is well outside of the ILIM max defined for Type 1, therefore it should be impossible for a compliant Type 1 device to violate this new SOA requirement.

SuggestedRemedy

Strike "Type 2"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **27** *L* **43** # 78

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X**

I am not sure how to solve this issue, but the assertion to remove power immediately upon PI current exceeding the limit makes me concerned about the response to a large transient causing the output FET to turn off and then inductance taking over and blowing things up. The test for this is going to be a challenge.

SuggestedRemedy

Change the term "immediately" to something more specific.

Proposed Response *Response Status* **W**

see 96

Cl **33** *SC* **2.8.8** *P* **27** *L* **49** # 122

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Change the Fusing equation in a way that refect all its parameters.
See "Fusing equation: how it was derived in 802.3af" presentation for September 2007 for more details.

SuggestedRemedy

Change from I=(0.025/t)^0.5
To: Iport=(K/t)^0.5
Where
Iport is the current at the PI
t is the duration that the PI sources Iport
K is a 25mJoul energy limitation of the port current when it is not in steady state normal operation.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **28** *L* **32** # 215

Vetteth, Anoop Cisco

Comment Type **T** *Comment Status* **X**

Figure 33-9a
The point on the y-axis (Iport) indicating 720mA is actually 820mA according to the presentaion schindler_1_0719.pdf

SuggestedRemedy

Change 720mA to "Icable x 400/350"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **28** *L* **32** # 23

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

Figure 33-9a title does not specify which PSE Type to which is applies, but the SOA curve applies only to Type 2 PSEs.

SuggestedRemedy

Replace title with:

'Type 2 PSE PI Safe Operating Area'

Proposed Response *Response Status* **W**

see 28
someone also commented that it could apply to type 1 also (Law?)

Cl **33** *SC* **2.8.8** *P* **28** *L* **35** # 8

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Editorial directive (Insert Figure) should appear above the appropriate figure.

SuggestedRemedy

Move "Insert Figure" above Figure 33-9a.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.8.9** *P* **28** *L* **39** # 111

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

Draft0.9:
33.2.8.9 text is true for the case that system (PSE and PD) are within their normal voltage operating range however it is not clear from the text.
It is clear from figure 33C.4 and 33C.6 which are located in the informative section.

SuggestedRemedy

Replace 33.2.8.9 text from:

"If a short circuit condition is detected, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33-5. See Figure 33C.4 and Figure 33C.6."

to:

For PI voltages within PI normal operating voltage range as defined by table 33-5 item 1, If a short circuit condition is detected, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33-5.
See Figure 33C.4, Figure 33C.6. and Figure 33C.6.1"

For PI voltages below or above Vport normal operating range as defined by table 33-5 item 1, If a short circuit condition is detected, power removal from the PI may begin at any time of t<TLIM and be complete by TOff, as specified in Table 33-5.
See Figure 33C.4, Figure 33C.6. and Figure 33C.6.1"

Proposed Response *Response Status* **W**

see 50, 121

Cl **33** *SC* **2.8.9** *P* **28** *L* **39** # 11

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

When violating the SOA curve in Figure 33-9a, TLIM is too long to wait for power removal. The current normative text in this section should apply only to Type 1 PSEs and Type 2 PSEs w/ ILIM current limiting.

SuggestedRemedy

Change text to read:

If a short circuit condition is detected by a Type 1 PSE or a Type 2 PSE implementing ILIM current limitation, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33-5. See Figure 33C.4 and Figure 33C.6.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.9** *P* **29** *L* **20** # 242

Diab, Wael — Broadcom

Comment Type **T** *Comment Status* **X**

This is not accurate as it does not include the Data Link Classification.

SuggestedRemedy

Please rewrite the following sentence to either one of these:

"Where a PSE does not provide either of the Physical Layer classification functions specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs."

TO

"Where a PSE does not provide the classification function specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs."

OR

"Where a PSE does not provide either of the Physical Layer or Data Link Layer classification functions specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.9** *P* **29** *L* **26** # 148

Law, David — 3Com

Comment Type **T** *Comment Status* **X**

The text states that '.. and the mechanism for obtaining that additional information, is beyond the scope of this standard ..'. I do not believe that is true anymore due to the link layer classification protocol.

SuggestedRemedy

Reword to acknoledge link layer classification.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.9** *P* **29** *L* **26** # 16

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **TR** *Comment Status* **X**

It unclear to me why using historical power consumption information should not be a valid means of managing power allocation. The sentence starts by saying it is out of scope, but then goes on to start placing restrictions on what is allowed. Furthermore, how would one even test compliance to this normative exclusion?

SuggestedRemedy

Strike the phrase:

"with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD."

Proposed Response *Response Status* **W**

is this Thompson text? I don't remember the origin.

Cl **33** *SC* **3.1** *P* **33** *L* **23** # 80

Dove, Daniel — ProCurve Networking

Comment Type **ER** *Comment Status* **X**

Table 33-7; This is a broad issue, but for the table you reference "Mode A and Mode B" whereas in the PSE section, they are "Alternate A and Alternate B". Is this intentional?

SuggestedRemedy

I think we need consistency for terminology for Modes, Alternatives, etc.

Proposed Response *Response Status* **W**

Isn't Alt A and B different from Mode A and B. Alt is the opwering mode of PSE, all tied together or ports isolated from each other? Mode is the cable pairs, 1,2,3,6 or 4,5,7,8.

Cl **33** *SC* **3.1** *P* **33** *L* **42** # 124

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

The note in line 42 precludes the following applications:
1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD.

2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or power application.

The standard should not preclude implementations that are using standard compliant 2P system.

Theoretically a PD can get N x 2P power sources while each of the 2P system is well defined by the standard and the standard should not preclude it since it is implementation issue and it is not a source of interoperability issues.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:
"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode are not precluded by this standard as long as the requirements of this standard are kept for each mode."

Other equivalent wording is possible.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.1** *P* **33** *L* **42** # 254

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **R** *rej*

I dont recall that we formally made a decision to change the draft from disallowing 4-pairs to treating them as out of scope. The draft should reflect the decisions made in the group, I would request that we retain the old wording and formalize the decision in the TF first.

SuggestedRemedy

Please return the original text until we make a formal decision on this in the group

Response *Response Status* **U**

REJECT.

The text says not allowed.

Cl **33** *SC* **3.1** *P* **34** *L* **10** # 173

Jones, Chad — Cisco

Comment Type **ER** *Comment Status* **R** *pdtype*

This is the first time Data Link Layer classification if referenced in the PD section and it is not defined.

SuggestedRemedy

Add the sentence: "Data Link Layer classification is a layer 2 protocol. Details can be found in section 33.6." after the paragraph.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33** *SC* **3.1.a** *P* **34** *L* **13** # 97

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **D** *rej*

The current text may cause wrong interpretations.

The problem with the current text is the wording "..the PD will appear to the PSE as Type 1 PD until..."
Instead saying that the PD will consume up to type 1 power max power level (it is type 2 PD due to its class 4 signature)

Rational:
If a Type 2 PSE implements only type 1 layer 1 classification and it reads class 4 which is type 2 PD only, it should appear to the PSE as class 4 PD which is type 2 PD that have the potential to require up to 29.5W however it will consume up to 12.95W until layer 2 is established.

SuggestedRemedy

Change from:
"Table 33-12 specifies the electrical characteristics of Type 1 and Type 2 PDs. When a PSE exhibiting only Type 1 Physical Layer classification powers a Type 2 PD, the PD will appear to the PSE as a Type 1 PD until the PSE successfully performs Data Link Layer classification thereby identifying itself as a Type 2 PSE."

To:
"Table 33-12 specifies the electrical characteristics of Type 1 and Type 2 PDs. When a PSE exhibiting only Type 1 Physical Layer classification powers a Type 2 PD, the PD will consume max. type 1 power levels until the PSE successfully performs Data Link Layer classification thereby identifying itself as a Type 2 PSE"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is the PD section. From the PD point of view it has only discovered a Type 1 PSE.

Cl **33** *SC* **3.1a** *P* **34** *L* **10** # 210

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **A** *pdtype*

Change the following text for clarity:
"Type 2 PDs shall implement both Type 2 hardware Physical Layer classification and link layer Data Link Layer classification. This limits the maximum power a PD may expect to draw from a PSE to 29.5 W."

SuggestedRemedy

To:
"Type 2 PDs implement both Type 2 hardware Physical Layer classification and link layer Data Link Layer classification. The maximum power a PD may expect to draw from a PSE is limited to 29.5 W."

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **34** *L* **11** # 35

Patoka, Martin TI

Comment Type **E** *Comment Status* **A** *pdtype*

The wording is awkward.

SuggestedRemedy

Type 2 PDs may draw no more than 29.5W from a PSE.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **34** *L* **11** # 255

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *pdtype*

29.5W is not an accurate number for the PD based on the information to date. The maximum power available to the PD is dependent on the maximum current which is dependent on the ambient temprature of the cables.

For example, a PD that is connected to a PSE with cabling that is at an ambient temperature higher than 45C can not reliably depend on 29.5W. The 29.5W is a maximum at a point on the curve. This implicitly assumes that 802.3at will NOT support ambient temperatures that are higher than 45C on the cabling, which we have not decided yet.

We need to deal with this issue prior to setting maximums / minimums in the spec.

This comment should apply to all references of maximum power for the PD

SuggestedRemedy

Delete the 29.5W and/or explictly state that 802.3at will not support temperatures above 45C.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29 and 247

Cl **33** *SC* **3.1a** *P* **34** *L* **13** # 138

Stanford, Clay — Linear Technology

Comment Type **E** *Comment Status* **A** *pdtype*

Paragrah lacks information and is confusing.

A re-written paragraph is appended.

SuggestedRemedy

IS:
Table 33–12 specifies the electrical characteristics of Type 1 and Type 2 PDs. When a PSE exhibiting only Type 1 Physical Layer classification powers a Type 2 PD, the PD will appear to the PSE as a Type 1 PD until the PSE successfully performs link layer Data Link Layer classification thereby identifying itself as a Type 2 PSE.

SHOULD BE:
Table 33–12 specifies the electrical characteristics of Type 1 and Type 2 PDs. If a PSE does not impement Physical Layer Classficiation, or only implements Type 1 Physical Layer classification, a Type 2 PD may appear to the PSE as a Type 1 PD. If the PSE is a Type 2, Data Link Layer PSE, it may subsequently perform DLLP classification. At that time, the PSE would recognize the Type 2 PD and the PD would be alerted that a Type 2 PSE is present.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **34** *L* **13** # 36

Patoka, Martin — TI

Comment Type **E** *Comment Status* **A** *pdtype*

Sentence is awkward:
When a PSE exhibiting only Type 1 Physical Layer classification powers a Type 2 PD, the PD will appear to the PSE as a Type 1 PD until the PSE successfully performs Data Link Layer classification thereby identifying itself as a Type 2 PSE.

SuggestedRemedy

When a type 2 PSE provides Type 1 Physical Layer classification, the PD must assume a type 1 PSE until Data Link Layer classification is subsequently completed.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **34** *L* **13** # 29

Delveaux, Bill — Cisco Systems

Comment Type **E** *Comment Status* **D** *pdtype*

Lines 13-16 seem redundant.

This basically says to stay a Type 1 PD until you know you are connected to a Type 2 PSE using L2. This does not need to be said again at this point, or it can be changed to a note if the group decides to leave it. We may also want to consider the same note for the L1 case.

SuggestedRemedy

Remove lines 13-16

Proposed Response *Response Status* **O**

Section 33.3.1a to read:

PDs can be categorized as either Type 1 or Type 2.

Type 1 PDs implement Type 1 hardware Physical Layer classification. This limits the maximum power the PD may expect to draw from a PSE to Pportmax as defined in Table 33-12.

Type 2 PDs implement both Type 2 Physical Layer classification and Data Link Layer classification. This limits the maximum power a PD may expect to draw from a PSE to Pportmax as defined in Table 33-12.

Cl **33** *SC* **3.1a** *P* **34** *L* **16** # 168

Law, David — 3Com

Comment Type **T** *Comment Status* **A** *pdtype*

This text realtes to how the PD appears to the PSE.

SuggestedRemedy

Change the text '.. classification thereby identifying itself as a Type 2 PSE.' to read '.. classification thereby identifying itself as a Type 2 PD.'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **34** *L* **16** # 175

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X**

The PD section is missing the statement that Type 2 PDs will provide external notification when powered by a Type 1 PSE.

SuggestedRemedy

After this paragraph, add the sentences: "A Type 2 PD that does not successfully detect Type 2 Physical Layer classification or Data Link Layer classification must conform to Type 1 PD power restrictions and shall provide the user with external notification that it is underpowered. The external notification is left to the implementor. Examples include flashing an LED or providing feedback via a management interface."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.1a** *P* **34** *L* **7** # 34

Patoka, Martin TI

Comment Type **E** *Comment Status* **A** *pdtype*

The context of the second sentence is odd.

SuggestedRemedy

Type 1 PDs may draw more than 12.95W from a PSE.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **48** *L* **7** # 209

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **A** *pdtype*

Change the following text for clarity:
"Type 1 PDs may optionally implement Type 1 hardware Physical Layer classification. This limits the maximum power the PD may expect to draw from a PSE to 12.95 W."

SuggestedRemedy

To:
"Type 1 PDs expect to draw from a PSE to 12.95 W and do not have Layer 2 classification. They may optionally implement Type 1 hardware Physical Layer classification."

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.2** *P* **36** *L* **6** # 189

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **A** *t33-12a*

Figure 33-12a needs to be redrawn to meet IEEE state diagram requirements.

SuggestedRemedy

Request the L1 ad hoc to create the state diagram.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See Editor's report.

Cl **33** *SC* **3.2.3** *P* **36** *L* **22** # 204

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **A** *t33-12a*

In the 8/29/07 Classification Ad Hoc meeting, it was generally agreed that a note should be added to explain Class Event 3 in the PD Physical Layer Classification State Diagram.

SuggestedRemedy

Add note below state digram or in text:

"Class Event 3 creates a defined behavior for a Type 2 PD which is brought into the classification range repeatedly.

In a typical power-on event, the PI voltage will transition from Mark Event range directly through Classification range to Power On. Class Event 3 durations less than Tclass may not allow a Type 2 PD to respond with a Classification current. There is no minimum Class Event 3 time duration and for Class Event 3 times less than Tclass, there is no requirement for a Type 2 PD to respond with a defined current."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Covered by motion on Sept 11, 2007.

Cl **33** *SC* **3.2.3** *P* **36** *L* **3** # 37

Patoka, Martin TI

Comment Type **E** *Comment Status* **R** *t33-12a*

Figure 33-12a.
Note on top middle "Transition via layer 2 ..." This is not referred to as "data link layer"

SuggestedRemedy

Change text to current terminology.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33** *SC* **3.3** *P* **37** *L* **11** # 62

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

Voltage and current offsett in table 33-8 are ambiguous.

SuggestedRemedy

Move a copy of figure 33C-20 to and annotate to show Ioffset. The value of Ioffset is not very restrictive since it is typically negative as shown in the figure. The voltage and current offset need to be defined as being related to the projection of the (two point) line-fit between 2.7V and 10.1V.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4** *P* **38** *L* **1** # 237

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

This is analogous to my comment on th PSE section.

This section is very confusing. We dive into Physical Layer classification and then do Data-Link Layer Classification. I would suggest that we make 33.3.4 a general introduction to classification. We then take 33.3.4 and 33.3.4a and make them subclauses of this new geenral section.

For the content of the general section on classification, I will submit a seperate comment (my previous comment in the .csv file).

SuggestedRemedy

I would suggest that we make 33.3.4 a general introduction to classification. We then take 33.3.4 and 33.3.4a and make them subclauses of this new geenral section.

Proposed Response *Response Status* **W**

see 51, 238

Cl **33** *SC* **3.4** *P* **38** *L* **1** # 238

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X**

Related to my previous comment on restructuiring this section, I would suggest the following text

SuggestedRemedy

Rename title of section 33.3.4 to PD Classifications

AND

insert the following text in the general section:

"A PD may be classified by the PSE based on Physical Layer classification information, Data Link classification or a combination of both provided
by the PD. The method of classification will depend on the Type of the PD and the Type of the PSE.

Type 1 PDs shall implement a Physical Layer classification as described below.

Type 2 PDs shall implement both a Physical Layer classification and a Data Link Classification as described below"

AND

Retain and restructure current text per my previous comment into sub-clauses

Proposed Response *Response Status* **W**

see 51, 237

Cl **33** *SC* **3.4** *P* **38** *L* **1** # 51

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X**

The presence of LL classification is harder to understand with the transfer of the requirement to 33.6.

SuggestedRemedy

Change title of 33.3.4 to: PD classifications.

Add sentence to line 5:

A type 2 PD that receives a type 1 physical layer classification, or partial type 2 physical layer classification shall behave as a type 0 PD.

Add paragraph at line 6 similar to:

A type 2 PD must respond to type 2 data link layer classification messsages as defined in section 33.6.

Proposed Response *Response Status* **W**

see 238, 237

Cl **33** *SC* **3.4.1** *P* **38** *L* **11** # 177

Jones, Chad — Cisco

Comment Type **T** *Comment Status* **X**

The statements "However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3." and "Type 2 PDs shall return a Class 4 classification signature in accordance with the maximum power draw..." (line 49) forces Type 2 PDs to only draw more than 12.95W. Why is it illegal for me to make a Type 2 PD that is Class 2 then uses LLDP to further refine the power consumption, say down to 5W? If I am forced to advertise Class 4 there will be situations where my PD could be powered by a PSE but won't be because the PSE has more than 7.0W but less than 15.4W left in reserve.

SuggestedRemedy

The text in 33.3.4.1 and 33.3.4.2 needs reworked to reflect this operating condition.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **23** # 12

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

The 'Usage' column in Table 33-10 seems unnecessary. Normative text already forces Type 1 PDs to use Class 0-3, and Type 2 PDs to use Class 4.

SuggestedRemedy

Remove 'Usage' column from Table 33-10.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **24** # 190

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

Table 33-10 is not clear. Why is a range of maximum stated? Does a class 2 PD need to draw at least 3.84 W?

A type 2 PD should be able to produce all classes.

SuggestedRemedy

Only state the maximum class power allowed. For example, a class 2 PD can draw up to 6.49 W.

Allow a type-2 PD to request the power it needs. That is, if it needs class-2 power levels it can do this directly using a type-1 PD Physical layer classification mechanism.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **39** # 38

Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

"A Class 4 signature cannot be provided
by a compliant Type 1 PD."

This might be construed to talk about the capability of an individual unit.

SuggestedRemedy

A compliant Type 1 PD shall not provide a class 4 signature.

Proposed Response *Response Status* **W**

can't put a shall in a note

see 234

Cl **33** *SC* **3.4.1** *P* **38** *L* **39** # 234

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

Is the intention of the note here to be cannot or shall not? There is nothing preventing someone from building a PD that is not compatile with the draft, hence cannot is not accurate.

SuggestedRemedy

Suggest changing cannot to shall not

Proposed Response *Response Status* **W**

see 38

Cl **33** *SC* **3.4.1** *P* **38** *L* **9** # 174

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X**

The text makes no statement about Type 1 PDs using Data Link Layer classification. For sure, manufacturers will do this.

SuggestedRemedy

Add the sentence: "A Type 1 PD may optionally choose to implement Data Link Layer classification."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **38** *L* **47** # 52

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X**

The concept of physical layer classification is difficult to general readers to understand. This compounded by the 2 event technique.

SuggestedRemedy

A figure such as containned in stanford_1_0707 page 12 should be incorporated into this section to clarify the whole subject. It is important to put it in the normative section to support the text.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **38** *L* **49** # 13

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

Type 2 PDs don't necessarily have to exhibit >12.95W power consumption. That makes the phrase 'in accordance with the maximum power draw as specified by Table 33-10' rather misleading.

SuggestedRemedy

Delete the phrase.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **39** *L* **14** # 147

Law, David 3Com

Comment Type **T** *Comment Status* **X**

There are actually two types of classification. [1] A PSE's classification of a PD. [2] A PD's classification of the PSE. The text seems to call all this PD hardware classification and while it is that mechanism that is used by the PD to classify the PSE I think we need to make that distinction clear in the text. Does the text 'Once a PD has been powered by a Type 2 PSE' imply that the PD has to detect that the current sourced by the PSE has exceeded the maximum for a Type 1 PSE - although even that doesn't guarantee it is Type 2 PSE power. The only real test that is available is that a Type 2 hardware classification or link layer classification has completed.

SuggestedRemedy

Perfom the following change: [a] Delete the first sentence of the third paragraph of subclause 33.3.4.2. Text currently reads 'Until successful Type 2 hardware classification or link layer classification has completed, a Type 2 PD's PSE Type state variable is set to Type 1.'. [b] Delete subclause 33.3.4.2.2. [c] Insert new subclause 33.3.4a, renumber as necessary. The content of this new subclause should cover the areas in [a] and [b] as well as clarify the text.

33.3.4a PSE type classifiction

A Type 2 PD shall classify the PSE Type as either Type 1 or Type 2. The default value of PSE Type shall be Type 1. After a successful Type 2 hardware classification or link layer classification has completed the PSE Type shall be set to Type 2. The PD shall reset the PSE Type to Type 1 when the voltage at the PI is less than or equal to VReset_lo max. Once a Type 2 hardware classification or link layer classification has completed a Type 2 PD shall reset the PSE Type to Type 1 if the voltage at the PI is less than or equal to VReset_hi min.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **39** *L* **15** # 235

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

The following sentence adds no value as the prior states the required, which is that these are externally observable parameters

SuggestedRemedy

Delete

"Equivalent implementations that present the same external behavior are allowed."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **39** *L* **19** # 236

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

The following sentence is very confusing as the referenced table has a PD type not PSE type:

"A Type 2 PD shall conform to the electrical requirements as defined by Table 33–12 of the Type defined in its PSE Type state variable."

SuggestedRemedy

Either clarify the sentence, change the reference, clarify the table titles or delte it all together.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **39** *L* **28** # 63

Patoka, Martin TI

Comment Type **T** *Comment Status* **A** *t33-11a*

Table 33-11a, item 1a:

The mark voltage event is somewhat misleading due to the first quadrant nature of the PSE, the switched loading of the PD, and the presence of capacitance on the link. This event is actually initiated by the PSE dropping the voltage below 15.5V / 14.5V.

SuggestedRemedy

Suggest adding a note in the Additional Information column something like: PD threshold between 14.5V and 10V. Otherwise this could be added to 33.3.4.2.1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolved by 126

Cl **33** *SC* **3.4.2** *P* **39** *L* **28** # 126

Beia, Christian STMicroelectronics

Comment Type **T** *Comment Status* **A** *t33-11a*

In table 33-11a the Mark event Voltage is defined between 6.9V and 10V, while in figure 33-12a (pg 36) the Mark threshold is indicated between 10V and 14.5V. Since the state change is defined by the mark threshold, I propose to add a row in Table 33-11a for the parameter Mark Threshold Vthm, with range between 10V and 14.5V.

SuggestedRemedy

Add parameter Mark Threshold in Table 33-11a. Symbol Vthm, Units V, Min 10, Max 14.5.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

replace "1a Mark Event Voltage VMark V 6.9 10"

with "1a Mark Event Voltage VMark V 6.9 "

add "1x Mark Event Threshold Vmark_th V 10 14.5"

add informative text "PD must draw Iclass above Vmark_th and Imark below Vmark_th."

Cl **33** *SC* **3.4.2** *P* **39** *L* **30** # 127

Beia, Christian STMicroelectronics

Comment Type **T** *Comment Status* **A** *t33-11a*

The behavior of the PD in the voltage range between 10V and 14.5V is undefined. In this range the PD should sink enough current to discharge the port voltage, and should not exceed the maximum Class 4 current. I propose to add a row in Table 33-11a to define the Mark Threshold Current. My understanding is that it should be between 0.25mA (minimum Mark current) and 44mA (max Class current).
I propose also to add a paragraph in section 33.3.4.2 to explain the link between the Mark Threshold current and the Mark threshold voltage range.

SuggestedRemedy

Add parameter Mark Threshold Current in table 33-11a, Symbol Ithm, Units mA, Min 0.25, Max 44, Additional Information See 33.3.4.2.x
Add paragraph 33.3.4.2.x with title Mark Threshold behavior, with text: A Type 2 PD shall not exceed the Ithr current limits when voltage at the PI enters the Mark Threshold voltage specification.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See 126.

Cl **33** *SC* **3.4.2** *P* **39** *L* **31** # 139

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **A** *t33-11a*

During the July 2007 meeting (http://grouper.ieee.org/groups/802/3/at/public/jul07/stanford_1_0707.pdf), I detailed how a spike which may occur during cable mating can confuse a Type 2 PD into thinking a Type 1 PSE is a Type 2 PSE. This was discussed further in the 7/29/07 Classification Ad Hoc meeting and it is generally agreed that the problem can be solved by insuring the PD does not present a valid detection signature during the Mark event. The following implemnets that change:

SuggestedRemedy

Add to table 33-11a-Type 2

1c Mark Event Signature blank blank blank blank "Type 2 PD to present non-valid PD detection signature per Table 33-9"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Already in state diagram. Editor to add text in appropriate spot.

Cl **33** *SC* **3.4.2** *P* **39** *L* **32** # 65

Patoka, Martin TI

Comment Type **T** *Comment Status* **A** *t33-11a*

Table 33-11a, Item 2a

Reset range is 2.8V max, however this is the PSE limit. In order to work properly, the PD must assure reset above the minimum PSE reset range (table 33-4a).

SuggestedRemedy

Range should be 2.8V or 2.9V min to 6.8V or 6.9V max. I woul dshoose 2.9V to 6.8V.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See 128.

Cl **33** *SC* **3.4.2** *P* **39** *L* **32** # 128

Beia, Christian STMicroelectronics

Comment Type **T** *Comment Status* **A** *t33-11a*

In table 33-11a the item Classification Low Reset Range is defined 2.8V max. In figure 33_12a (pg 36) the Reset Threshold is indicated between 2.8V and 6.9V. This double definition can create confusion (Where should I put my reset? Above or below 2.8V?) Since my understanding is that the reset should be between 2.8V and 6.9V, I propose to change the Table 33_11a, indicating Classification Low Reset Voltage Range 2.8V min, 6.9V max.

SuggestedRemedy

Change Min and Max values in Table 33-11a, Parameter Classification Low Reset Voltage Range, with the following values: Min 2.8, Max 6.9.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

change:"2a Classification Low Reset Voltage Range VReset_lo V 2.8 See 33.3.4.2.2"

to: "2a Classification Reset Threshold VReset V 2.8 6.9 See 33.3.4.2.2"

Cl **33** *SC* **3.4.2** *P* **39** *L* **34** # 140

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **A** *t33-11a*

In the 8/29/07 Classification Ad Hoc meeting it was generally agreed that a Type 2 PD should not have a Classification High Reset Voltage Range and that this requirement should be removed from draft.

SuggestedRemedy

Table 33-11a-Type 2

Remove entire entry:

2b Classification High Reset Voltage Range Vreset_hi V 30

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **3.4.2** *P* **39** *L* **35** # 66

Patoka, Martin TI

Comment Type **T** *Comment Status* **A** *t33-11a*

Table 33-11a. Item 2b.
Classification high reset voltage range. There is a potential that noise, short dropouts, and transients could cause Vpi to dropout momentarily. This is not seen by the class circuit due to the bulk capacitance. Once in the powered state, the PSE must return to the power off phase before repowering the PD. Since there is no reclassification, the PD should sample this only once at startup.

SuggestedRemedy

Remove this entry.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See 140

Cl **33** *SC* **3.4.2** *P* **39** *L* **39** # 196

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

A type-2 PD should be able to request the power it needs.
A type-2 PD should be able to use type-1 physical layer classification.

SuggestedRemedy

Replace the existing sentence with:
A Type 2 PD shall return the same class signature irrespective of the number of classification voltage probes performed by the PSE.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2.1** *P* **39** *L* **45** # 64

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

The classification adhoc recommends that the PD have an invalid signature while in the Mark state.

SuggestedRemedy

Add statement:

The PD shall have an invalid detection signature while in the Mark range.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2.2** *P* **39** *L* **51** # 99

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X**

The state diagram of the PD in 33-12a doesn't include reset high range as per the last updates however the text in 33.3.4.2.2 and item 2b in table 33-11a still contains reset high definitions.

Reset high is not required since when PD is disconnected for time duration longer then 300-400msec the PSE disconnects the power from the port and eventually the port voltage enters Vreset low range so Vreset high range is redundant and requires a bit more circuit complexity in the PD.

SuggestedRemedy

1. Delete item 2b from table 33-11a.
2. Change lines 48-52 from:
"The PD shall reset its PSE Type state variable to Type 1 when the voltage at the PI is less than or equal to VReset_lo max as defined in Table 33-11a. Once a PD has been powered by a Type 2 PSE, it shall reset its PSE Type state variable to Type 1 if the voltage at the PI is less than or equal to VReset_hi min as defined in Table 33-11a."

To:

"The PD shall reset its PSE Type state variable to Type 1 when the voltage at the PI is less than or equal to VReset_lo max as defined in Table 33-11a. Once a PD has been powered by a Type 2 PSE, it shall reset its PSE Type state variable to Type 1 if the voltage at the PI is less than or equal to VReset_low as defined in Table 33-11a."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4a** *P* **40** *L* **1** # 256

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

We still need to have a section on Link Layer here. I believe the material in 33.6 is intended to complement 33.3.4a (or whichever way we end up renumbering it) even if it is a reference to a later section. Otherwise its confusing

SuggestedRemedy

See Comment. We need to have a control section in addition to the management section.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **42** *L* **22** # 53

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X** *t33-12*

Table 33-12 item 3: see also 33.3.5.3 p43 line 46.

The term inrush is not defined.

SuggestedRemedy

Add statement similar to the following to 33.3.5.3:

Inrush current is drawn during the startup period beginning with the application of input compliant with table 33-12 Vport requirements, and ending when Cport is charged to within 99% of its final value. This period must be less than Tlim min per table 33-5.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **42** *L* **24** # 191

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *t33-12*

The peak operating current specified in this section is Pport_max/Vport. It is not clear that Pport_max is the power the PD is classified to because the Iport max of table item 4 contradicts this. For example, a class 3 PD can draw 6.49 W and with a 36 V input will draw 6.49/36 = 180 mA. The value in item 4 states 210 mA.

Also see a related comment on this same parameter. It is also not clear which Iport is being referenced-table 33-12 has items 4 and 5 with the same name.

SuggestedRemedy

The task force needs to review these values and state what ensures interoperability.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **42** *L* **32** # 274

NoName

Comment Type **E** *Comment Status* **X** *t33-12*

CommenterName: Ostrovski Shlomo
CommenterEmail: shlomo@advice.ci.il
CommenterPhone: +972-39000-900
CommenterCo: Advice LTD

Table 33-12 item 4:

If the max. average current of the cable is I average and the project objective is to have 30W minimum at the PD input or any P_port_average that will be decide, then the standard should allow some ac current so the peak current may be higher then the average in order to accommodate with PD circuits components accuracies.

This concept was used in 802.3af without additional cost due to the fact that the specification at the PD side required that the average current and the RMS current will be kept within the same number therefore no additional RMS or Average power beyond the max. permitted average cable current so no additional cost to support this feature which is a standard approach in power supply design.

SuggestedRemedy

Table 33-12 item 4: Peak operating current at class 4 for type 2 PD: Ipeak = at least 15% above max. cable average current. 0.823A minimum.

Proposed Response *Response Status* **W**

see 122, identical comment

Cl **33** *SC* **3.5** *P* **42** *L* **32** # 277

NoName

Comment Type **E** *Comment Status* **X** *t33-12*

CommenterName: Levy Avinoam
CommenterEmail avinoam@solarpower.co.il
CommenterPhone: +972-9-8654904
CommenterCo: SolarPower LTD

In 802.3af the standard allowed the PD to have some current variation on the top of the max. DC current

in order to have robust system design and efficiently utilizing the maximum permitted DC current.

For that matter it was allowed to the PD load to have peak current higher than the average current by ~14%

for limited time and duty cycle in addition to the requirement that the PD shall not consume more then the max permitted current in terms of DC and RMS values.

In this way the specification guarantees that no additional burden will be on the PSE power supply or the PSE port driver.

If the permitted peak current will be lower then the above margin it will effectively reduce the usable max. cable current

Due to the fact that circuit accuracy and application dynamic load variation will drive users to exclude applications that now

became marginal hence the effective usable power will be lower then 29.5W.

Due to the above arguments it is suggested to use the same 802.3 specification for PD input current parameters and change only the numbers for the max. cable DC and RMS current i.e. 720mA and ~820mA for the peak current.

SuggestedRemedy

Set item 4 to be 820mA up to 50msec max. and 5% duty cycle max.

Proposed Response *Response Status* **W**

see 122, identical comment

Cl **33** *SC* **3.5** *P* **42** *L* **32** # 112

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *t33-12*

Draft0.9:
Table 33-12 item 4:
Project objective was to deliver 30W to the PD.
In order to achieve this objective we set a 720mA max. DC current.
In order to utilize the full power capability derived from 720mA or any average current we need to allow some ac wave form to coexist on top of the DC level in order to handle the following input parameters:
a) Application circuit components accuracy limitation
b) PD DC/DC converter components accuracy
c) Application load variations

This concept was succesfully used in 802.3af without additional complexity or cost due to the fact that the specification requires also from the PD vendor to keep the RMS and the DC value not to excceed the same number i.e. 350mA and in our case is 720mA. Threfore there is no additional power consumption beyond the max. power specifyied.

Regarding the issue of supporting PSE current transient due to dv/dt simultaneously with PD peak current=823mA when PSE is using constant current limit near Icut_max so net charging current is zero, the following solution is suggested:
When using constant current limit the PSE vendor will set ILIM_MIN = PSE'S icut_max + Margin.
The margin is the current required to charge Cpd (<50mA).

Other alternative would be to minimize th erequirements from the standard it is a PSE issue and not system issue hence no interoperability risk that requires the standard to adress both PSE and PD.
Rational:
1. It is enugh to define that PSE is required to support current transients due to PSE dv/dt up to 7V at a slew rate of TBD. At this point it is depened only at the PSE how to implement this support. The PD is not a player that need to be defined. It is already defined by Cpd=180uF.

If PD is usig up to 180uF and PSE dv/dt is limited to 7V then the peak current and its duration are both function of PSE implementation. If PD input capacitor is > 180uF then the PD is responsibble to limit the current at its input to Icut_max.

2. If PSE choose to implement energy based current limit, then it will work within the 2A peak and 3msec time as suggested by the Vport_ad hoc.

3. If PSE choose to use constant current limit, it will choose the correct ILIM and TLIM_min pairs to maintain th eport at ON state for TLIM_MIN.

4. There is no issue with PD application load transient current due to the fact that per the concept of type 1 PD which is suggested for type 2 PD as well, the max peak current at the PD is Icut_max and it is limited to 50msec, 5% duty cycle max.
In addition, in previous commnet, it was shown that in any case the system will get to 820mA for 250usec when PSE voltage is droped by 7.6% (46.2V) per table 33-5 item 2a so in any case PD may work at 820mA and PSE shall support it by setting minimum ILIM=820mA + Margin.

5. There is no added cost as was proven in 802.3af:
5.1 The max. average current is always 720mA (350mA in 802.3af)
5.2 The max. RMS current is 720mA rms. (350mA in 802.3af)
Hence no additional resistive loss in the system.
5.3 As aresult the total average power is always 29.5W max. (12.95W in 802.3af)
5.3.1 The specification is explicetly defines that the total PD input power shall not exceed Pport_max 12.95(/29.5W) average over 1sec.

SuggestedRemedy

Itme 4: Peak operating current at class 4 for type 2 PD:

Ipeak = 0.72A*0.4/0.35 = 0.823A. (Same Icut/Iport ratio as in 802.3af)
Number may be rounded to 820mA.

Proposed Response *Response Status* **W**

see 270, 274, 277, 278

Cl **33** *SC* **3.5** *P* **42** *L* **32** # 278

NoName

Comment Type **E** *Comment Status* **X** *t33-12*

CommenterName: Asher Bitton
CommenterEmail: asherb@advice.co.il
CommenterPhone: +972-39000-900
CommenterCo: Advice LTD

Table 33-12 item 4:

The PSE is allowed to have low transient voltage down to 46V.

In this case the current at the PD input will be ~820mA.

Therefore the peak current is more then the average current of 720mA for limited time ~250uSec.

The current 802.3 concept allow ~15% current change above the average for 50msec max and for 5% maximum duty so the above transient is well covered with this concept.

In addition, there are many applications that required peak current for limited duration and most of the time the current is much less of the average current.

This physical behavior allows low cost implementations in term of small capacitance at power supply input/outputs while keeping the same average power and also the same losses dissipated in the power supply or even lower. The current 802.3 specification support and allow this feature i.e. keeping the same power and its cost by limiting the PD average and RMS current to the same number i.e. 350mA average max and 350mA RMS max.

There is no technical reason for changing a working concept especially if it creates more problems then solutions.

The Vport ad hoc has shown a dv/dt scenario caused by the PSE which in return creates positive transient current which may happen simultaneously with PD load current peak. These low probability scenario may easily treated by the PSE based on "implementation specific" solution as proposed by the ad hoc members.

All of the proposed solutions for this issue do not increase the Burdon on the PSE port due to the fact that the worst case in terms of power loss is during startup mode.

SuggestedRemedy

1. Use the same 802.3af concept in Type 2 PD for handling the DC, Peak and RMS current.

1.1 Ipek=820mA for 50msec max. 5% duty cycle max.

Proposed Response *Response Status* **W**

see 122, identical comment

Cl **33** *SC* **3.5** *P* **42** *L* **32** # 270

NoName

Comment Type **TR** *Comment Status* **X** *t33-12*

CommenterName: Daniel Feldman
CommenterEmail: dfeldman@microsemi.com
CommenterPhone: 14084062639
CommenterCo: Microsemi Corp.
Comment:
Table 33-12 item 4:

One of the project's objective was to deliver 30W to the Powered Device.

This could be achieve with a 720mA max. DC current (which brings power to 29.52W)

In order to utilize the full power capability derived from 720mA or any average current we need to allow some ac wave form to coexist on top of the DC level in order to handle the following input parameters:

a) PD DC/DC converter components accuracy

b) Application circuit components accuracy limitation

c) Application load variations

This concept was successfully used in the IEEE802.3af project without additional complexity or cost due to the fact that the specification requires also from the PD vendor to keep the RMS and the DC value not to exceed the same number i.e. 350mA (and in our case 720mA). Therefore there is no additional power consumption beyond the maximum power specified.

On the issue of supporting PSE current transient due to dv/dt simultaneously with PD peak current=823mA when PSE is using constant current limit near Icut_max so net charging current is zero, the following solution is suggested:

When using constant current limit the PSE vendor will set ILIM_MIN = PSE'S icut_max + Margin.

The margin is the current required to charge Cpd (<50mA).

Another alternative would be to minimize the requirements from the standard it is a PSE issue and not system issue hence no interoperability risk that requires the standard to address both PSE and PD.

Rationale:

1. It is enough to define that PSE is required to support current transients due to PSE dv/dt up to 7V at a slew rate of TBD. At this point it depends only on the PSE how to implement this support. The PD does not need to be defined (it is already defined by Cpd=180uF).

If PD is using up to 180uF and PSE dv/dt is limited to 7V then the peak current and its duration are both a function of PSE implementation. If PD input capacitor is > 180uF then the PD is responsible to limit the current at its input to Icut_max.

2. If the PSE chooses to implement energy based current limit, then it will work within the 2A peak and 3msec time as suggested by the Vport_ad hoc.

3. If the PSE chooses to use constant current limit, it will choose the correct ILIM and TLIM_min pairs to maintain the port at ON state for TLIM_MIN.

4. There is no issue with PD application load transient current due to the fact that per the concept of type 1 PD which is suggested for type 2 PD as well, the max peak current at the PD is Icut_max and it is limited to 50msec, 5% duty cycle max.

In addition, in a previous comment, it was shown that in any case the system will get to 820mA for 250usec when PSE voltage is dropped by 7.6%
(46.2V) per table 33-5 item 2a so in any case PD may work at 820mA and PSE shall support it by setting minimum ILIM=820mA + Margin.

5. There is no added cost as was proven in 802.3af:

5.1 The max. average current is always 720mA (350mA in 802.3af)

5.2 The max. RMS current is 720mA rms. (350mA in 802.3af)

Hence no additional resistive loss in the system.

5.3 As a result the total average power is always 29.5W max. (12.95W in 802.3af)

5.3.1 The specification is explicitly defines that the total PD input power shall not exceed Pport_max 12.95(/29.5W) average over 1sec.

SuggestedRemedy

Itme 4: Peak operating current at class 4 for type 2 PD:

Ipeak = 0.72A*0.4/0.35 = 0.823A. (Same Icut/Iport ratio as in 802.3af)

Number may be rounded to 820mA.

Proposed Response *Response Status* **W**

see 122, identical comment

Cl **33** *SC* **3.5** *P* **42** *L* **39** # 39

Patoka, Martin TI

Comment Type **E** *Comment Status* **X** *t33-12*

Table 33-12 item 5: Maximum current

720mA * 41V = 29.52
520mA * 57V = 29.64

SuggestedRemedy

Change 520 to 517.5mA.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **43** *L* **12** # 67

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *t33-12*

Table 33-12 item 10: Backfeed voltage
see also 33.3.5.10 P45 line 24.

The maximum allowed bridge reverse current is 2.8V/100K = 28uA. This requirement is too stringent and appears to prevent the use of schotty diodes. Given that we are doubling the current, efficiency and component temperature rise are adversely impacted. THere is no reason to limit the implementation of a PD to preclude the use of Schottky diodes.

SuggestedRemedy

Decrease the resistance to 9.09k. this was selected based on a B2100 diode 2A, 100V schottky at 125C reverse leakage at 60V (.3ma).

Proposed Response *Response Status* **W**

do you mean 90.9K?

Cl **33** *SC* **3.5.1** *P* **43** *L* **19** # 54

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X**

"The PD shall turn off at a voltage less than VPort minimum and greater than or equal to VOff."

"The specification for VPort in Table 33–12 is for the input voltage range after startup, and it includes loss in the cabling plant."

The terms "off" and "startup" are not defined.

SuggestedRemedy

after the first sentence add:

"Startup begins upon application of Vport per table 33-12 and concludes at the end of the inrush period per 33.3.5.3."

this relies on the additions to the inrush paragraph.
change the sentences to:

"The PD shall not draw more current than its Class current per table 33-11 at voltages less than Vport min."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **43** *L* **23** # 192

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

Some people are confused how to calculate duty cycle.

SuggestedRemedy

In a note state that duty cycle shall be calculated using a sliding window with a 1 second width around any level above Pport_max/Vport.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **43** *L* **24** # 258

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

Why are we discussing the resistance of the cabling here? I think we should either refer to the worst case setup using the cabling types or find a way to test the PD at its input

SuggestedRemedy

see comment

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **43** *L* **25** # 144

Bennett, Ken — Sifos Technologies, In

Comment Type **T** *Comment Status* **X**

The measurements of Average Power, which include series resistors in the Annex 33C, are existing recommendations. The Annex states that other test circuits are possible, so long as compliance with Clause 33 are adequately demonstrated. Using the words "Shall be Measured" in Clause 33.3.5.2 changes this recommendation to a requirement for existing measurement techniques, which may already use adequately demonstrated alternatives.

SuggestedRemedy

Remove the two sentences containing the words "shall be measured".

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **43** *L* **26** # 146

Law, David — 3Com

Comment Type **ER** *Comment Status* **X**

Please follow the correct format for equations define in the IEEE Style guide [http://standards.ieee.org/guides/style/2007_Style_Manual.pdf#Page=29]. Additional formatting information can be found at [http://www.ieee802.org/3/tools/editorial/requirements/scc14.html].

In addition for these specific equations it is not clear that the measurement using 20 Ohms for type 1 and 12.5 Ohms for Type 2 are mandatory. If they are, as I suspect they are, they should be shall statements.

SuggestedRemedy

This formatting needs to be carried on the entire draft or there is the possibility that SCC14 may try to force these changes during sponsor ballot and RevCom submittal - SCC14 is a mandatory coordination [http://standards.ieee.org/faqs/coor.html].

In this particular case the equation should be changed as follows:

[1] The text 'where:' followed by a list of variables with their definition should be provided.

[2] The letter symbols for physical quantities, mathematical variables, indices and general functions (as opposed to mathematical functions), are always printed in italic. In this case P, V and I should be italic. Subscripts and superscripts follow the same rules. Symbols for physical quantities, mathematical variables, indices and general functions are printed in italic. Therefore in this case 'Port' should be in upright font as it is not a symbol for a variable.

To address the measurement specification issue the resistances should be included in shall statements. This subclause would therefore read:

The specification for PPort in Table 33-12 shall apply for the input power averaged over 1 second. For a Type 1 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 20 W in series. For a Type 2 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 12.5 W in series. PPort is defined as:

PPort = VPort x IPort

where

PPort is the input average power
VPort is the input voltage
IPort is the input current, either DC or RMS

See the file P802p3at_sub_33p3p5p2.FM supplied with comment file for full formatting example.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **43** *L* **26** # 176

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X**

The statement "For a Type 2 PD PPort shall be measured when the PD is fed by 44 V to 57 V with..." has a typo in the voltage. The struck through text below this sentence shows that the 44V is supposed to be a 50V.

SuggestedRemedy

Change the 44V to 50V.

Proposed Response *Response Status* **W**

see 141, 199

Cl **33** *SC* **3.5.2** *P* **43** *L* **26** # 199

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

Fix the typo.

SuggestedRemedy

Replace "44 V to 57 V" with "50 V to 57 V." Consider placing all numerical values in one table and referring to them using a variable. This would ensure that numerical values appears in only one place in this specification.

Proposed Response *Response Status* **W**

see 176, 141

Cl **33** *SC* **3.5.2** *P* **43** *L* **26** # 141

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **X**

Error in Type 2 PSE operating voltages.

Says 44-57V
Should say 50-57V

SuggestedRemedy

IS:
For a Type 2 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 12.5ohms in series.

SHOULD BE:
For a Type 2 PD PPort shall be measured when the PD is fed by 50 V to 57 V with 12.5ohms in series.

Proposed Response *Response Status* **W**

CE Note: comment type was blank, set to T.

See 176, 199

Cl **33** *SC* **3.5.3** *P* **43** *L* **39** # 68

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

In order to have the inrush current agree with the Vport specification, the PD should not startup at voltages less than Vport min. Otherwise inrush current may be drawh at voltages in the detection and classification ranges. Figure 33C-1 and startup dv/dt 33C.1.8, as well as many other figures imply that the PD does not draw current at less than 33V. Since 33.2.8.5 does not require the PSE to provide ANY current at 0V out, figure 33C-1 can best be described as a test of the foldback characteristic. That is, a capacitor at 0V applied to the PSE output may never charge - and is not required to do so. Requiring PSEs to supply inrush current into a short is potentiually a burdensome cost adder to the PSE. This then leads to the ability to allow the PSE a fast turn-off into a short.

SuggestedRemedy

Add the following sentence:

"PDs shall not draw inrush current at voltages less than Vport min."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **43** *L* **4152** # 41

Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

-2005 revision used units of mA throughout. The new equations are OK, but inconsistent.

SuggestedRemedy

Add units of A(mperes) to the variable description

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **43** *L* **46** # 184

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

The value of Iport_max created by the formula-using PD Pport_max-does not match the value provided in table 33-12. For example, class 0 PD power is 12.95 W maximum and 12.95W/44V = 294 mA, not the 400 mA shown in table 33-12, item 4.

SuggestedRemedy

The PD formula provides approximately the correct answers when the PSE Pport_max values are scaled by 400/350 for the system classified power.

Table 33-12 values should match values created by the formula-rounding appears to have been used.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **43** *L* **46** # 40

Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

"At any operating condition the peak current shall not exceed PPort max/VPort for more than 50ms max and"

Given the Vport adhoc work, this shouls be clarified that this is true if V(pse) is static.

SuggestedRemedy

change to:
"At any static link supply voltage, and PD operating condition the peak current shall not exceed PPort max/VPort for more than 50ms max and"

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **44** *L* **7** # 86

Darshan, Yair Microsemi Corporation

Comment Type **E** *Comment Status* **X**

Iport_ac is the RMS value of the AC comonent of the input current.

SuggestedRemedy

Change from :
"is the AC component of the input current"

to:

"is the RMS value of the AC component of the input current"

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4A** *P* **44** *L* **31** # 142

Stanford, Clay Linear Technology

Comment Type **E** *Comment Status* **X**

Draft has added a PD transient current requirement.

Text needs to clarify that transient is with static PI voltage.

SuggestedRemedy

IS:
When the input voltage at the PI is in the range defined by Table 33–12 item 1, the transient current draw by the PD shall not exceed 15 mA/ìs in either polarity.

SHOULD BE:
When the input voltage at the PI is static and in the range defined by Table 33–12 item 1, the transient current draw by the PD shall not exceed 15 mA/ìs in either polarity.

Proposed Response *Response Status* **W**

CE Note: comment type was blank, set to E by default.

Cl **33** *SC* **3.5.7** *P* **45** *L* **8** # 171

Jones, Chad Cisco

Comment Type **ER** *Comment Status* **X**

This paragraph is redundant with 33.3.5.1 and these are redundant shalls.

SuggestedRemedy

Either delete the paragraph under 33.3.5.1 or move the last sentence of 33.3.5.7 to 33.3.5.1 and delete 33.3.5.7.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.6** *P* **45** *L* **41** # 14

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

Items (c) and (d) do not provide any new information, and are really just repetition of items (a) and (b).

SuggestedRemedy

Strike items (c) and (d) and replace with the following statement:

A PD that does not maintain the MPS components a) and b) above may have its power removed within the limits of TMPDO as specified in Table 33-5.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.6.1** *P* **46** *L* **13** # 15

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X**

The itemized list is generally confusing. The whole point is that a PD with >180uF input capacitance may have difficulty meeting the DC MPS during a voltage transient.

SuggestedRemedy

Replace with a general CAUTION statement:

CAUTION--A PD with CPort > 180uF may not be able to meet the IPort specification in Table 33-13 during the maximum allowable port voltage droop (i.e. 57V to 44V in series with 20 ohms for a Type 1 PSE and 57V to 50V in series with 12.5 ohms for a Type 2 PSE). Such a PD should increase its IPort min or make other such provisions to ensure meeting the DC maintain power signature.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.6.1** *P* **46** *L* **15** # 221

Diab, Wael Broadcom

Comment Type **E** *Comment Status* **X**

The text may be confusing, I would suggest writing out the entire range for both Type 1 and Type 2

SuggestedRemedy

Change

"when the PD input voltage is dropped from 57 V to 44 V (for a Type 1) or to 50 V (for a Type 2)"

to

"when the PD input voltage is dropped from 57 V to 44 V for a Type 1 or 57V to 50 V for a Type 2"

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.3** *P* **48** *L* **23** # 18

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Equations on lines 23, 27, 33 not set in accordance with 2007 style manual.

SuggestedRemedy

Re-set equations to meet 2007 style manual guidelines.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **4.4** *P* **49** *L* **1** # 193

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

This specification is not consistent with its common mode noise measurement requirements. Clause 33 specifies a range of 1 MHz to 100 MHz for a PSE. Other clauses are for a MDI signal pairs and have no concept of measurement BW.

Testing during clause 33development ensured data integrity with the constraints imposed. Reducing the BW of existing clause common mode measurements should not reduce the compliance of legacy systems. Requiring PSE to meet other clauses below 1 MHz places an unnecessary cost burden on the system.

SuggestedRemedy

Modify other clauses or place a statement in clause 33 that allows the Ethernet MDI to use the clause 33 common mode requirements whether PoE power is present or not.

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.7** *P* **51** *L* **44** # 81

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X**

75 ohms is not defined at any particular frequency.

SuggestedRemedy

Most ports that have such termination are AC coupled to maintain DC isolation, thus they will not be 75 ohms at DC. We need to spec this better.

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.8** *P* **53** *L* **52** # 88

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Draft D0.9

We need to clearly define that Midspan should provide signal continuity for 1G Midspan as well.

SuggestedRemedy

Change line 53 from"A Midspan PSE inserted into a channel shall provide continuity for the signal pairs."

To "A Midspan PSE inserted into a channel shall provide continuity for the signal pairs for 10/100 and 1000BT Midspan device".

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.8** *P* **54** *L* **5** # 211

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **X**

Comment about 2 pair Cat 5 cabling is misleadingly acceptive.

SuggestedRemedy

Add text:
"The specification of two pair midpan PSEs is beyond the scope of this document."

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.8.1.1** *P* **54** *L* **22** # 19

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Equations on lines 22 and 32 are not set according to 2007 style manual.

SuggestedRemedy

Re-set equations to meet 2007 style manual guidelines.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **4.8.1.4** *P* **55** *L* **1** # 82

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **D**

Category 5 is obsolete now that 1000BASE-T is supported

SuggestedRemedy

Change to Category 5E

Proposed Response *Response Status* **O**

Cl **33** *SC* **5.5** *P* **56** *L* **1** # 20

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Equation is not set according to 2007 style manual.

SuggestedRemedy

Re-set equation to meet 2007 style manual guidelines.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **5.8** *P* **56** *L* **25** # 200

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

The cable current limits selected should provide temperature margin above design limits of the broader market. Ambient values do not need to be specified but values used to calculate system interoperability parameters should reflect broad market requirements.

SuggestedRemedy

Survey the task force members to determine an acceptable ambient operating range for cables. Calculate parameters dependent on ambient temperature using the results of this survey.

Proposed Response *Response Status* **O**

Cl **33** *SC* **5.9** *P* **56** *L* **36** # 69

Patoka, Martin TI

Comment Type **T** *Comment Status* **X**

"a) Power classification and power level in terms of maximum current drain over the operating voltage range, 44V to 57 V, applies for PD only"

"d) “PSE” or “PD” as appropriate"

Since we have new and incompatible PD/PSE combinations, labelling the PSE and PD type would be of value

SuggestedRemedy

"a) Power classification, type (e.g. 1 or 2) and power level in terms of maximum current drain over the operating voltage range, 44V to 57 V, applies for PD only"

"d) “PSE” or “PD” and type (e.g. 1 or 2) as appropriate"

Proposed Response *Response Status* **O**

Cl **33** *SC* **5.9** *P* **56** *L* **36** # 89

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Draft D0.9

Update a) : If it for PDs only it should be from 36V to 57V.

SuggestedRemedy

Change a) from " Power classification and power level in terms of maximum current drain over the operating voltage
range, 44V to 57 V, applies for PD only"

To: "Power classification and power level in terms of maximum current drain over the operating voltage range, 36V to 57 V, applies for PD only"

Proposed Response *Response Status* **O**

Cl **33** *SC* **6** *P* *L* # 268

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

We need to consider what happens when there is a loss of communication more carefully. Simply throttling the power back to the HW level does not make sense as teh device is hosed

SuggestedRemedy

At the very least the PSE should support the last negotiated state not the HW state as it is not guranteed what the device will do if the power is throttled back.

Additionally, we can look at mechanisms like power cycling within certain time limits that we specify to try and get the agent up and running.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6** *P* **57** *L* **2** # 123

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X**

PDs that requires more then 12.95W has a name. It is called type 2 PDs and they are classified as Class 4 PDs.

SuggestedRemedy

Change from:

"....PDs that require more then 12.95W shall.."

To:

"Type 2 PDs shall.."

Proposed Response *Response Status* **W**

see 239

Cl **33** *SC* **6** *P* **57** *L* **2** # 259

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

I believe our plan is to use 802.1ABREV not 802.1AB

SuggestedRemedy

Please correct the reference to relfect the revised version of 802.1AB

Proposed Response *Response Status* **W**

see 263

Cl **33** *SC* **6** *P* **57** *L* **2** # 239

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X**

This should ready Type 2 PDs to be consistant with the rest of the draft

SuggestedRemedy

Please rewrd the following:

"PDs that require more than 12.95 W"

TO

"Type 2 PDs"

Proposed Response *Response Status* **W**

see 123

Cl **33** SC **6.1** P **57** L **8** # 83
Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X**

Sentence does not constrain requirement to PSEs that implement clause 22 or 45

SuggestedRemedy

Change to "A PSE implementing either clause 22 or clause 45 management interface shall...

Proposed Response *Response Status* **O**

Cl **33** SC **6.1.1** P **57** L **33** # 98
Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X**

Error in the description of the bit.

SuggestedRemedy

Should be 0=Type 2 Physical.....

Proposed Response *Response Status* **O**

Cl **33** SC **6.1.1** P **57** L **33** # 197
Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

Correct the typo in table 33-15, bit 11.4.

SuggestedRemedy

Changed the bit value to 0 for the disabled state.

Proposed Response *Response Status* **O**

Cl **33** SC **6.2** P **61** L # 266
Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

The TLV descriptions are a summary of what is in ANSI/TIA 1057. In addition to a risk that at some point these two standards may differ, the information needs to be elaborated on

SuggestedRemedy

Either do this whole thing by reference or incorporate the entire descriptions from ANSI/TIA 1057-2006

Proposed Response *Response Status* **O**

Cl **33** SC **6.2** P **61** L # 241
Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**

Some of the text in section 33.6.2 and its subsection is not correctly marked according to the convention used by the editor. For example 33.6.2.2 is new material from 802.3-2005

SuggestedRemedy

Pls. mark text according to convention w.r.t 802.3-2005, D0.8 etc.

Proposed Response *Response Status* **O**

Cl **33** SC **6.2** P **61** L **25** # 263
Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

I believe our plan is to use 802.1ABREV not 802.1AB

SuggestedRemedy

Please correct the reference to relfect the revised version of 802.1AB

Proposed Response *Response Status* **W**

see 259

Cl **33** SC **6.2** P **61** L **33** # 42
Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

"shown in Annex 33F (Informative)."

Annex 33F not in draft

SuggestedRemedy

Don't forget to add ...

Proposed Response *Response Status* **W**

see 264, 24

Cl **33** SC **6.2** P **61** L **33** # 24
LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **X**

Reference to Annex 33F, which is non-existent.

SuggestedRemedy

TF to generate Annex 33F for incorporation into draft, or remove reference.

Proposed Response *Response Status* **W**

see 264, 42

Cl **33** *SC* **6.2** *P* **61** *L* **33** # 264
Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**
We are referencing material in an Annex that is not created yet (33F)

SuggestedRemedy
Please delete text or insert editorial note to indicate that this text is pending Annex 33F

Proposed Response *Response Status* **W**
see 24, 42

Cl **33** *SC* **6.2** *P* **62** *L* **18** # 25
LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **X**
Table 33-18 contains fields marked 'TBD.'

SuggestedRemedy
Fill 'TBD' fields with real data, or remove from table.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.2.1** *P* **61** *L* **43** # 217
Diab, Wael Broadcom

Comment Type **E** *Comment Status* **X**
Can we reproduce the ANSI TLV in the 802.3 document?

SuggestedRemedy
Please reproduce the TLV in the 802.3 document, or at the very least circulate with the review package

Proposed Response *Response Status* **W**
CE Note: comment was missing comment type. CE set it to E.

See 240

Cl **33** *SC* **6.2.1** *P* **61** *L* **43** # 43
Patoka, Martin TI

Comment Type **E** *Comment Status* **X**
"The minimum status TLV definition follows the format defined in ANSI/TIA-1057"

The paragraph number may change by document revision

SuggestedRemedy
Add the document revision, data, etc.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.2.1** *P* **61** *L* **43** # 240
Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X**
Do we have a release from ANSI/TIA to copy material into our draft?

SuggestedRemedy
If needed, please work with the staff or alert them to this issue

Proposed Response *Response Status* **W**
see 217

Cl **33** *SC* **6.2.2** *P* **61** *L* **47** # 212
Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **A** *ez*
The material regarding TLVs is all new. There is nothing about even the concept of TLVs in 802.3af

SuggestedRemedy
Correctly mark all new material using 802.3af as the baseline

Response *Response Status* **U**
ACCEPT IN PRINCIPLE.

see 22

Cl **33** *SC* **6.2.2** *P* **61** *L* **47** # 22
LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **A** *ez*

Text is new, but not marked as an insertion.

SuggestedRemedy

Mark text as a D0.9 insertion.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **6.3** *P* **63** *L* **1** # 26
LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **X**

Table 33-19 contains fields marked TBD.

SuggestedRemedy

Develop information to place into 'TBD' fields, or delete from table altogether.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.3.2** *P* **63** *L* **27** # 198
Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X**

The PD power in not completely specified.

SuggestedRemedy

The PD power should represent its peak 1 second average power.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.4** *P* **64** *L* **6** # 84
Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X**

State diagram has a number of undefined variables

SuggestedRemedy

Define all variables used in the state diagram.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.4.1** *P* **65** *L* **14** # 145
Law, David 3Com

Comment Type **TR** *Comment Status* **X**

Subclause 33.2.7.2a Type 2 hardware classification permits a Type 2 PSE to perform a single classification if it supports link layer classification. It however then requires that a PD that is classified as Class 4 is treated as a Type 1 PD until link layer classification is performed. I assume the link layer classification is then allowed to increase the power up to the Type 2 PD levels.

Based on the above, if a communications failure causes the PSE to revert to the initial hardware classification, in this case a PD that has increase its power through link layer classification it would have its power allocation cut back in the PSE to the Type 1 maximum. Since the PD may have no idea this is happening it may continue to draw the additional power it though it still had allocated - this in turn could cause the PSE to shut off the PD since it is now exceeding its 'requested' power.

SuggestedRemedy

Change the text so that in event of loss of communications the allocated power will remain at whatever level the last link layer classification was.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.4.1** *P* **65** *L* **7** # 267
Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

The "collision" mechanism needs to be thought out a little more. Specifically, the cases that occur. For example, if the PD is requesting more power and PSE is requesting less power may be a different situation than if both are requesting more power. The timers may not be the best way to resolve the conflict

Also, the term collision is confusing and should be avoided.

SuggestedRemedy

Seperate state machines for the PSE and PD should be done. In each state machine, if a new request is received a behaviour can be defined

In this paradigm we can identify what would constitute a conflict that needs to be resolved.

Proposed Response *Response Status* **O**

Cl **33** *SC* **7** *P* **66** *L* **1** # 232

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **D**

Please update PICs

SuggestedRemedy

Please update PICs OR Please add an editors note at the beginning of the PICs section stating that these are innaccurate until the normative text is near complete.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The CE assumes that PICS will be generated after the text is completed, so while I agree with the comment no changes to the text will be made.

Cl **33** *SC* **7.2.3** *P* **67** *L* **6** # 45

Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

T2 PD required to support classification

SuggestedRemedy

Add section for t2 PD, both physical and LLDP are required

Proposed Response *Response Status* **O**

Cl **33** *SC* **7.2.4** *P* **67** *L* **10** # 44

Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

PSE major capability for type 1 or 2 not present

SuggestedRemedy

add this capability

Proposed Response *Response Status* **O**

Cl **33** *SC* **7.3.2** *P* **68** *L* **21** # 47

Patoka, Martin TI

Comment Type **E** *Comment Status* **X**

With addition of 1000bT, 33.2.1 allows midspan powering on either pair

SuggestedRemedy

Feature: PSEs supporting only 10bT and 100bT shall only implement Alternative B

Proposed Response *Response Status* **O**

Cl **33** *SC* **7.3.2** *P* **69** *L* **30** # 46

Patoka, Martin TI

Comment Type **E** *Comment Status* **A** *ez*

new PSE requirements need to be added.

SuggestedRemedy

PSE25: Type 1 PSE assign to class 0 ...
PSE25a: Type 2 PSE recognize class4 as a T2 PD
PSE25b: T2 PSE provide either T2 physical layer, T2 LLDP, or both classification

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The CE assumes that PICS will be generated after the text is completed, so while I agree with the comment no changes to the text will be made.

Cl **33** *SC* **7.3.3** *P* **72** *L* **35** # 55

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X**

Table item 11 for PD does not reflect PD type 2 capability. Also, other T2 characteristics not accounted for

SuggestedRemedy

PD 11 recomends this for type 1
PD11a added for T2 PDS to present Class 4 and to handle physical layer 2 class
PD11b added for T2 PD to perform LLDP classification and messaging

Proposed Response *Response Status* **O**

Cl **33** *SC* **Figure 33-12a** *P* **36** *L* **1** # 231

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **A** *t33-12a*

Please redraw Figure 33-12a in Frame. It is difficult to maintain non-frame figures in the 802.3 documents once the group is done. for example, modifications due to maintenance are hard.

SuggestedRemedy

Please redraw using Frame and similar conventions as used in other state diagrams

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **figure 33-12a** *P* **36** *L* **15** # 87

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **R** *t33-12a*

Draft D0.9

The purpose of class event 3 is to create defined behaviour for type 2 PD when pinged repeaedly by Type 2 PSE.
There is no need to require that class 3 must consume 40mA.
It is possible that after two class events the PD will shut off the classiication current source due to thermal limitations.

SuggestedRemedy

1. Define class event 3 as follows:
"class event 3 is the event when PSE voltage ramps from V>Vthm towards Von"
2. Delete the "i=40mA" from Class Event 3 or add explenatory comment that explains that the 40mA is defined for future use of finger # 3 etc and is not required for compliant Type 2 device or eq. wording.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33** *SC* **Figure 33-4** *P* **5** *L* **1** # 74

Dove, Daniel — ProCurve Networking

Comment Type **TR** *Comment Status* **A** *fig33-4*

These figures are missing information that would be useful such as the pair A, B,C,D or pin #s. Also for figure 34a. Figure 34b looks like two identical drawings..reminds me of the kid puzzle "find the difference". I was never good at that game, but they look identical.

SuggestedRemedy

Assign pair A, B,C,D on the pairs and fix 34b so there are two different drawings.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Resolved by 250

Cl **33** *SC* **Figure 33-4b** *P* **7** *L* **1** # 250

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **A** *fig33-4*

These figures are not accurate. They are showing 4-Pair power rather than 2-Pair power over the 2 different alternatives.

SuggestedRemedy

Please only show the 2-Pair power attaching to the correct pairs for Alt A and Alt B. Once we have the vote on 4-Pair power, we can go back and remodify these figures if necessary.

Also, please label the pairs to be consistant with Alt A and Alt B.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Editor to delete appropriate wires and add pin numbers to wires.

Cl **33** *SC* **Figure 33-9a** *P* **28** *L* **20** # 114

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D**

We vote on 820mA and not 720mA at the horizontal part of the curve after 75msec.

SuggestedRemedy

Change from 720mA to 820mA from T=75msec to infinity.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

see 215

Cl **33** *SC* **Table 33-12** *P* **40** *L* **18** # 104

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *t33-12*

Draft D0.9:

Table 33-12 items 1: 40V (acctually it is 39.71V) is the correct number for steady state operation however in order to meet the 7.6% low transient support as specified in table 33-5 item 2a, the PD should design and work at 36V minimum as well.
In addition, the ad hoc have decided to use the same voltage thresholds used in 802.3af PD for 802.3at PD in order to simplify the specification.

Rational and some mathematics to support the above:

a) PSE voltage during transient: 50V-50*7.6% = 46.2V
b) PD voltage at the PI:
Vpd=(Vpse+(Vpse^2-4*R*Ppd)^0.5)/2.
For Ppd=29.5W,
R=12.5 ohms
Vpd=(46.2+(46.2^2-4*12.5*29.5)^0.5)/2=35.93V ==> 36V.
c) At this point the port current will be 29.5W/35.93V=0.82A.
In addition: PSE's Icut_min must be equal or higher then 0.82A.

See attached presentation for more details.

SuggestedRemedy

1. Table 33-12 item 1 for type 2 PD:
Change PD minimum operating voltage to 36V.

2. Table 33-5 item 8:
Add additional row for type 2 PSE specifying that Icut_min=41000/Vport for overload caused by PSE voltage down transient up to 250usec.

3. Add in the additional information column in 33.2.8.6:
"The PSE shall not turn off the port if Iport is less then or equal to 820mA for a time duration of leass then or equal to 250uSec."

Notes (an other reasons why 820mA, 50msec, 5% duty is a good thing):
1. This is not a positive current transient caused by PSE dv/dt. It is cuased by PSE voltage drop.
Per other comments, Tcut min. should be 50msec min. so this requiremnet for 820mA , 250usec is already covered.
3. PD shall not limit its input below 820mA for 250usec duration.
Per other comments PD may require 820mA for max. 50msec , 5% max duty cycle.

Proposed Response *Response Status* **O**

Cl **33** *SC* **Table 33-15** *P* **57** *L* **29** # 260

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X**

Currently the management object only shows control and status for Physical Layer Classification. Need to add equivelant for Data Link Layer Classification

SuggestedRemedy

Please add the following bit:

"11.5 Enable Type 2 Data Link Layer Classification
1= Type 2 Data Link Layer classification enabled
0= Type 2 Data Link Layer classification disabled
R/W
"

Change the first row, first column from "11.15:5" to "11.15:6"

Insert appropriate description of bit:

33.6.1.1.1b Enable Type 2 Data Link Layer Classification (11.5)
Bit 11.5 controls Type 2 Data Link Layer classification as specified in 33.2.7.2a. A PSE that indicates support for Type 2 Data Link Layer classification in register 12.14 may also provide the option of disabling Type 2 Physical Layer classification through bit 11.5.

A PSE that does not support Type 2 Data Link Layer classification shall ignore writes to bit 11.5 and shall return a value of '0' when read. A PSE that supports Type 2 Data Link Layer classification but does not allow the function to be disabled shall ignore writes to bit 11.5 and shall return a value of '1' when read. The Type 2 Data Link Layer classification function shall be enabled by setting bit 11.5 to logic one and disabled by setting bit 11.5 to logic zero.

Proposed Response *Response Status* **O**

Cl **33** *SC* **Table 33-16** *P* **59** *L* **5** # 261

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

Currently the management object only shows control and status for Physical Layer Classification. Need to add equivelant for Data Link Layer Classification

SuggestedRemedy

Please add the following bit:

"12.14 Type 2 Data Link Layer Classification Supported
1= PSE supports Type 2 Data Link Layer classification
0= PSE does not support Type 2 Data Link Layer classification
RO
"

Change the first row, first column from "12.15:14" to "12.15"

Insert appropriate description of bit:

Insert section 33.6.1.2.1b:
33.6.1.2.1b Type 2 Data Link Layer Classification Supported (12.14)
When read as a logic one, bit 12.14 indicates the PSE supports Type 2 Data Link Layer classification as defined in 33.2.7.2a. When read as a logic zero, bit 12.14 indicates that the PSE lacks support for Type 2 Data Link Layer classification. If supported, the function may be enabled or disabled through the Enable Type 2 Data Link Layer Classification bit (11.5).

Proposed Response *Response Status* **O**

Cl **33** *SC* **Table 33-3** *P* **18** *L* **11** # 244

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **X**

Please either delete the table in its entirety or modify the right hand most column

SuggestedRemedy

Either delete the entire table

OR

change the title of the right hand column to read "Power Ranges Available at output of PSE" and modify each row accordingly:

0 ... 0 - 15.4W
1 ... 0 - 4.0W
2 ... 4.0 - 7.0W
3 ... 7.0 - 15.4W
4 ... Type 1...Assign to Class 0
4 ... Type 2...0 - 36W

Proposed Response *Response Status* **W**

see 9, 163

Cl **33** *SC* **Table 33-4a** *P* **20** *L* **12** # 115

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-4a*

DraftD0.9:
There is no technical reason to require two current limit thresholds one for Class event up to 100mA and the 2nd is up to 5mA for mark event.

They should be the same number i.e. 100mA max otherwise it will increas PSE costs for no justified reason.
The implemntor can use lower number then 100mA.

SuggestedRemedy

Change item 2b in table 33-4a from 5mA max. to 100mA max.
Change the minimum value of item 2b to 5mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. See 135.

Cl **33** SC **Table 33-5** P **24** L **35** # 247

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *t33-5*

720mA does not accurately reflect the minimum current or for that matter the maximum. The contribution for TIA-TR42 ties the maximum current allowed to the ambient temperature. Thus, 720mA is only valid at 45C ambient and not for example at 55C, 57C, 52C, 47C etc. By stating 720mA as the minimum current, we are implicitly restricting the use of 802.3at to 45C ambient on the cables, which would impact our broad market potential.

The cabling community has put a lof of effort into their contribution and we should accurately reflect that in our draft.

SuggestedRemedy

There are 3 possible solutions to this issue:

- If the current framework is to be retained, the accurate minimum would be 0mA and the accurate maximum would be 720mA. This would cover the entire range of operating currents and temperatures. We would then need to decide on how to detect/enforce this and what the PD can rely on and/or if it needs to do power management based on temp.

- Alternately, a designation of variable with the explanation that this is reflective of the ambient temperature in the associated text section to this line item in the table. This would also have the same issues as the above

- Alternately, the group can decide on an acceptable operating temperature that meets the broad market criterea. Based on this we can pick the current level.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Insert section 33.1.4: "To use IEEE 802.3at, the ambient must be 15C below cable rating. Reference ISO/IEC XXXX. The value of Icable is 720mA.
Editors note: these numbers are not final and are subject to further information from the cabling liaisons. Final numbers will require 75% for adoption."

Replace all references, direct or indirect to cable current with Icable.

Cl **33C** SC **1.7** P **85** L **6** # 93

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X**

We need to update this part for supporting tests for foldback current limit tests in more general way as done for the startup mode.
(Comments from the maintanance group per MR # 1162.)

SuggestedRemedy

Change the following in Annex 33C clause 33C.1.7:

1. In Figure 33C.7 upper part: add a box labeled "variable load" in series to S1
2. Replace test procedure PSE-7 item 3 text from:

"3) Verify that Iport is within the limits shown in Figure 33C.4"

With "3) Change the variable load in order to verify that Iport is within the limits of Figures 33C.4 and 33C6.1. Please note that the variable load type (resistive, constant voltage or other) depends on different PSE implementations."

Clause 33C.1.4 PSE-4:
Change item 3 in PSE 4 from "Verify that ..in Figure 33C.4" to "Verify that ..in Figures 33C.4 and 33C.6.1"

Change the note in the last two sentences in clause 33C.1.4 after item 6 in PSE-4:
From: "Test setup…….expected per Figure 33C.4."
To: "Test setup…….expected per Figure 33C.4 and 33C.6.1."

Proposed Response *Response Status* **O**

Cl **99** SC P L # 219

Diab, Wael Broadcom

Comment Type **E** *Comment Status* **A** *ez*

Some pages are missing line numbers

SuggestedRemedy

Please add line numbers

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* **1** *L* **1** # 153

Law, David 3Com

Comment Type **E** *Comment Status* **A** *ez*

While the front matter is not within scope of any ballot please consider the following comments.

[1] Please change the text 'Amendment to IEEE Std 802.3(tm)-2005' to read 'Amendment to IEEE Std 802.3(tm)-200X' since this will be an amendment to the IEEE 802.3 revision currently under development, not IEEE Std 802.3-2005.

[2] Please remove the TM symbol related to the IEEE P802.3at Task Force, a document can be trademarked, a Task Force can't.

[12] While the style manual states that lower case roman numerals should be used for the front matter please change to arabic numerals so that the page number match the pdf page number.

SuggestedRemedy

See comment.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* **11** *L* **1** # 151

Law, David 3Com

Comment Type **E** *Comment Status* **A** *ez*

We do not provide Table of Figures or Table of Tables in IEEE 802.3 standards. I don't have any problem with them being included in the draft however a editors note should be provided to state that they will be removed during publication.

SuggestedRemedy

See comment.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* **2** *L* **31** # 152

Law, David 3Com

Comment Type **ER** *Comment Status* **A** *ez*

The text 'Balloted positive votes implicitly apply to the draft amendment as published for review—including any future changes to such provisional technical specifications.' seems to be in conflict to IEEE balloting procedure. When a voter casts an approve ballot on one draft they have the right to cast a disapprove ballot on the next draft based on any changes made between the two drafts.

SuggestedRemedy

Delete the text 'Balloted positive votes implicitly apply to the draft amendment as published for review—including any future changes to such provisional technical specifications.'.

Response *Response Status* **U**

ACCEPT.

Cl **99** *SC* *P* **3** *L* **55** # 208

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **A** *ez*

Please do not number the front matter pages with alpha characters. This leads to confusion during comment generation as to whether to use PDF page numbers or printed pages numbers.

SuggestedRemedy

Make printed pages number match PDF page numbers

Response *Response Status* **U**

ACCEPT.

Cl **99** *SC* *P* **5** *L* **1** # 149

Law, David 3Com

Comment Type **E** *Comment Status* **A** *ez*

Please update the list of special symbols to the latest version that can be obtained from URL:[http://www.ieee802.org/3/tools/index.html].

SuggestedRemedy

See comment.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* **7** *L* **1** # 150

Law, David 3Com

Comment Type **E** *Comment Status* **A** *ez*

Please use TOC reference page from the attached FrameMaker file for generating the index. This will fix the spacing issues and will also cope better with multi-line titles as well as Annex titles which are current missing the Annex title text.

SuggestedRemedy

See comment.

Response *Response Status* **C**

ACCEPT.

Cl **99** *SC* *P* **ii** *L* **20** # 218

Diab, Wael Broadcom

Comment Type **E** *Comment Status* **X**

I think the inserted text is inserted relative to D0.8 not D0.9

SuggestedRemedy

May want to clarify text and/or watchout for it on next draft

Proposed Response *Response Status* **O**

Cl **99** *SC* *P* **ii** *L* **24** # 230

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A** *ez*

Please note that it will require 75% to adopt final number

SuggestedRemedy

Please note that it will require 75% to adopt final number

Response *Response Status* **U**

ACCEPT.

Cl **99** *SC* *P* **iii** *L* **2** # 229

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A** *ez*

Im assuming the box on this page is an editor's note

SuggestedRemedy

Please mark accordingly. Add 'NOTE -' in front of 'This'

Response *Response Status* **U**

ACCEPT.