Cl **33** *SC* **2.2** *P* **8** *L* **50** # 116

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *4p*

The standard should not preclude implementations that are using both alternative A and B due to the following reasons:
a) It is out of scope of the standard to limit implementations.
b) There are no interoperability issues if PD gets power from two 2 pairs power source. It is the load responsibility (PD) to meet the 2P specification for each 2P. Implementation methods are out of scope of the standard.
c) It is economically feasible as shown in numerous presentations
d) It is technically feasible as shown by the same presentations.
e) There are products in the market that already is using the 2 x 2P implementation e.g. High power Midspan that is using 2 x 2P and applications that are using 2P power coming from the Switch and additional power delivered from Midspan.
f) There is huge market for higher power then 30W over 2P.
g) There is no additional cost issue. The $/watt cost is even lower then in 2P system as shown in previous meeting presentations.
h) For outdoor applications, temperature rise issues of the cables when using 60degC cabling system grade can be solved if the same power is delivered over 2 x 2P which is an easy solution for outdoor applications.
i) Users will do it any way to utilize the full capability of the existing infrastructure.
J) In previous meeting switch and PHY vendors wanted the ability to use the same cable which consists of 4 pairs to support two PDs that each one of them is connected to a 2P system. The current text precludes using this feature.

SuggestedRemedy

Change from:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.3.4** *P* **10** *L* **29** # 106

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *baseline*

Draft0.9
During "Short Circuit" Condition i.e. when PSE and PD are no longer at their operating voltage range, there is no technical need to keep PSE port on for TLIM.
It creates many problems such:
1. Prevents meeting item 21 in table 33-5, Ted (Time delay between consecutive start ups.
2. Excessive heat.
See more details in MR #1167.

SuggestedRemedy

To allow the PSE to turn the port to OFF mode when Vport <> Normal operating range at any t<TLIM_MIN.
Remedy steps:
1) Add new variable option_vport_lim to 33.2.3.4. It will be an optional variable.

option_vport_lim
This variable is indicating If PSE port voltage is out of operating range during normal operating mode.
Values:
False: Vport is within the Vport normal operating range as defined by table 33-5.
True: Vport is not within the Vport normal operating range as defined by table 33-5.
3) Add the following text to 33.2.8.8 after item e. Items d and e are resereved for maintanance request 1162).
"f) During short circuit condition, for PI voltages below or above Vport normal operation range as specifiied in table 33-5 the PSE may turn to IDLE state at any time t < TLIM_MIN.
"

4) Change state diagram (figure 33-6) per the attached drawing.

Using this optional variable in the state diagram will fix the problem by changing the inputs to ERROR_DELAY_SHORT state
from: tlim_timer_done
to: Tlim_timer_done + !tlim_timer_done*option_vport_lim*power_applied)

Effect on legacy equipment: None since the variable is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.5** *P* **16** *L* **25** # 57

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

Table 33-2. Calculation of the signature is not provided (as in 33.3.3), therefore a tolerance is not applicable. Current tolerance is bounded to 0uA, however this is not true of the PD (no minimum, could be -infinite). Since PDs theoretically have a NEGATIVE current intercept, bounding PSE to 0 causes a consistensy problem. Note that Fogure 33C-20 indicates a negative current offset. Current offsetts are cancelled out by the computation methed anyway.

SuggestedRemedy

Recomment setting the PSE tolerance to +/-50uA. Recommend moving figure 33C-20 to this section of normative text, including method of computation, and annotating the current offset on the figure.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.5.1** *P* **16** *L* **31** # 202

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *baseline*

The existing section on PD detection requires specific design requirements that are not necessary to ensure interoperability. Other detection methods have been disclosed:
http://www.ieee802.org/3/poep_study/public/sep05/naegeli_1_0905.pdf
The IEEE specification should ensure requirements for interoperability are in place.

This comment may also affect text in section 33.3.3.

SuggestedRemedy

Reference the PD model shown in figure 33-10, and require that the PSE detect values of Rpd_d for all permissible values of Cpd_d as specified in table 33-2.

Remove the text requiring two values but continue to provide guidance for designs that use the two probe method.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 227

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

This section is very confusing. We dive into Physical Layer classification and then do Data-Link Layer Classification. I would suggest that we make 33.2.7 a general introduction to classification. We then take 33.2.7 and 33.2.7a and make them subclauses of this new geenral section.

For the content of the general section on classification, I will submit a seperate comment (my previous comment in the .csv file).

SuggestedRemedy

I would suggest that we make 33.2.7 a general introduction to classification. We then take 33.2.7 and 33.2.7a and make them subclauses of this new geenral section.

Proposed Response *Response Status* **W**

see Law 170
see 226, 49

Cl **33** *SC* **2.7** *P* **17** *L* **31** # 180

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *33.2.7*

A PSE does not have to perform Type 2 Physical Layer classification in order to ensure mutual identification with a type2 PD.

SuggestedRemedy

Replace the sentence on line 31 with:

A Type 2 PSE shall perform type 2 Physical Layer classification and/or Data Link Layer classification.

Proposed Response *Response Status* **O**

see 71

A Type 2 PSE shall perform Physical Layer classification or Data Link Layer classification or both.

A Type 2 PSE may implement PL or DLL classification or both.

A Type 2 PSE that does not perform DLL classification shall implement PL classification.

Question:
Should a Type 2 PSE be required to implement PL classification?

Y: 6, N: 9, A: 2

.3 only:

Y: 3, N: 7, A: 1

Question:
Do we reject the comment?

Y: 8, N: 8, A: 2

Cl **33** *SC* **2.7** *P* **17** *L* **32** # 71

Patoka, Martin — TI

Comment Type **TR** *Comment Status* **X** *33.2.7*

"A Type 2 PSE shall perform classification using Type 2 hardware Physical Layer classification and may optionally perform link layer Data Link Layer classification."

We had a motion November 2006 that a type 2 PSE may choose its extension, which I interpret to mean that an endspan need only perform L2 class. This was recorded in the motion aggregator.

SuggestedRemedy

An Type 2 endspan PSE must perform classification using Type 2 Physical Layer classification or Type 2 Data Link Layer classification. A midspan PSE must perform Type 2 Physical Layer classification.

Proposed Response *Response Status* **W**

see 180

Cl **33** *SC* **2.7** *P* **17** *L* **35** # 117

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *33.2.7*

Draft0.9:
It is not clear from the text that A Type 2 PSE must do at least Type 1 Physical Layer classification in order to read Class 4 PDs that are Type 2 PDs by definition.
Class 4 IS THE UNIQUE IDENTIFICATION MEANS as required by the 5 Criteria.
Therefore:
PSE Type 2 must do at least 1st finger Physical layer classification to read if it class 1,2,3 or 4.
PSE Type 2 may omits the 2nd finger if it is using Layer 2 classification.
A type 2 PDs must implement both Layer 2 AND Physical layer classification.

SuggestedRemedy

Add the following text at line 35:

"Type 2 PSE shall implement at least one classification event of the Physical Layer Classification as per table 33-4a, to uniquely identify if PD is Type 1 or Type 2. Type 2 unique signature is Class 4 and represents PD max. Power.
If PSE is equipped with Layer 2 classification, it may later communicate with PD type 2 for lower PD power requirements"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Class 4 is the unique identifier required for midspans and that is why PDs are required to display class 4, but an endspan PSE can choose to not class the PD at all and use L2 as the mutual identification method. Since PDs are required to do both, the outcome will be full power in both cases.

[pulled out of the 33.2.7.bucket]

Cl **33** *SC* **2.7** *P* **17** *L* **44** # 58

Patoka, Martin — TI

Comment Type **T** *Comment Status* **D** *33.2.7*

"A Type 2 PSE performs Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

GIven that an endspan PSE may prefer to do L2 classification, this sentence should be ammended.

SuggestedRemedy

"A Type 2 PSE performs optional Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

Proposed Response *Response Status* **W**

see 180
See 216

Cl **33** *SC* **2.7** *P* **17** *L* **44** # 216

Diab, Wael — Broadcom

Comment Type **T** *Comment Status* **D** *33.2.7*

Second sentence needs to have the word may.

SuggestedRemedy

Please rewrite sentence from "A Type 2 PSE performs hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

"A Type 2 PSE may perform hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

Proposed Response *Response Status* **W**

see 180

I disagree that the word may adds any value. See 117 for reasoning. See also 58

Cl **33** *SC* **2.7.1** *P* **18** *L* **27** # 113

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *33.2.7*

Draft0.9:
According to the classification base line concept and associated motions the text should explicitly note that PD that asks more power then advertised in L1 hardware classification is not compliant.

The rational for this was to prevent interoperability issues when a Type 2 PD is connected to end span and get service while if connected to Midspan it will not work due to the fact that Midspan cant support L2.
As a result we mandate PD type 2 to support both L1 and L2 classification and specify that hardware classification results are max. Power values.

In addition it is already specified in the 802.3 specification that all numbers of class power are maximum numbers.

SuggestedRemedy

Add the following text right after Table 33:
"PD that asks more power then advertised in L1 hardware classification is not compliant to this standard".

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **18** *L* **42** # 59

Patoka, Martin — TI

Comment Type **T** *Comment Status* **X** *33.2.7*

"The Type 2 PSE shall provide to the PI VClass as defined in Table 33–4a."

H/W L1 class is optional.

SuggestedRemedy

"The Type 2 PSE may optionaly provide an enhanced hardware classification to the PI which consists of the following sequence where levels are defined in Table 33–4a. The PSE provides strong sourcing current and weak sinking current.
* Apply Vclass
* Allow settling time
* Measure Iclass
* Apply Vmark
* Allow settling time
* Apply Vclass
* ...

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **19** *L* **35** # 201

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *33.2.7*

A PSE can legally detect and power on a PD without classifying a PD. This allowance should continue.

SuggestedRemedy

Replace the sentence at line-34 with:
If classification is not performed or the result of the first classification event is class 4, …

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7.2a** *P* **19** *L* **40** # 181

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *33.2.7*

A PD should be able to ask for the power it requires.

Three independent classification mechanisms exist: type 1 and 2 Physical layer and type 2 Data Link Layer. Interoperability is ensured when a PD requests power from a PSE that can interpret the request. A type 2 PD can use type 1 Physical layer classification to request power.

SuggestedRemedy

Replace the sentence on line 40 with,
If the result of the first classification is any classes 0, 1, 2, 3, the PSE may omit the subsequent mark …

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8** *P* **7b** *L* **49** # 143

Johnson, Peter — Sifos Technologies

Comment Type **TR** *Comment Status* **X** *t33-5*

Tmps, Table 33-5 Item 7b, is presented from the perspective of a PD, not a PSE, it seems. 60 msec is the Minimum Valid Load Current Time that a PD must sustain to assure the PSE will keep it powered. From the PSE's perspective however, Tmps is the MAXIMUM allowed Valid (Imin2) Load Interval over which the PSE does not have to reset its Tmpdo timer (and therefore delay a shutdown). Since this parameter is expressed as a minimum, it can be (and has been) interpreted as the Minimum Valid Load Time required to re-start shutdown timing.

SuggestedRemedy

Title the Parameter in 33-5, 7-b, "Valid DC MPS Signature Time Required to Restart Disconnect Shutdown Timing". "60 msec" should then become a MAXIMUM limit, not a MINIMUM limit.

Proposed Response *Response Status* **W**

Need to clarify text.

Cl **33** *SC* **2.8.4** *P* **26** *L* **37** # 195

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *Ipeak*

The formula for IPEAK ensures a constant PSE power of 17.6 W. To ensure interoperability the PSE needs to provide what the PD can demand.

The PD may demand 14.4 W. When the PSE is providing 44 V, the PSE must provide 17.6 W. However, when the PSE is providing 57 V, the PSE only needs to provide 16.0 W to support the same PD demand. This unnecessary power requirement increases when using PoE plus power levels. These requirements place an unnecessary burden on the PSE.

These comments also apply to 33.2.8.4a.

This comment is related to other comments on this same section and the PD table 33-12 and 33.3.5.2.

SuggestedRemedy

If the PD is a constant power load that can demand 400/350Iport more, then determine the PSE power for a given PD demand, divide this PSE power by the PSE voltage to get IPEAK. This is a quadratic equation.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.5** *P* **27** *L* **9** # 121

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *annex*

Draft0.9:
In many ocasions the normative text send the reader to see figures 33C.4 and 33C.6 which contains valuble data.
These drawings should be at the normative text as it was in early drafts of 802.3af and were moved to the informative section due to editing considerations.

SuggestedRemedy

Move figures 33C.4 and 33C.6 to the normative section at the location where they are mentioned for the first time.

Proposed Response *Response Status* **W**

see 50

Cl **33** *SC* **2.8.6** *P* **27** *L* **11** # 50

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X** *annex*

Overload is used in a particular way, and the requirement is difficult to understand. Also, confusion persists about the relationship of the ranges.

SuggestedRemedy

add definition:
"Overload is defined as the load current range between the maximum current defined in 33.2.8.4 and the short circuit current defined in 33.2.8.8"

Move figure 33C-6 from the informative into this section to support the normative text. Create a second figure to support .at.

Proposed Response *Response Status* **W**

see 121

Cl **33** *SC* **2.8.8** *P* **27** *L* **33** # 61

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

The term "short circuit" is not defined, arising to much confusion about table 33-5. Also, there has been much discussion about the foldbacl of 33.2.8.5. Many veterans believe that the inferred foldback applies to short circuit as well as startup.

SuggestedRemedy

Add definition: "The short circuit condition occurs when the PSE output is loaded beyond the overload range (Icut_max) and some form of hardware limiting occurs to keep the maximum output current below Ilim_max."

I have suggested 33C-6 be move to normative text, so the reference should change.

I recommend that the foldback limits of 33.2.8.5 be moved here and an output I/V curve be provided. These have been discussed in maintenance.

Proposed Response *Response Status* **W**

Cl **33** *SC* **2.8.8** *P* **27** *L* **41** # 108

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *annex*

Draft0.9:
The specification allows foldback current limit implementations in startup mode as defined by 33.2.8.5.
MR request 1162 material and maintenance group attached drawing shows that the intent of the specification was to allow the same implementations during short circuit condition as well. However items d and e of 33.2.8.5 was not copied to 33.2.8.8 as should have done.

SuggestedRemedy

1. Move drawing 33C.4 or its updated version as a result of the Vport ad-hoc work to the normative section as it was in the early drafts of the IEEE802.3af.
2. Move drawing 33C.6 or its updated version as a result of the Vport ad-hoc workto the normative section as it was in the early drafts of the IEEE802.3af.
3. Add drawing 33C.6.1 to 33.2.8.8

4. Replace the following text:

The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC input voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
See Figure 33C.4 and Figure 33C.6.

With the proposed text: (items d and e are additions to previous text)
The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC output voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
d) During short circuit condition, for PI voltages above 30V, the ILIM requirement is as specified in Table 33-5, item 10.
e) During short circuit condition, for PI voltages between 10V and 30V, the minimum ILIM requirement is 60mA as long as system decides to keep the port ON, and the maximum requirement is as specified in Table 33-5, item 10.
During short circuit condition, for PI voltages between 0V and 10V, the minimum ILIM requirement is 0mA and the maximum requirement is as specified in Table 33-5, item 10.
See Figures 33C.4, 33C.6 and 33C.6.1."

5. Add the following notes after 33.2.8.8-e:

Notes:

1. Items d and e in 33.2.8.8 allows implementation of foldback
current limit type in which ILIM requirement is decreased if Vport is

decreased below pre specified value.

2. Short circuit condition definition in IEEE802.3af is a case in which the port voltages is dropped below normal operating voltages as defined by table 33-5 items 1 and 2 due too load fault conditions that exceeds table 33-5 item 8"

6. Add the following note text after 33.2.8.5-e:

Note: items d and e in 33.2.8.5 allows implementation of foldback current limit type in which Iinrush requirement is decreased if Vport is decreased below pre specified value.

Foldback current limit is optional in the standard.

IMPACT ON EXISTING NETWORKS:

No impact. It is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.1** *P* **33** *L* **42** # 124

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *4p*

The note in line 42 precludes the following applications:
1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD.

2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or power application.

The standard should not preclude implementations that are using standard compliant 2P system.

Theoretically a PD can get N x 2P power sources while each of the 2P system is well defined by the standard and the standard should not preclude it since it is implementation issue and it is not a source of interoperability issues.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:
"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode are not precluded by this standard as long as the requirements of this standard are kept for each mode."

Other equivalent wording is possible.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.3** *P* **37** *L* **11** # 62

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

Voltage and current offsett in table 33-8 are ambiguous.

SuggestedRemedy

Move a copy of figure 33C-20 to and annotate to show Ioffset. The value of Ioffset is not very restrictive since it is typically negative as shown in the figure. The voltage and current offset need to be defined as being related to the projection of the (two point) line-fit between 2.7V and 10.1V.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **38** *L* **47** # 52

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X** *annex*

The concept of physical layer classification is difficult to general readers to understand. This compounded by the 2 event technique.

SuggestedRemedy

A figure such as containned in stanford_1_0707 page 12 should be incorporated into this section to clarify the whole subject. It is important to put it in the normative section to support the text.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **42** *L* **24** # 191

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *Ipeak*

The peak operating current specified in this section is Pport_max/Vport. It is not clear that Pport_max is the power the PD is classified to because the Iport max of table item 4 contradicts this. For example, a class 3 PD can draw 6.49 W and with a 36 V input will draw 6.49/36 = 180 mA. The value in item 4 states 210 mA.

Also see a related comment on this same parameter. It is also not clear which Iport is being referenced-table 33-12 has items 4 and 5 with the same name.

SuggestedRemedy

The task force needs to review these values and state what ensures interoperability.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **43** *L* **46** # 184

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *baseline*

The value of Iport_max created by the formula-using PD Pport_max-does not match the value provided in table 33-12. For example, class 0 PD power is 12.95 W maximum and 12.95W/44V = 294 mA, not the 400 mA shown in table 33-12, item 4.

SuggestedRemedy

The PD formula provides approximately the correct answers when the PSE Pport_max values are scaled by 400/350 for the system classified power.

Table 33-12 values should match values created by the formula-rounding appears to have been used.

Proposed Response *Response Status* **W**

proposal 1: The peak current shall not exceed PPort max/VPort for more than 50ms max with a 5% duty cycle max. Peak current shall not exceed [equation].

Proposal 2: add:Iport_peak as definedin Table 33-12 item 4.

proposal 3: change to: The current for class 0-3 shall not exceed PPort max/VPort for more than 50ms max with a 5% duty cycle max. Current for class 4… Peak current shall not exceed [equation].

Cl **33** *SC* **3.6.1** *P* **46** *L* **13** # 15

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X** *baseline*

The itemized list is generally confusing. The whole point is that a PD with >180uF input capacitance may have difficulty meeting the DC MPS during a voltage transient.

SuggestedRemedy

Replace with a general CAUTION statement:

CAUTION--A PD with CPort > 180uF may not be able to meet the IPort specification in Table 33-13 during the maximum allowable port voltage droop (i.e. 57V to 44V in series with 20 ohms for a Type 1 PSE and 57V to 50V in series with 12.5 ohms for a Type 2 PSE). Such a PD should increase its IPort min or make other such provisions to ensure meeting the DC maintain power signature.

Proposed Response *Response Status* **W**

NOTE--A PD with CPort > 180uF may not be able to meet the IPort specification in Table 33-13 during the maximum allowable port voltage droop. Such a PD should increase its IPort min or make other such provisions to ensure meeting the DC maintain power signature.

Failed to pass consensus.

Cl **33C** *SC* **1.7** *P* **85** *L* **6** # 93

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X** *annex*

We need to update this part for supporting tests for foldback current limit tests in more general way as done for the startup mode.
(Comments from the maintanance group per MR # 1162.)

SuggestedRemedy

Change the following in Annex 33C clause 33C.1.7:

1. In Figure 33C.7 upper part: add a box labeled "variable load" in series to S1
2. Replace test procedure PSE-7 item 3 text from:

"3) Verify that Iport is within the limits shown in Figure 33C.4"

With "3) Change the variable load in order to verify that Iport is within the limits of Figures 33C.4 and 33C6.1. Please note that the variable load type (resistive, constant voltage or other) depends on different PSE implementations."

Clause 33C.1.4 PSE-4:
Change item 3 in PSE 4 from "Verify that ..in Figure 33C.4" to "Verify that ..in Figures 33C.4 and 33C.6.1"

Change the note in the last two sentences in clause 33C.1.4 after item 6 in PSE-4:
From: "Test setup…….expected per Figure 33C.4."
To: "Test setup…….expected per Figure 33C.4 and 33C.6.1."

Proposed Response *Response Status* **O**