Cl **33** *SC* **2.5** *P* **16** *L* **25** # 57

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

Table 33-2. Calculation of the signature is not provided (as in 33.3.3), therefore a tolerance is not applicable. Current tolerance is bounded to 0uA, however this is not true of the PD (no minimum, could be -infinite). Since PDs theoretically have a NEGATIVE current intercept, bounding PSE to 0 causes a consistensy problem. Note that Fogure 33C-20 indicates a negative current offset. Current offsetts are cancelled out by the computation methed anyway.

SuggestedRemedy

Recomment setting the PSE tolerance to +/-50uA. Recommend moving figure 33C-20 to this section of normative text, including method of computation, and annotating the current offset on the figure.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.5** *P* **27** *L* **9** # 121

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *annex*

Draft0.9:
In many ocasions the normative text send the reader to see figures 33C.4 and 33C.6 which contains valuble data.
These drawings should be at the normative text as it was in early drafts of 802.3af and were moved to the informative section due to editing considerations.

SuggestedRemedy

Move figures 33C.4 and 33C.6 to the normative section at the location where they are mentioned for the first time.

Proposed Response *Response Status* **W**

see 50

Cl **33** *SC* **2.8.6** *P* **27** *L* **11** # 50

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X** *annex*

Overload is used in a particular way, and the requirement is difficult to understand. Also, confusion persists about the relationship of the ranges.

SuggestedRemedy

add definition:
"Overload is defined as the load current range between the maximum current defined in 33.2.8.4 and the short circuit current defined in 33.2.8.8"

Move figure 33C-6 from the informative into this section to support the normative text. Create a second figure to support .at.

Proposed Response *Response Status* **W**

see 121

Cl **33** *SC* **2.8.8** *P* **27** *L* **33** # 61

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

The term "short circuit" is not defined, arising to much confusion about table 33-5. Also, there has been much discussion about the foldbacl of 33.2.8.5. Many veterans believe that the inferred foldback applies to short circuit as well as startup.

SuggestedRemedy

Add definition: "The short circuit condition occurs when the PSE output is loaded beyond the overload range (Icut_max) and some form of hardware limiting occurs to keep the maximum output current below Ilim_max."

I have suggested 33C-6 be move to normative text, so the reference should change.

I recommend that the foldback limits of 33.2.8.5 be moved here and an output I/V curve be provided. These have been discussed in maintenance.

Proposed Response *Response Status* **W**

Cl **33** *SC* **2.8.8** *P* **27** *L* **41** # 108

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *annex*

Draft0.9:
The specification allows foldback current limit implementations in startup mode as defined by 33.2.8.5.
MR request 1162 material and maintenance group attached drawing shows that the intent of the specification was to allow the same implementations during short circuit condition as well. However items d and e of 33.2.8.5 was not copied to 33.2.8.8 as should have done.

SuggestedRemedy

1. Move drawing 33C.4 or its updated version as a result of the Vport ad-hoc work to the normative section as it was in the early drafts of the IEEE802.3af.
2. Move drawing 33C.6 or its updated version as a result of the Vport ad-hoc workto the normative section as it was in the early drafts of the IEEE802.3af.
3. Add drawing 33C.6.1 to 33.2.8.8

4. Replace the following text:

The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC input voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
See Figure 33C.4 and Figure 33C.6.

With the proposed text: (items d and e are additions to previous text)
The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC output voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
d) During short circuit condition, for PI voltages above 30V, the ILIM requirement is as specified in Table 33-5, item 10.
e) During short circuit condition, for PI voltages between 10V and 30V, the minimum ILIM requirement is 60mA as long as system decides to keep the port ON, and the maximum requirement is as specified in Table 33-5, item 10.
During short circuit condition, for PI voltages between 0V and 10V, the minimum ILIM requirement is 0mA and the maximum requirement is as specified in Table 33-5, item 10.
See Figures 33C.4, 33C.6 and 33C.6.1."

5. Add the following notes after 33.2.8.8-e:

Notes:

1. Items d and e in 33.2.8.8 allows implementation of foldback current limit type in which ILIM requirement is decreased if Vport is decreased below pre specified value.

2. Short circuit condition definition in IEEE802.3af is a case in which the port voltages is dropped below normal operating voltages as defined by table 33-5 items 1 and 2 due too load fault conditions that exceeds table 33-5 item 8"

6. Add the following note text after 33.2.8.5-e:

Note: items d and e in 33.2.8.5 allows implementation of foldback current limit type in which Iinrush requirement is decreased if Vport is decreased below pre specified value.

Foldback current limit is optional in the standard.

IMPACT ON EXISTING NETWORKS:

No impact. It is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.3** *P* **37** *L* **11** # 62

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

Voltage and current offsett in table 33-8 are ambiguous.

SuggestedRemedy

Move a copy of figure 33C-20 to and annotate to show Ioffset. The value of Ioffset is not very restrictive since it is typically negative as shown in the figure. The voltage and current offset need to be defined as being related to the projection of the (two point) line-fit between 2.7V and 10.1V.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **38** *L* **47** # 52

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X** *annex*

The concept of physical layer classification is difficult to general readers to understand. This compounded by the 2 event technique.

SuggestedRemedy

A figure such as containned in stanford_1_0707 page 12 should be incorporated into this section to clarify the whole subject. It is important to put it in the normative section to support the text.

Proposed Response *Response Status* **O**

Cl **33C** *SC* **1.7** *P* **85** *L* **6** # 93

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X** *annex*

We need to update this part for supporting tests for foldback current limit tests in more general way as done for the startup mode.
(Comments from the maintanance group per MR # 1162.)

SuggestedRemedy

Change the following in Annex 33C clause 33C.1.7:

1. In Figure 33C.7 upper part: add a box labeled "variable load" in series to S1
2. Replace test procedure PSE-7 item 3 text from:

"3) Verify that Iport is within the limits shown in Figure 33C.4"

With "3) Change the variable load in order to verify that Iport is within the limits of Figures 33C.4 and 33C6.1. Please note that the variable load type (resistive, constant voltage or other) depends on different PSE implementations."

Clause 33C.1.4 PSE-4:
Change item 3 in PSE 4 from "Verify that ..in Figure 33C.4" to "Verify that ..in Figures 33C.4 and 33C.6.1"

Change the note in the last two sentences in clause 33C.1.4 after item 6 in PSE-4:
From: "Test setup…….expected per Figure 33C.4."
To: "Test setup…….expected per Figure 33C.4 and 33C.6.1."

Proposed Response *Response Status* **O**