Cl **33** *SC* **2.1** *P* **21** *L* **4** # 155

Law, David 3Com

Comment Type **TR** *Comment Status* **A** *fig33-4*

I can see no difference between the Alternative A and Alternative B shown in Figure 33-4b. Both alternatives show (incorrectly) all four pairs connected to the PSE.

SuggestedRemedy

Correct the figure so that only two pairs on each alternative are connected to the PSE. Following the convention we seem to be using in Figure 33-4, the outer two pairs are used for Alternative A and the inter two pairs are used for Alternative B. The Figure will however require some additional annotation to indicated which is which pair, since the 1000BASE-T PHY uses all four pairs, and without this annotation the figure will effectively be content free.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Resolved by 250

Cl **33** *SC* **2.2** *P* **8** *L* **50** # 116

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *4p*

The standard should not preclude implementations that are using both alternative A and B due to the following reasons:
a) It is out of scope of the standard to limit implementations.
b) There are no interoperability issues if PD gets power from two 2 pairs power source. It is the load responsibility (PD) to meet the 2P specification for each 2P. Implementation methods are out of scope of the standard.
c) It is economically feasible as shown in numerous presentations
d) It is technically feasible as shown by the same presentations.
e) There are products in the market that already is using the 2 x 2P implementation e.g. High power Midspan that is using 2 x 2P and applications that are using 2P power coming from the Switch and additional power delivered from Midspan.
f) There is huge market for higher power then 30W over 2P.
g) There is no additional cost issue. The $/watt cost is even lower then in 2P system as shown in previous meeting presentations.
h) For outdoor applications, temperature rise issues of the cables when using 60degC cabling system grade can be solved if the same power is delivered over 2 x 2P which is an easy solution for outdoor applications.
i) Users will do it any way to utilize the full capability of the existing infrastructure.
J) In previous meeting switch and PHY vendors wanted the ability to use the same cable which consists of 4 pairs to support two PDs that each one of them is connected to a 2P system. The current text precludes using this feature.

SuggestedRemedy

Change from:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8** *P* **7b** *L* **49** # 143

Johnson, Peter — Sifos Technologies

Comment Type **TR** *Comment Status* **X** *t33-5*

Tmps, Table 33-5 Item 7b, is presented from the perspective of a PD, not a PSE, it seems. 60 msec is the Minimum Valid Load Current Time that a PD must sustain to assure the PSE will keep it powered. From the PSE's perspective however, Tmps is the MAXIMUM allowed Valid (Imin2) Load Interval over which the PSE does not have to reset its Tmpdo timer (and therefore delay a shutdown). Since this parameter is expressed as a minimum, it can be (and has been) interpreted as the Minimum Valid Load Time required to re-start shutdown timing.

SuggestedRemedy

Title the Parameter in 33-5, 7-b, "Valid DC MPS Signature Time Required to Restart Disconnect Shutdown Timing". "60 msec" should then become a MAXIMUM limit, not a MINIMUM limit.

Proposed Response *Response Status* **W**

Need to clarify text.

Cl **33** *SC* **2.8.4** *P* **26** *L* **37** # 195

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *Ipeak*

The formula for IPEAK ensures a constant PSE power of 17.6 W. To ensure interoperability the PSE needs to provide what the PD can demand.

The PD may demand 14.4 W. When the PSE is providing 44 V, the PSE must provide 17.6 W. However, when the PSE is providing 57 V, the PSE only needs to provide 16.0 W to support the same PD demand. This unnecessary power requirement increases when using PoE plus power levels. These requirements place an unnecessary burden on the PSE.

These comments also apply to 33.2.8.4a.

This comment is related to other comments on this same section and the PD table 33-12 and 33.3.5.2.

SuggestedRemedy

If the PD is a constant power load that can demand 400/350Iport more, then determine the PSE power for a given PD demand, divide this PSE power by the PSE voltage to get IPEAK. This is a quadratic equation.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.1** *P* **33** *L* **42** # 124

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *4p*

The note in line 42 precludes the following applications:
1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD.

2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or power application.

The standard should not preclude implementations that are using standard compliant 2P system.

Theoretically a PD can get N x 2P power sources while each of the 2P system is well defined by the standard and the standard should not preclude it since it is implementation issue and it is not a source of interoperability issues.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:
"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode are not precluded by this standard as long as the requirements of this standard are kept for each mode."

Other equivalent wording is possible.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **23** # 12

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **T** *Comment Status* **X** *pd33.2.7*

The 'Usage' column in Table 33-10 seems unnecessary. Normative text already forces Type 1 PDs to use Class 0-3, and Type 2 PDs to use Class 4.

SuggestedRemedy

Remove 'Usage' column from Table 33-10.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **43** *L* **12** # 67

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *backfeed*

Table 33-12 item 10: Backfeed voltage
see also 33.3.5.10 P45 line 24.

The maximum allowed bridge reverse current is 2.8V/100K = 28uA. This requirement is too stringent and appears to prevent the use of schotty diodes. Given that we are doubling the current, efficiency and component temperature rise are adversely impacted. THere is no reason to limit the implementation of a PD to preclude the use of Schottky diodes.

SuggestedRemedy

Decrease the resistance to 9.09k. this was selected based on a B2100 diode 2A, 100V schottky at 125C reverse leakage at 60V (.3ma).

Proposed Response *Response Status* **W**

Cl **33** *SC* **Table 33-12** *P* **40** *L* **18** # 104

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *t33-12*

Draft D0.9:

Table 33-12 items 1: 40V (acctually it is 39.71V) is the correct number for steady state operation however in order to meet the 7.6% low transient support as specified in table 33-5 item 2a, the PD should design and work at 36V minimum as well.
In addition, the ad hoc have decided to use the same voltage thresholds used in 802.3af PD for 802.3at PD in order to simplify the specification.

Rational and some mathematics to support the above:

a) PSE voltage during transient: 50V-50*7.6% = 46.2V
b) PD voltage at the PI:
Vpd=(Vpse+(Vpse^2-4*R*Ppd)^0.5)/2.
For Ppd=29.5W,
R=12.5 ohms
Vpd=(46.2+(46.2^2-4*12.5*29.5)^0.5)/2=35.93V ==> 36V.
c) At this point the port current will be 29.5W/35.93V=0.82A.
In addition: PSE's Icut_min must be equal or higher then 0.82A.

See attached presentation for more details.

SuggestedRemedy

1. Table 33-12 item 1 for type 2 PD:
Change PD minimum operating voltage to 36V.

2. Table 33-5 item 8:
Add additional row for type 2 PSE specifying that Icut_min=41000/Vport for overload caused by PSE voltage down transient up to 250usec.

3. Add in the additional information column in 33.2.8.6:
"The PSE shall not turn off the port if Iport is less then or equal to 820mA for a time duration of leass then or equal to 250uSec."

Notes (an other reasons why 820mA, 50msec, 5% duty is a good thing):
1. This is not a positive current transient caused by PSE dv/dt. It is cuased by PSE voltage drop.
Per other comments, Tcut min. should be 50msec min. so this requiremnet for 820mA , 250usec is already covered.
3. PD shall not limit its input below 820mA for 250usec duration.
Per other comments PD may require 820mA for max. 50msec , 5% max duty cycle.

Proposed Response *Response Status* **O**