Cl **00** *SC* **0** *P* *L* # 265

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

I believe that w emay be adding new difinitions and references.

For example Type 1 and Type 2 PSE and PDs. Also, Is ANSI/TIA 1057 already referenced in Clause 1?

SuggestedRemedy

Please add additions and changes to Clause 1

Response *Response Status* **C**

ACCEPT.

Cl **00** *SC* **0** *P* *L* # 222

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A** *ez*

Please make the page numbers at the bottom on the page (printed) and the pdf numbers the same. This will eliminate confusion in commenting.

SuggestedRemedy

I would be happy to wokr with the Chief Editor to make this happen using Framemaker

Response *Response Status* **C**

ACCEPT.

Cl **00** *SC* **0** *P* *L* # 233

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A**

Im assuming that we will modify Clause 30 as well for management

SuggestedRemedy

Need specific suggested remedy or editorial instructions. Someone will need to take on the task to edit Clause 30.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

assigned to David Law

Cl **00** *SC* **0** *P* *L* # 245

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

Where is the statement and what sections are covered by the resolution to comment 80 which stated

"Editor to incorporate Hugh's text as an addition to 33.6 and recirculate with next draft. Also, add note before section stating that text has not been accepted by 75% of TF."

SuggestedRemedy

Please clarify what text is new and NOT adopted by 75% at beginning of meeting and if we do not get around to adopting this text or a version of it for next draft, please include editor's note per resolution to comment 80 from D0.8

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

editor to add note to 33.6, and to Hugh's text moved outside of 33.6.

Cl **00** *SC* **0** *P* *L* # 248

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

All values in this table that are dependent on the underlying maximum current should be stated as such until we have a final resolution there.

SuggestedRemedy

Please state all parameters that are dependent on the DC current as a percentage of that.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE 182, 247

Cl **00** *SC* **0** *P* *L* # 257

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

The deleted diagrams Figs Figure 33–9a and Figure 33–12b are useful illustrations of how link layer works even though they are not normative state diagrams.

SuggestedRemedy

Create an informative annex showing these diagrams as example of link layer behavious

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Create Informative Annex 33F and place in Annex 33F
drawings on page 21 and 40.

Cl **00** *SC* **0** *P* *L* # 252

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

There is a subtle inconsistancy between the classification baseline we adopted and the draft. Specifically, the PD can only expect to see a maximum of 12.95W from the PSE while it waits for the L2 mechanism to come up. The issue in the draft is in several places describing this process it says that the PSE will treat a class 4 PD as it would under HW classification until the L2 engine is up. If I look at the power tables for HW classification they say 36W not 15.4W!

SuggestedRemedy

Please correct the following:
- In describing what a Type-2 PSE that is L2 capable does please specifically call out the limits to the power to be 15.4W consistant with the adopted baseline
- Please qualify the HW power tables with a footnote to explain when these apply for a Type 4

I will try to point out the descrepencies in other comments and specific locations but if I miss something please use this commeny

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Place a note:

Note- Power must remain within class 0 limits until mutual identification is completed.

Cl **33** *SC* **1** *P* **1** *L* **22** # 223

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A**

Please delete the words "An optional". The mechanism to do .3at allows for either L1 or L2 on the PSE, optional is not the correct indication.

SuggestedRemedy

Please delete the words "An optional".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See 4

Cl **33** *SC* **2** *P* **17** *L* **33** # 159

Law, David 3Com

Comment Type **TR** *Comment Status* **A**

It is not correct to state that all PSEs have to classify the PD. A Type 1 PD can still, optionally, choose not to do this.

SuggestedRemedy

Change '.. classify the PD ..' to read '.. optionally classify the PD ..'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolved by 251

Cl **33** *SC* **2** *P* **3** *L* **33** # 251

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

Deleting the word optional makes the functionality requirement of classification ambigious for Type 1 vs. Type 2

SuggestedRemedy

Append the following sentence to the end of the paragraph: ""The classification function may be optional depending on the Type of PSE""

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

remove "classify the PD" from line 33.

add this to end of paragraph: "In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD."

see 159

Cl **33** *SC* **2.1** *P* **17** *L* **51** # 158

Law, David 3Com

Comment Type **TR** *Comment Status* **A** *midloc*

The text states that 'Midspan PSEs shall use Alternative B when used in 10BASE-T or 100BASE-TX systems'. It then states that 'Midspan PSEs may support either Alternative A or B, or both when used in 1000BASE-T systems'. There is no definition of what a 10BASE-T, 100BASE-T or 1000BASE-T 'system' is, so in the following I will assume that simply it means that the link is operating with that type of PHY at each end.

Many ports these days are 10/100/1000BASE-T capable. Based on this, take the case of a 10/100/1000BASE-T non-PSE switch port that is connected to a Midspan. The Midspan connected to this port will have to be a 1000BASE-T capable Midspan or the link will never be able to operate at 1000BASE-T. The port however may not actually be operating at 1000BASE-T so this would seem to force the Midspan to be Alternative B to meet the mandatory requirement for 10BASE-T and 100BASE-T operation. In fact unless you can guarantee that the link the 1000BASE-T Midspan is connected in will only ever operate at 1000BASE-T, which I do not believe the Midspan has any way to force, the Midspan will have to be Alternative B.

The option of being able to build an Alternative A Midspan therefore seem unusable.

SuggestedRemedy

Either (i) mandate that all Midspans have to be Alternative B or (ii) allow 10BASE-T and 100BASE-T Midspans to be Alternative A as well as Alternative B. I suggest the second option on the basis that if it has been proved that 1000BASE-T Alternative A Midspans can be built while maintaining the link segment requirements they should be permitted for 10BASE-T and 100BASE-T operation as well. If this has not been proved then my first option has to be used.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change text "Endpoint PSEs may support either Alternative A or B, or both. Midspan PSEs shall use Alternative B when used in 10BASE-T or 100BASE-TX systems. Midspan PSEs may support either Alternative A or B, or both..."

to:
PSEs may support either Alternative A or B, or both.

see 207, 154

vote:

Y:20, N:0

Cl **33** *SC* **2.1** *P* **19** *L* **38** # 154

Law, David 3Com

Comment Type **TR** *Comment Status* **A** *midloc*

We seem to now have defined two 'types' of Midspan PSEs which are not interchangeable, a 10/100BASE-T Midspan which does not provide continuity on the spare pairs (see Figure 33-4), and a 1000BASE-T Midspan that does (see Figure 33-4a). Combine that with Types of PSE defined in 33.2.2a and we have a total of four types of Midspan:

10/100BASE-T Type 1 Midspan PSE
1000BASE-T Type 1 Midspan PSE
10/100BASE-T Type 2 Midspan PSE
1000BASE-T Type 2 Midspan PSE

Now I note that there is a statement in subclause 33.4.8 that 'A Midspan inserted in a channel shall provide continuity for the signal pairs'. I'm not sure if that is a contradiction to Figure 33-4 10/100BASE-T Midspan PSE Alternative B which shows no continuity on two of the four pairs.

SuggestedRemedy

Add a new subclause that clearly defines that where each type of Midspan can and cannot be used. Suggest a new subclause 33.2.1a as follows:

33.2.1a Midspan PSE types

There are two types of Midspan PSE defined.

10/100BASE-T Midspan PSE
A Midspan that will result in a link that can only support 10BASE-T and 100BASE-T operation (see Figure 33-4). Note that this limitation is due to the presence of the Midspan regardless if it is supplying power or not.

1000BASE-T Midspan PSE
A Midspan that will result in a link can support 10BASE-T, 100BASE-T and 1000BASE-T operation (see Figure 33-4a)

Response *Response Status* **C**

ACCEPT.

see 158, 207

Cl **33** *SC* **2.1** *P* **3** *L* **52** # 279

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *midloc*

There is nothing to prevent a 100BASE-TX device from being plugged into a midspan that implements Alt. A. Implementations of an Alt. A midspan may interfere with a 100BASE-TX PHY implementation that rely on the link partner's output inductance as required by the specification.

SuggestedRemedy

Either disallow implementations of Alt A OR Insert the following statement: "Midspans implementing Alternative A shall not interfere with the data performance of a 100BAE-TX link, specifically as it relates to the output inductance requirement. This shall apply regardless of power being applied (i.e. when power is privisoned and when it is not).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add this text:
Note - Midspans implementing Alternative A are not allowed to interfere with the data performance of a 100BASE-TX link. This applies regardless of power being applied. Refer to Clause 25 for 100BASE-TX compatability requirements.

Cl **33** *SC* **2.1** *P* **7** *L* **1** # 70

Patoka, Martin TI

Comment Type **TR** *Comment Status* **A** *fig33-4*

Figures 33-4b
Figures are drawn showing the PSE connecting power to all 4 pairs, even though figures are labelled alternative A andd B.

SuggestedRemedy

Remove connections within PSE block to show only one pair powered.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolved by 250

Cl **33** *SC* **2.10.1.2** *P* **32** *L* **11** # 17

LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **A**

Resistor value is not printed correctly. The spec. in Table 33-6 says the impedance should be greater than 1980k, not a std. resistor value and tolerance.

SuggestedRemedy

Resistor value should be " >1980 kohms"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Delete Rpd and number in drawing

Cl **33** *SC* **2.3.7** *P* **13** *L* **4** # 125

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *fig33-6*

It is not clear from the PSE state diagram that detection phase always starts form IDLE state in which the PSE is at OFF mode.
OFF mode is the PSE mode were the average voltage at the PI is <=2.8V.

Any other possibility may end with invalid detection even if the PD has valid signature elements.
e.g.: The PSE did detection and for some reason system decided to not power the port and to issue additional detection phase.
In this case the port voltage may be >2.8V which may cause invalid detection results this loop can go forever and the port may never be ON.

SuggestedRemedy

Add text that requires the following:

Between two consecutive detection attempts, the PI shall gone through OFF mode as defined by table 33-5 item 13b.

Equivalent wording is possible.

Add text that requires the following:

Between two consecutive detection attempts, the PI shall gone through OFF mode as defined by table 33-5 item 13b.

Equivalent wording is possible.

The task force members are encourage to check if the proposed fix may reduce implementation flexibility.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The text does not match the state diagram.

Change 33.2.8.10:

from:
"The PSE enters the IDLE state when VPort drops 1 V below the steady-state value after…"

to:
"Toff starts when VPort drops 1 V below the steady-state value after…"

add new sentence following above change:
"Toff ends when Vport <= Voff."

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 161

Law, David — 3Com

Comment Type **TR** *Comment Status* **A** *33.2.7*

[a] It is difficult to follow the various different types of classification we now have, and there is no overall introduction to guide the reader to what options there are and what features each option provides. There should be a broad introduction to all types of classification, and introduction to each specific type of classification then finally the details of the operation.

[b] Subclause 33.2.7 PSE Hardware classification of PDs' currently states that 'A PSE may remove power to a PD that violates the maximum power required for its advertised class.' which implies this only applies to hardware classification and that if a PD violates the maximum power it advertised through Link Layer classification it isn't permitted to do this. I don't believe this is correct and it is just as valid to do this for Link Layer classification. This text should therefore be moved so that it applies to all classification methods. See also other comment on this text.

SuggestedRemedy

Suggest that:

[1] Subclause 33.2.7 become an introductory clause that reads:

33.2.7 PSE classification of PDs

The ability of a PSE to classify a PD allows features such as load management to be implemented. There are two forms of classification, hardware classification and optional link layer classification. Hardware classification allows a PSE to classify a PD into one of a limited number of granular classes, this classification occurs once after a PSE successfully completes detection of a PD. Link layer classification allows a more granular classification that the initial hardware classification, this classification occurs continuously and provides the ability for the PD classification to change.

A PSE may remove power from a PD that violates the maximum power it has advertised it requires. This maximum power is initially derived from the advertised class during hardware classification and then, if implemented, subsequently updated by link layer classification.

[2] A new subclause 33.2.7.1a be inserted that reads:

33.2.7.1 PSE hardware classification of PDs

There are two types of hardware classification dependant of the PSE type, Type 1 hardware classification and Type 2 hardware classification.

A Type 1 PSE may optionally perform hardware classification. If a Type 1 PSE does perform hardware classification it shall use Type 1 hardware classification (see 33.2.7.2). If a Type 1 PSE does not classify the PD using hardware classification, then the Type 1 PSE shall assign the PD to Class 0.

A Type 2 PSE shall perform hardware classification and shall use Type 2 hardware classification (see 33.2.7.2a). This is to ensure that a Type 2 PSE implementing only

hardware classification can indicate its presence and identify the Type 2 PD's power requirements.

A successful hardware classification of a PD requires:

a) Successful PD detection, and subsequently,
b) Successful Type 1 or Type 2 Class 0-4 hardware classification.

The PSE hardware classification circuit should have adequate stability to prevent oscillation when connected to a PD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

[1] Subclause 33.2.7 become an introductory clause that reads:

33.2.7 PSE classification of PDs

The ability of a PSE to classify a PD allows features such as load management to be implemented. There are two forms of classification, hardware classification and optional link layer classification. Hardware classification allows a PSE to classify a PD into one of a limited number of granular classes, this classification occurs once after a PSE successfully completes detection of a PD. Link layer classification allows a more granular classification that the initial hardware classification, this classification occurs continuously and provides the ability for the PD classification to change.

A PSE may remove power from a PD that violates the maximum power it has advertised it requires. This maximum power is initially derived from the advertised class during hardware classification and then, if implemented, subsequently updated by link layer classification.

[2] A new subclause 33.2.7.1a be inserted that reads:

33.2.7.1 PSE hardware classification of PDs

There are two types of hardware classification dependant of the PSE type, Type 1 hardware classification and Type 2 hardware classification.

A Type 1 PSE may optionally perform hardware classification. If a Type 1 PSE does perform hardware classification it shall use Type 1 hardware classification (see 33.2.7.2). If a Type 1 PSE does not classify the PD using hardware classification, then the Type 1 PSE shall assign the PD to Class 0.

[editors note: text introducing HW mechanism used by a Type 2 PSE to be added at a later date.]

A successful hardware classification of a PD requires:

a) Successful PD detection, and subsequently,
b) Successful Type 1 or Type 2 Class 0-4 hardware classification.

The PSE hardware classification circuit should have adequate stability to prevent oscillation when connected to a PD.

Cl **33** *SC* **2.7** *P* **17** *L* **33** # 172

Jones, Chad Cisco

Comment Type **ER** *Comment Status* **A** *33.2.7*

This sentence is the first appearance of Data Link Layer classification in the text and it is not defined.

SuggestedRemedy

Add the sentence: "Data Link Layer classification is a layer 2 protocol. Details can be found in section 33.6." after the paragraph.

Response *Response Status* **C**

ACCEPT.

see Law 170, incorporate

Cl **33** *SC* **2.7** *P* **17** *L* **47** # 249

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *33.2.7*

There is a should statement here without a PICs. Specifically, the sentence "The PSE hardware Physical Layer classification circuit should have adequate stability to prevent oscillation when connected to a PD."

SuggestedRemedy

One of the following 3 suggestions:
- Either delete the statement all together OR
- Make this a note and remove the word should
- Add a PICs and test associated with this

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

make it a note

Cl **33** *SC* **2.7.2a** *P* **19** *L* **22** # 194

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **R**

The intent of the sentence is not clear: "If at any point the classification sequence the PSE allows the voltage at the PI to enter the VRESET range as defined in Table 33-4a, the PSE shall classify the PD as Class 0."

The intent appears to require that the PSE and PD remain synchronized. If the PSE causes a reset the PSE should assume the PD has been reset. It takes time for the PSE/PD to sense the reset condition.

SuggestedRemedy

Clear outline the requirements and purpose.

Response *Response Status* **C**

REJECT. see 132, 103

Cl **33** *SC* **2.7.2a** *P* **19** *L* **25** # 119

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A**

Drfat0.9:
According to the current text the PSE is required to measure the class current and the mark current.
It looks that it is not cost effective and not technically required to measure it twice over the time domain with short time intervals.
It is sufficient to measure Iclass and check its value if it match one of the values of the class current or if it is > Iclass-_lim.
It is not important if I>Imark_lim due to the following reasons:
1. It is not cost effective to measure Imark_lim with in 6-12msec time frame just after that Iclass has been measured.
2. At the worst case if Imark_lim is wrong and cause Vmark to be out of range, then it will be reflected to a bad class reading which will be handled by the PSE anyway so it is redundant measurement and technically difficult one.
3. Imark timing is PD dependent and PSE will have difficulties to guess where and when to measure especially in multi-port systems where many operations are done in parallel to others.
4. And most important the need for measuring Imark is not required by the concept for we choose proper operation.

SuggestedRemedy

1. Delete the need for measuring Imark from the PD state diagram and the normative text in page 19 lines 24-29.
2. Use the parameter of Iclass_lim_max for the entire classification period with the same max. value i.e. 100mA max for the class and mark time duration.
3. Set Imark_lim_min to 5mA (to have margin from Imark_max=2mA)

Response *Response Status* **C**

ACCEPT. see 133

Cl **33** *SC* **2.7.2a** *P* **19** *L* **28** # 118

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A**

Draft 0.9:

When PSE classify the PD after Iclass_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to adress this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset=5 to 30msec (TBD).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Classification AdHoc to address issue and suggest remedy.

No change in text results.

Cl **33** *SC* **2.7.2a** *P* **19** *L* **45** # 253

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **A**

I like the note. I would suggest that we have a default in case this case happens for some error in the system. Undefined behaviour is scary

SuggestedRemedy

I would suggest that the whole detection process is restarted and no power is applied if the 2 results are different.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

remove the word "Note-" at the beginning of line 45.
If a Type 2 PSE observes mixed results, it shall return to the idle state.

Make state machine reflect this behavior.

Cl **33** *SC* **2.7.2a** *P* **20** *L* **12** # 27

LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **A** *t33-4a*

IMark_LIM is unnecessarily restrictive. It should encompass both classification circuit and detection circuit current limitations for maximum implementation flexibility.

SuggestedRemedy

Change to IMark_LIM min 5mA, IMark_LIM max 100mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. see 135

Cl **33** *SC* **2.7a** *P* **21** *L* **3** # 246

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

We still need to have a section on Link Layer here. I believe the material in 33.6 is intended to complement 33.2.7a (or whichever way we end up renumbering it) even if it is a reference to a later section. Otherwise its confusing.

For example, the timing relation between the data-link layer and the Type 1 physical layer needs to be defined and described

SuggestedRemedy

See Comment. We need to have a control section in addition to the management section.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Create Normative Annex [different from Informative 33F]. Place 33.6.2 and 33.6.3 in this new normative annex.

Place a copy of 33.6.4 under DLL classification for PSE and PD under headings 33.2.7a and 33.3.4a. (need to place editors note from comment 245 here also)

Retain register changes related to DLL in 33.6

Any management attributes to be moved to clause 30.

Cl **33** *SC* **2.8** *P* **25** *L* **15** # 187

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **A** *t33-5*

The specification requires that a PSE remove power based on ILIM and TLIM thresholds. The selected levels are not required to ensure interoperability or meet the safety specifications, and therefore, are unnecessarily restrictive.

SuggestedRemedy

A PSE system needs to operate within the region between PD current needs (TBD) and SOA current limits (current limit and duration).

Allow existing ILIM requirements or current requirements derived from figure 33-9a SOA requirements.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **2.8** *P* **25** *L* **15** # 107

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-5*

Draft0.9:

Table 33-5 item 10:
Replace TBDs with numbers or figure 33-9a data.

SuggestedRemedy

1) ILIM_MAX=SOA curve.
2) ILIM_MIN=Icable * (400/350)

3. Add the following text to 33.2.8.8 after line 45:
"Minimum ILIM for Type 2 PSE when implementing constant current limit shall be 870mA minimum in order to support the scenario of positive PSE dv/dt which cause to PSE to be at ILIM simultaneously when PD is consuming 820mA for up to 50msec.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

1) ILIM_MAX= (blank).
2) ILIM_MIN=(Pport/Vport) * (400/350)

Cl **33** *SC* **2.8** *P* **25** *L* **16** # 109

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **R** *t33-5*

Draft0.9:

Table 33-5 item 11.

Type 1 and Type 2 PSEs may have different TLIM_MIN and TLIM_MAX.

SuggestedRemedy

1. Split item 11 to type 1 and type 2 PSE.
Updated numbers/curves will be supplied by the Vport ad hoc.

2. Update 33.2.8.9 accordingly.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Will recomment after section is updated in next draft.

Cl **33** *SC* **2.8** *P* **25** *L* **23** # 182

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A** *t33-5*

All references requiring a PSE to provide 15.4 W/(TBD AT power) minimum do not match the state diagram shown in figure 33-6. Also see p26, l31 and 32; p70, PSE37.

SuggestedRemedy

In all cases, the PSE provides the power the PD requests or it does not power the PD. The power provided is Pport.

table 33-5, item 14 can be deleted;

33.2.8.4, p26, l31-32, and p26, l49-50, replace numerical value with Pport;

P70 PSE36, replace numerical value with Pport. This assumes the PSE can provide only Pport and not provide the maximum allowed by the standard.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

replace table 33-5, item 14 with Pclass
Pclass is the power defined in 33.2.7 or the result of DLL class as defined in 33.6.

33.2.8.4, p26, l31-32, and p26, l49-50, replace numerical value (15.4W and 36W) with Pport;

Cl **33** *SC* **2.8** *P* **25** *L* **38** # 105

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-5*

Draft0.9:
1. Classification time Tpdc for type 1 and 2 PSE's are different.

SuggestedRemedy

Split item 20 in table 33-5 for type 1 and type 2 PSEs:

Add the following data for type 2 PSE:
Tpdc min. = 12mesec for PSE using layer 2 which uses only single finger.
Tpdc max.= per the max. values in table 33-4a.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Split item 20 in table 33-5 for type 1 and type 2 PSEs:

Leave type 1 as is.
Add the following data for type 2 PSE:
point to table 33-4a.

Cl **33** *SC* **2.8.12** *P* **29** *L* **1** # 188

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A**

The current imbalance requirements need to be reevaluated for PoE plus levels. For example, the main source of imbalance is connector resistance. This same resistance is now over a much lower channel resistance and this will cause a larger than 3% current imbalance.

Millions of PoE ports are in use with cable lengths significantly less than 80 m (the value used to determine the legacy 3% imbalance value). A short cable length increases the current imbalance to levels where many transformers can not guaranty the 350uH inductance requirement of IEEE 802.3 yet ports continue to operate as expected. Therefore, assumptions made by the IEEE should be re-evaluated.

SuggestedRemedy

A transformer ad hoc should be formed to create system requirements for Ethernet transformers that ensure compliant systems are acceptable to the broader market.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

AdHoc will be created. Fred will chair the AdHoc.

Cl **33** *SC* **2.8.4** *P* **26** *L* **36** # 183

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A**

The statements are not clear: is "a" or "b" required?
Option "b" has no time or duty cycle constraint provided. These comments also apply to the new section 33.2.8.4a.

SuggestedRemedy

Allow options "a" or "b."
Have one statement for duty cycle and time that applies to both "a" and "b".

The same comments apply to section 33.2.8.4a and table 33-12.

See a related comment on section 33.3.5.4.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
a) Ipeak = 0.4A minimum for 50ms minimum and 5% duty cycle minimum.
b) For VPort > 44V, Ipeak = 17.6 W/VPort.

To:
Ipeak = (17.6 W/Vport) minimum for 50ms minimum and 5% duty cycle minimum.

Do similar for 33.2.8.4a

Cl **33** *SC* **2.8.4a** *P* **26** *L* **49** # 120

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-5*

The behavior of Type 1 PSE should be similar to the behavior of type 2 PSE in terms of supporting ac current waveforms parameters (Similar PDs environment just more power, similar application load accuracies, similar circuit tolerances and margins..).

The concept in type 1 is working well and do not increase the burden on PSE Power Supply due to the fact that the specification requires that the average current and the rms current will be the same number which is equal to the max. DC operating cable current i.e. 720mA which is the same concept used in Type 1.
Therefore no additional power is required from the PSE PS hence no additional cost. We just improved system robustness for PD load dynamic changes which exceeds max. DC current for limited time duration and duty cycle.

The above is a physical fact.

See 802.3af documentations/presentations more details.
See contribution sent to 802.3at task force for September 2007 meeting which summarize this issue again.

SuggestedRemedy

In 33.2.8.4a:
Change TBD in item a line 49 to 823mA. (or 820mA)
Change TBD in item b LINE 50 to 36*0.4/0.35=41.14W

Table 33-5:
Item 10 for type 2 minimum value: Change TBD to 820mA min.

Table 33-12 item 4:
Change TBD max. value to 820mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In 33.2.8.4a:
Change TBD in item a line 49 to Icable * (400/350).
Change TBD in item b LINE 50 to Pport* (400/350)

Table 33-5:
resolved by 107.

Table 33-12 item 4:
Change TBD max. value to Icable * (400/350).

Cl **33** *SC* **3.1** *P* **34** *L* **10** # 173

Jones, Chad Cisco

Comment Type **ER** *Comment Status* **R** *pdtype*

This is the first time Data Link Layer classification if referenced in the PD section and it is not defined.

SuggestedRemedy

Add the sentence: "Data Link Layer classification is a layer 2 protocol. Details can be found in section 33.6." after the paragraph.

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33** *SC* **3.1a** *P* **34** *L* **10** # 210

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **A** *pdtype*

Change the following text for clarity:
"Type 2 PDs shall implement both Type 2 hardware Physical Layer classification and link layer Data Link Layer classification. This limits the maximum power a PD may expect to draw from a PSE to 29.5 W."

SuggestedRemedy

To:
"Type 2 PDs implement both Type 2 hardware Physical Layer classification and link layer Data Link Layer classification. The maximum power a PD may expect to draw from a PSE is limited to 29.5 W."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.1a** *P* **34** *L* **11** # 255

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *pdtype*

29.5W is not an accurate number for the PD based on the information to date. The maximum power available to the PD is dependent on the maximum current which is dependent on the ambient temprature of the cables.

For example, a PD that is connected to a PSE with cabling that is at an ambient temperature higher than 45C can not reliably depend on 29.5W. The 29.5W is a maximum at a point on the curve. This implicitly assumes that 802.3at will NOT support ambient temperatures that are higher than 45C on the cabling, which we have not decided yet.

We need to deal with this issue prior to setting maximums / minimums in the spec.

This comment should apply to all references of maximum power for the PD

SuggestedRemedy

Delete the 29.5W and/or explictly state that 802.3at will not support temperatures above 45C.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29 and 247

Cl **33** *SC* **3.1a** *P* **48** *L* **7** # 209

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **A** *pdtype*

Change the following text for clarity:
"Type 1 PDs may optionally implement Type 1 hardware Physical Layer classification. This limits the maximum power the PD may expect to draw from a PSE to 12.95 W."

SuggestedRemedy

To:
"Type 1 PDs expect to draw from a PSE to 12.95 W and do not have Layer 2 classification. They may optionally implement Type 1 hardware Physical Layer classification."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE. See comment 29

Cl **33** *SC* **3.2** *P* **36** *L* **6** # 189

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A** *t33-12a*

Figure 33-12a needs to be redrawn to meet IEEE state diagram requirements.

SuggestedRemedy

Request the L1 ad hoc to create the state diagram.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See Editor's report.

Cl **33** *SC* **3.4a** *P* **40** *L* **1** # 256

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **A**

We still need to have a section on Link Layer here. I believe the material in 33.6 is intended to complement 33.3.4a (or whichever way we end up renumbering it) even if it is a reference to a later section. Otherwise its confusing

SuggestedRemedy

See Comment. We need to have a control section in addition to the management section.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE

Cl **33** *SC* **3.5** *P* **42** *L* **22** # 53

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **A** *t33-12*

Table 33-12 item 3: see also 33.3.5.3 p43 line 46.

The term inrush is not defined.

SuggestedRemedy

Add statement similar to the following to 33.3.5.3:

Inrush current is drawn during the startup period beginning with the application of input compliant with table 33-12 Vport requirements, and ending when Cport is charged to within 99% of its final value. This period must be less than Tlim min per table 33-5.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **3.5** *P* **42** *L* **32** # 112

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-12*

Draft0.9:
Table 33-12 item 4:
Project objective was to deliver 30W to the PD.
In order to achieve this objective we set a 720mA max. DC current.
In order to utilize the full power capability derived from 720mA or any average current we need to allow some ac wave form to coexist on top of the DC level in order to handle the following input parameters:
a) Application circuit components accuracy limitation
b) PD DC/DC converter components accuracy
c) Application load variations

This concept was succesfully used in 802.3af without additional complexity or cost due to the fact that the specification requires also from the PD vendor to keep the RMS and the DC value not to excceed the same number i.e. 350mA and in our case is 720mA. Threfore there is no additional power consumption beyond the max. power specifyied.

Regarding the issue of supporting PSE current transient due to dv/dt simultaneously with PD peak current=823mA when PSE is using constant current limit near Icut_max so net charging current is zero, the following solution is suggested:
When using constant current limit the PSE vendor will set ILIM_MIN = PSE'S icut_max + Margin.
The margin is the current required to charge Cpd (<50mA).

Other alternative would be to minimize th erequirements from the standard it is a PSE issue and not system issue hence no interoperability risk that requires the standard to adress both PSE and PD.
Rational:
1. It is enugh to define that PSE is required to support current transients due to PSE dv/dt up to 7V at a slew rate of TBD. At this point it is depened only at the PSE how to implement this support. The PD is not a player that need to be defined. It is already defined by Cpd=180uF.

If PD is usig up to 180uF and PSE dv/dt is limited to 7V then the peak current and its duration are both function of PSE implementation. If PD input capacitor is > 180uF then the PD is responsibble to limit the current at its input to Icut_max.

2. If PSE choose to implement energy based current limit, then it will work within the 2A peak and 3msec time as suggested by the Vport_ad hoc.

3. If PSE choose to use constant current limit, it will choose the correct ILIM and TLIM_min pairs to maintain th eport at ON state for TLIM_MIN.

4. There is no issue with PD application load transient current due to the fact that per the concept of type 1 PD which is suggested for type 2 PD as well, the max peak current at the PD is Icut_max and it is limited to 50msec, 5% duty cycle max.
In addition, in previous commnet, it was shown that in any case the system will get to

820mA for 250usec when PSE voltage is droped by 7.6% (46.2V) per table 33-5 item 2a so in any case PD may work at 820mA and PSE shall support it by setting minimum ILIM=820mA + Margin.

5. There is no added cost as was proven in 802.3af:
5.1 The max. average current is always 720mA (350mA in 802.3af)
5.2 The max. RMS current is 720mA rms. (350mA in 802.3af)
Hence no additional resistive loss in the system.
5.3 As aresult the total average power is always 29.5W max. (12.95W in 802.3af)
5.3.1 The specification is explicetly defines that the total PD input power shall not exceed Pport_max 12.95(/29.5W) average over 1sec.

SuggestedRemedy

Itme 4: Peak operating current at class 4 for type 2 PD:

Ipeak = 0.72A*0.4/0.35 = 0.823A. (Same Icut/Iport ratio as in 802.3af)
Number may be rounded to 820mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE

see 270, 274, 277, 278

Cl **33** *SC* **3.5.2** *P* **43** *L* **23** # 192

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **A**

Some people are confused how to calculate duty cycle.

SuggestedRemedy

In a note state that duty cycle shall be calculated using a sliding window with a 1 second width around any level above Pport_max/Vport.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Insert a note stating that duty cycle shall be calculated using any sliding window with a 1 second width.

Cl **33** *SC* **3.5.2** *P* **43** *L* **26** # 146

Law, David 3Com

Comment Type **ER** *Comment Status* **A**

Please follow the correct format for equations define in the IEEE Style guide [http://standards.ieee.org/guides/style/2007_Style_Manual.pdf#Page=29]. Additional formatting information can be found at [http://www.ieee802.org/3/tools/editorial/requirements/scc14.html].

In addition for these specific equations it is not clear that the measurement using 20 Ohms for type 1 and 12.5 Ohms for Type 2 are mandatory. If they are, as I suspect they are, they should be shall statements.

SuggestedRemedy

This formatting needs to be carried on the entire draft or there is the possibility that SCC14 may try to force these changes during sponsor ballot and RevCom submittal - SCC14 is a mandatory coordination [http://standards.ieee.org/faqs/coor.html].

In this particular case the equation should be changed as follows:

[1] The text 'where:' followed by a list of variables with their definition should be provided.

[2] The letter symbols for physical quantities, mathematical variables, indices and general functions (as opposed to mathematical functions), are always printed in italic. In this case P, V and I should be italic. Subscripts and superscripts follow the same rules. Symbols for physical quantities, mathematical variables, indices and general functions are printed in italic. Therefore in this case 'Port' should be in upright font as it is not a symbol for a variable.

To address the measurement specification issue the resistances should be included in shall statements. This subclause would therefore read:

The specification for PPort in Table 33-12 shall apply for the input power averaged over 1 second. For a Type 1 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 20 W in series. For a Type 2 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 12.5 W in series. PPort is defined as:

PPort = VPort x IPort

where

PPort is the input average power
VPort is the input voltage
IPort is the input current, either DC or RMS

See the file P802p3at_sub_33p3p5p2.FM supplied with comment file for full formatting example.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The advice given at the two urls will be followed by the editor.

Cl **33** *SC* **3.5.2** *P* **43** *L* **26** # 199

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A**

Fix the typo.

SuggestedRemedy

Replace "44 V to 57 V" with "50 V to 57 V." Consider placing all numerical values in one table and referring to them using a variable. This would ensure that numerical values appears in only one place in this specification.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. see 176,

Cl **33** *SC* **3.5.7** *P* **45** *L* **8** # 171

Jones, Chad — Cisco

Comment Type **ER** *Comment Status* **A**

This paragraph is redundant with 33.3.5.1 and these are redundant shalls.

SuggestedRemedy

Either delete the paragraph under 33.3.5.1 or move the last sentence of 33.3.5.7 to 33.3.5.1 and delete 33.3.5.7.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Move last sentence of 3.5.7. to 3.5.1 and change reference in item 8 of table 33-12 to see 33.3.5.1

Delete section 33.3.5.7

Cl **33** *SC* **6** *P* **57** *L* **2** # 123

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **A**

PDs that requires more then 12.95W has a name. It is called type 2 PDs and they are classified as Class 4 PDs.

SuggestedRemedy

Change from:

"....PDs that require more then 12.95W shall.."

To:

"Type 2 PDs shall.."

Response *Response Status* **C**

ACCEPT. see 239

Cl **33** *SC* **6** *P* **57** *L* **2** # 259

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **A**

I believe our plan is to use 802.1ABREV not 802.1AB

SuggestedRemedy

Please correct the reference to relfect the revised version of 802.1AB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

change "802.1AB" to "IEEE Std 802.1AB-200x (Note: the 2005 version is currently under revision. We will reference the revised version.)"
Editors note: update this during preparation for publication.
see 263

Cl **33** *SC* **6** *P* **57** *L* **2** # 239

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **A**

This should ready Type 2 PDs to be consistant with the rest of the draft

SuggestedRemedy

Please rewrd the following:

"PDs that require more than 12.95 W"

TO

"Type 2 PDs"

Response *Response Status* **C**

ACCEPT. see 123

Cl **33** *SC* **6.1.1** *P* **57** *L* **33** # 197

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **A**

Correct the typo in table 33-15, bit 11.4.

SuggestedRemedy

Changed the bit value to 0 for the disabled state.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **6.2** *P* **61** *L* # 241
Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A**

Some of the text in section 33.6.2 and its subsection is not correctly marked according to the convention used by the editor. For example 33.6.2.2 is new material from 802.3-2005

SuggestedRemedy

Pls. mark text according to convention w.r.t 802.3-2005, D0.8 etc.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **6.2** *P* **61** *L* **25** # 263
Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

I believe our plan is to use 802.1ABREV not 802.1AB

SuggestedRemedy

Please correct the reference to relfect the revised version of 802.1AB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

see 259

Cl **33** *SC* **6.2** *P* **61** *L* **33** # 264
Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

We are referencing material in an Annex that is not created yet (33F)

SuggestedRemedy

Please delete text or insert editorial note to indicate that this text is pending Annex 33F

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE

Cl **33** *SC* **7** *P* **66** *L* **1** # 232
Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A**

Please update PICs

SuggestedRemedy

Please update PICs OR Please add an editors note at the beginning of the PICs section stating that these are innaccurate until the normative text is near complete.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add editors note that PICs aren't accurate and to not comment on this section yet.

Cl **33** *SC* **7.3.3** *P* **72** *L* **35** # 55
Patoka, Martin TI

Comment Type **ER** *Comment Status* **R**

Table item 11 for PD does not reflect PD type 2 capability. Also, other T2 characteristics not accounted for

SuggestedRemedy

PD 11 recomends this for type 1
PD11a added for T2 PDS to present Class 4 and to handle physical layer 2 class
PD11b added for T2 PD to perform LLDP classification and messaging

Response *Response Status* **C**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **33** *SC* **Figure 33-12a** *P* **36** *L* **1** # 231
Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **A** *t33-12a*

Please redraw Figure 33-12a in Frame. It is difficult to maintain non-frame figures in the 802.3 documents once the group is done. for example, modifications due to maintenance are hard.

SuggestedRemedy

Please redraw using Frame and similar conventions as used in other state diagrams

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **Figure 33-4b** *P* **7** *L* **1** # 250

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *fig33-4*

These figures are not accurate. They are showing 4-Pair power rather than 2-Pair power over the 2 different alternatives.

SuggestedRemedy

Please only show the 2-Pair power attaching to the correct pairs for Alt A and Alt B. Once we have the vote on 4-Pair power, we can go back and remodify these figures if necessary.

Also, please label the pairs to be consistant with Alt A and Alt B.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Editor to delete appropriate wires and add pin numbers to wires.

Cl **33** *SC* **Figure 33-9a** *P* **28** *L* **20** # 114

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **A**

We vote on 820mA and not 720mA at the horizontal part of the curve after 75msec.

SuggestedRemedy

Change from 720mA to 820mA from T=75msec to infinity.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE

Cl **33** *SC* **Table 33-15** *P* **57** *L* **29** # 260

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *dll*

Currently the management object only shows control and status for Physical Layer Classification. Need to add equivelant for Data Link Layer Classification

SuggestedRemedy

Please add the following bit:

"11.5 Enable Type 2 Data Link Layer Classification
1= Type 2 Data Link Layer classification enabled
0= Type 2 Data Link Layer classification disabled
R/W
"

Change the first row, first column from "11.15:5" to "11.15:6"

Insert appropriate description of bit:

33.6.1.1.1b Enable Type 2 Data Link Layer Classification (11.5)
Bit 11.5 controls Type 2 Data Link Layer classification as specified in 33.2.7.2a. A PSE that indicates support for Type 2 Data Link Layer classification in register 12.14 may also provide the option of disabling Type 2 Physical Layer classification through bit 11.5.

A PSE that does not support Type 2 Data Link Layer classification shall ignore writes to bit 11.5 and shall return a value of '0' when read. A PSE that supports Type 2 Data Link Layer classification but does not allow the function to be disabled shall ignore writes to bit 11.5 and shall return a value of '1' when read. The Type 2 Data Link Layer classification function shall be enabled by setting bit 11.5 to logic one and disabled by setting bit 11.5 to logic zero.

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **Table 33-16** *P* **59** *L* **5** # 261

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A**

Currently the management object only shows control and status for Physical Layer Classification. Need to add equivelant for Data Link Layer Classification

SuggestedRemedy

Please add the following bit:

"12.14 Type 2 Data Link Layer Classification Supported
1= PSE supports Type 2 Data Link Layer classification
0= PSE does not support Type 2 Data Link Layer classification
RO
"

Change the first row, first column from "12.15:14" to "12.15"

Insert appropriate description of bit:

Insert section 33.6.1.2.1b:
33.6.1.2.1b Type 2 Data Link Layer Classification Supported (12.14)
When read as a logic one, bit 12.14 indicates the PSE supports Type 2 Data Link Layer classification as defined in 33.2.7.2a. When read as a logic zero, bit 12.14 indicates that the PSE lacks support for Type 2 Data Link Layer classification. If supported, the function may be enabled or disabled through the Enable Type 2 Data Link Layer Classification bit (11.5).

Response *Response Status* **C**

ACCEPT.

Cl **33** *SC* **Table 33-4a** *P* **20** *L* **12** # 115

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **A** *t33-4a*

DraftD0.9:
There is no technical reason to require two current limit thresholds one for Class event up to 100mA and the 2nd is up to 5mA for mark event.

They should be the same number i.e. 100mA max otherwise it will increas PSE costs for no justified reason.
The implemntor can use lower number then 100mA.

SuggestedRemedy

Change item 2b in table 33-4a from 5mA max. to 100mA max.
Change the minimum value of item 2b to 5mA.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. See 135.

Cl **33** *SC* **Table 33-5** *P* **24** *L* **35** # 247

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **A** *t33-5*

720mA does not accurately reflect the minimum current or for that matter the maximum. The contribution for TIA-TR42 ties the maximum current allowed to the ambient temperature. Thus, 720mA is only valid at 45C ambient and not for example at 55C, 57C, 52C, 47C etc. By stating 720mA as the minimum current, we are implicitly restricting the use of 802.3at to 45C ambient on the cables, which would impact our broad market potential.

The cabling community has put a lof of effort into their contribution and we should accurately reflect that in our draft.

SuggestedRemedy

There are 3 possible solutions to this issue:

- If the current framework is to be retained, the accurate minimum would be 0mA and the accurate maximum would be 720mA. This would cover the entire range of operating currents and temperatures. We would then need to decide on how to detect/enforce this and what the PD can rely on and/or if it needs to do power management based on temp.

- Alternately, a designation of variable with the explanation that this is reflective of the ambient temperature in the associated text section to this line item in the table. This would also have the same issues as the above

- Alternately, the group can decide on an acceptable operating temperature that meets the broad market criterea. Based on this we can pick the current level.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Insert section 33.1.4: "To use IEEE 802.3at, the ambient must be 15C below cable rating. Reference ISO/IEC XXXX. The value of Icable is 720mA.
Editors note: these numbers are not final and are subject to further information from the cabling liaisons. Final numbers will require 75% for adoption."

Replace all references, direct or indirect to cable current with Icable.