Cl **00** *SC* *P* *L* # 280

NoName

Comment Type **E** *Comment Status* **X**

SuggestedRemedy

Proposed Response *Response Status* **O**

Cl **00** *SC* **0** *P* *L* # 169

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *cable*

The objectives state that we will support ISO/IEC 11801-1995 Class D cabling. This cabling is specifies with a maximum loop resistance of 40 Ohms [http://www.ieee802.org/3/at/public/nov06/3n807.pdf] although as stated in this liaison, a high proportion of the 1995 Class D channels are expected to meet the 25 Ohms. DC loop resistance.'.

I believe we have been using a loop resistance of 25 Ohms has been used in our calculations therefore we cannot absolutely claim that we can support ISO/IEC 11801-1995 Class D cabling.

SuggestedRemedy

Options are either:

[1] Change the objectives to state that we support ISO/IEC 11801-1995 Class D with the exception of the 40 Ohm loop resistance, update the draft as appropriate.

or:

[2] Ensure that we have used a 40 Ohm loop resistance in all calculations.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Progress on option one.

This requires no change to the draft.

Cl **00** *SC* **0** *P* *L* # 269

Diab, Wael Broadcom

Comment Type **TR** *Comment Status* **D** *cable*

We need to have a section that discusses PoE+ operation over cable of categories less than Class D

SuggestedRemedy

Insert a section that says something to the effect of

"Operation over cabling systems of Class D or lower is not guranteed"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Type 2 operation on cabling less than Class D is out of scope.

Cl **33** *SC* **1** *P* **23** *L* **10** # 156

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *cable*

I don't believe the draft states anywhere that for Type 2 operation ISO/IEC 11801:1995 Class D cabling or better is required. In addition we need to provide place holders in the draft for the cabling ambient operating temperature derating as well as the bundle size limitation. In respect to these I propose that we choose the third option in [http://www.ieee802.org/3/at/public/may06/law_1_0506.pdf], a fixed derating value.

SuggestedRemedy

Add a new subclause 33.3a 'Cabling system characteristics for Type 2 PSE and PD operation'

Type 2 PSE and PD requires Class D cabling as specified in ISO/IEC 11801:1995. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5e components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995. Additionally:

a) Type 2 PSE and PD operation requires the maximum ambient operating temperature of the cabling to be derated by TBD C.
b) The maximum number of cables in a bundle supporting Type 2 PSE and PD operation is limited to TBD.

Type 2 PSE and PD operation on cabling worse than Class D ISO/IEC 11801:1995 may result in intermittent operation at maximum requested power and is beyond the scope of this standard.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 169

Cl **33** *SC* **1.1** *P* **1** *L* **36** # 224

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **D** *baseline*

These objectives do not include the ones from .3at.

SuggestedRemedy

Please add the 802.3at objectives

Proposed Response *Response Status* **W**

Cl **33** *SC* **1.1** *P* **15** *L* **45** # 157

Law, David — 3Com

Comment Type **T** *Comment Status* **X** *cable*

In the case of Type 2 PSE and PD operation it is no longer correct to state that 'adds no significant requirements to the cabling.' since it will [1] require the use of ISO/IEC 11801:2002 Class D or better base on the objectives, [2] require a limit on the ambient operating temperature of the cabling below that of the cable specification and [3] a limit on the maximum bundle size based on the current liaison information.

SuggestedRemedy

Delete the text 'adds no significant requirements to the cabling.'.

Proposed Response *Response Status* **W**

see 213

Cl **33** *SC* **1.1** *P* **15** *L* **46** # 213

Thompson, Geoff — Nortel

Comment Type **TR** *Comment Status* **X** *cable*

The text:
"Compatibility—Clause 33 utilizes the existing MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification and adds no significant requirements to the cabling."
...is not quite true. To get the full power delivery capabilities of 802.3at the user MUST have a 5e or better cabling system. The difference between that system (25 ohm) and a legacy Cat 5 system can result in as much as a 7% difference in the worst case power available at the PD.

SuggestedRemedy

I do not have remedial text prepared at this point but the draft must make explicit the differences in performance expected from 25 vs. 40 ohm cabling systems.
-OR-
Must do the design entirely based on the worst case cabling (40 ohm) and take the 7% hit on delivered power.

Proposed Response *Response Status* **W**

see 157

Cl **33** *SC* **2.2** *P* **8** *L* **50** # 116

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *4p*

The standard should not preclude implementations that are using both alternative A and B due to the following reasons:
a) It is out of scope of the standard to limit implementations.
b) There are no interoperability issues if PD gets power from two 2 pairs power source. It is the load responsibility (PD) to meet the 2P specification for each 2P. Implementation methods are out of scope of the standard.
c) It is economically feasible as shown in numerous presentations
d) It is technically feasible as shown by the same presentations.
e) There are products in the market that already is using the 2 x 2P implementation e.g. High power Midspan that is using 2 x 2P and applications that are using 2P power coming from the Switch and additional power delivered from Midspan.
f) There is huge market for higher power then 30W over 2P.
g) There is no additional cost issue. The $/watt cost is even lower then in 2P system as shown in previous meeting presentations.
h) For outdoor applications, temperature rise issues of the cables when using 60degC cabling system grade can be solved if the same power is delivered over 2 x 2P which is an easy solution for outdoor applications.
i) Users will do it any way to utilize the full capability of the existing infrastructure.
J) In previous meeting switch and PHY vendors wanted the ability to use the same cable which consists of 4 pairs to support two PDs that each one of them is connected to a 2P system. The current text precludes using this feature.

SuggestedRemedy

Change from:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously."

To:
"A PSE shall implement Alternative A or Alternative B, or both, provided the PSE meets the constraints of 33.2.3. Implementers are free to implement either alternative or both."

In addition in 33.3.1 page 33 line 42 delete "note allowed by" and replace with "out of scope of"

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.3.1** *P* **10** *L* **6** # 6

LANDRY, MATTHEW SILICON LABORATO

Comment Type **E** *Comment Status* **D** *baseline*

Final sentence in paragraph is too long and reads choppily.

SuggestedRemedy

Replace sentence with:

This ensures that a PSE performing detection using Alternative A will complete a successful detection cycle prior to a PSE using Alternative B that might also be present on the same link section and causing the invalid signature.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

See 179

Cl **33** *SC* **2.3.4** *P* **10** *L* **29** # 106

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *baseline*

Draft0.9
During "Short Circuit" Condition i.e. when PSE and PD are no longer at their operating voltage range, there is no technical need to keep PSE port on for TLIM.
It creates many problems such:
1. Prevents meeting item 21 in table 33-5, Ted (Time delay between consecutive start ups.
2. Excessive heat.
See more details in MR #1167.

SuggestedRemedy

To allow the PSE to turn the port to OFF mode when Vport <> Normal operating range at any t<TLIM_MIN.
Remedy steps:
1) Add new variable option_vport_lim to 33.2.3.4. It will be an optional variable.

option_vport_lim
This variable is indicating If PSE port voltage is out of operating range during normal operating mode.
Values:
False: Vport is within the Vport normal operating range as defined by table 33-5.
True: Vport is not within the Vport normal operating range as defined by table 33-5.
3) Add the following text to 33.2.8.8 after item e. Items d and e are resereved for maintanance request 1162).
"f) During short circuit condition, for PI voltages below or above Vport normal operation range as specifiied in table 33-5 the PSE may turn to IDLE state at any time t < TLIM_MIN.
"

4) Change state diagram (figure 33-6) per the attached drawing.

Using this optional variable in the state diagram will fix the problem by changing the inputs to ERROR_DELAY_SHORT state
from: tlim_timer_done
to: Tlim_timer_done + !tlim_timer_done*option_vport_lim*power_applied)

Effect on legacy equipment: None since the variable is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.3.6** *P* **26** *L* **47** # 165

Law, David 3Com

Comment Type **T** *Comment Status* **D** *33.2.7*

See previous comment on default behavior, a Type 1 should default to Class 0, a Type 2 to Class 4.

SuggestedRemedy

Change the text 'Class 0 is returned if an invalid classification signature is detected.' to read ' If an invalid classification signature is detected Class 0 is returned by a Type 1 PSE, Class 4 is returned by a Type 2 PSE.'

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.5** *P* **16** *L* **25** # 57

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *annex*

Table 33-2. Calculation of the signature is not provided (as in 33.3.3), therefore a tolerance is not applicable. Current tolerance is bounded to 0uA, however this is not true of the PD (no minimum, could be -infinite). Since PDs theoretically have a NEGATIVE current intercept, bounding PSE to 0 causes a consistensy problem. Note that Fogure 33C-20 indicates a negative current offset. Current offsetts are cancelled out by the computation methed anyway.

SuggestedRemedy

Recomment setting the PSE tolerance to +/-50uA. Recommend moving figure 33C-20 to this section of normative text, including method of computation, and annotating the current offset on the figure.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.5.1** *P* **16** *L* **31** # 202

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *baseline*

The existing section on PD detection requires specific design requirements that are not necessary to ensure interoperability. Other detection methods have been disclosed: http://www.ieee802.org/3/poep_study/public/sep05/naegeli_1_0905.pdf
The IEEE specification should ensure requirements for interoperability are in place.

This comment may also affect text in section 33.3.3.

SuggestedRemedy

Reference the PD model shown in figure 33-10, and require that the PSE detect values of Rpd_d for all permissible values of Cpd_d as specified in table 33-2.

Remove the text requiring two values but continue to provide guidance for designs that use the two probe method.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7** *P* **17** *L* # 226

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

33.2.7 can be made into the intro section for PSE classification per my next comment. This comment addresses the contents of the introductory section:

There needs to be an introduction that details what a Type-2 PSE can do. Specifically, that it can do either a Dat-Link or Physical Layer classification. It is required to do one or the other. The section can then point to a section (a) that details the Physical Layer Classification and a section (b) that details Data-Link Layer Classification.

Currently, there is no mention of the Link Layer Classification in the openning section. Further it is confusing to get to the Link Layer option

SuggestedRemedy

One way to do this is to retain the paragraph starting at line 43 as teh opening paragraphe. Then:

Please append the following sentence after the current sentence that reads "A Type 2 PSE may* perform hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

"A Type 2 PSE may perform Data Link Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2b."

Please insert the following sentence as the last sentence in the section: "Type 2 PSEs Shall perform either Physical Layer or Data Link Layer Classification"

* Please note that I have asked for a seperate change to the retained paragrpah to include the word "may" in a seperate comment.

Proposed Response *Response Status* **W**

see Law 170
see 227, 49

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 49

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X** *33.2.7*

LL classification was moved to the management section. In order to make the requirements clear, we need to pull together the endspan and midspan requirements. I believe that we should use this paragraph as an overview. Paragraph 33.3.7.2a text (p18 line 34 & ff) should be moved to 2.7. The equivalent of stnaford_1_0707 page 16 should be included as a guide.

SuggestedRemedy

A Type 1 PSE may optionally classify a PD. If a Type 1 PSE successfully completes detection of a PD, and the PSE does not classify the PD using hardware Physical Layer classification, then the PSE shall assign the PD to Class 0.

Type 2 PSEs shall classify to determine the PD type. Endspan PSEs shall perform either Type 2 physical layer classification, or Type 1 Physical Layer classification and Type 2 Link Layer Classification per 33.6. Midspan TYpe 2 PSEs shall perform Type 2 Physical layer classification per 33.2.7.2a.

If a type 2 PSE classifies a type 1 PD, the PSE need only perform the first type 2 hardware classification event. Type 2 Physical Layer and Type 2 Link Layer classification permit mutual classification.

A successful classification of a PD requires:
a) Successful PD detection, and subsequently,
b) Successful Type 1 or Type 2 Class 0–4 hardware Physical Layer classification.
A PSE may remove power to a PD that exceeds the maximum power limit for its advertised class.
A Type 1 PSE performs optional hardware Physical Layer classification of a PD by applying voltage and
measuring current, as specified in 33.2.7.2. A Type 2 PSE performs hardware Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a.
The PSE hardware Physical Layer classification circuit should have adequate stability to prevent oscillation
when connected to a PD.

Proposed Response *Response Status* **W**

see Law 170
see 226,227

Cl **33** *SC* **2.7** *P* **17** *L* **25** # 227

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

This section is very confusing. We dive into Physical Layer classification and then do Data-Link Layer Classification. I would suggest that we make 33.2.7 a general introduction to classification. We then take 33.2.7 and 33.2.7a and make them subclauses of this new geenral section.

For the content of the general section on classification, I will submit a seperate comment (my previous comment in the .csv file).

SuggestedRemedy

I would suggest that we make 33.2.7 a general introduction to classification. We then take 33.2.7 and 33.2.7a and make them subclauses of this new geenral section.

Proposed Response *Response Status* **W**

see Law 170
see 226, 49

Cl **33** *SC* **2.7** *P* **17** *L* **28** # 164

Law, David — 3Com

Comment Type **TR** *Comment Status* **D** *33.2.7*

On the long standing basis that we should be conservative on what we send but liberal on what we receive I think we should state what should be done if classification fails for some reason for both a Type 1 PSE and a Type 2 PSE.

In IEEE Std 802.3-2005 we state 'If a PSE successfully completes detection of a PD, and the PSE does not classify the PD in Class 1, 2, 3, or 4, then the PSE shall assign the PD to Class 0.' Now this text does not state the reason why the PSE does not classify the PD so this seems to apply to [a] a PSE that doesn't perform classification and [b] a PSE that does perform classification but when the classification cycle occurs the values return do not match a value. I believe this is confirmed by the State Diagram (figure 33-6) which states in the do_classification function that definition (subclause 33.2.3.6) that 'Class 0 is returned if an invalid classification signature is detected'.

One approach would seem to be to apply the same approach to IEEE P802.3at, if hardware classification fails regardless of Type treat the PD as a class 0. There is however one edge case if a Type 2 PD has a fault such that a PSE cannot detect it as a Type 2 yet it is still capable of detecting a Type 2 PSE. In this case the PSE would treat it as Class 0 and possibly limit it to 15.4W while the PD having detected a Type 2 PSE will operate as if 36W is available. Based on this I guess the default has to be Class 0 for Type 1 and Class 4 for a Type 2.

SuggestedRemedy

Change the text to read 'If a PSE successfully completes detection of a PD, but the PSE fails to classify the PD as a Class 1, 2, 3, or 4 using hardware classification, then the a Type 1 PSE shall assign the PD to Class 0 a Type 2 PSE shall assign the PD to be a Class 4.'.

Proposed Response *Response Status* **W**

Change the text to read 'If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of the PD, then the a Type 1 PSE shall assign the PD to Class 0 a Type 2 PSE shall assign the PD to be a Class 4.'.

Cl **33** *SC* **2.7** *P* **17** *L* **31** # 180

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *33.2.7*

A PSE does not have to perform Type 2 Physical Layer classification in order to ensure mutual identification with a type2 PD.

SuggestedRemedy

Replace the sentence on line 31 with:

A Type 2 PSE shall perform type 2 Physical Layer classification and/or Data Link Layer classification.

Proposed Response *Response Status* **O**

see 71

A Type 2 PSE shall perform Physical Layer classification or Data Link Layer classification or both.

A Type 2 PSE may implement PL or DLL classification or both.

A Type 2 PSE that does not perform DLL classification shall implement PL classification.

Question:
Should a Type 2 PSE be required to implement PL classification?

Y: 6, N: 9, A: 2

.3 only:

Y: 3, N: 7, A: 1

Question:
Do we reject the comment?

Y: 8, N: 8, A: 2

Cl **33** *SC* **2.7** *P* **17** *L* **31** # 170

Law, David — 3Com

Comment Type **TR** *Comment Status* **D** *33.2.7*

The draft is in conflict with the folowing motions:

March 2006

The IEEE 802.3at Task Force affirms that a PD requiring more than 12.95W will support a Layer-1 Classification extension and a Layer-2 Classification mechanism. Endpoint PSEs must support Layer-2 classification or Layer-1 classification extension for PDs requiring more than 12.95W.

November 2006

Relevant page from diab_schindler_1106_1.pdf:
Simple Classification Baseline
PSE
- AT L2: Detects and classifies class 4. Communicates with PD in L2. Mutual ID achieved.
- AT L1: Detects and classifies class 4. Repeats classification ("dumb ping-pong"). Mutual ID achieved.
- AT PSEs shall choose the classification extension used.
- Legacy PSEs: Unchanged PD
- AT PD: Use class 4 for all 802.3at PDs. After 1st classification, either
- L2 communication which identifies 802.3at endspan
- Second classification ("dumb ping-pong"). Identifies 802.3at midspan
- Power-on after one classification cycle. Identifies legacy PSE
- Legacy PDs: Unchanged
Power Limits after classifying a Class 4 PD
- AT L2 PSEs enforce legacy limit until L2 is up
- AT L1 PSEs enforce maximum power limit per 802.3at objective
- AT PDs operate under class 0 limits until either L2 is up or second class and power-on
- Legacy PDs and PSEs Unchanged

SuggestedRemedy

Update the draft as follows:

Subclause 33.2.7, page 31, line 31.
Change 'A Type 2 PSE shall perform classification using Type 2 Physical Layer classification and may optionally perform Data Link Layer classification.' to read 'A Type 2 Midspan PSE shall perform classification using Type 2 Physical Layer classification and may optionally perform Data Link Layer classification. A Type 2 Endpoint PSE shall perform classification using either Type 2 Physical Layer classification or Data Link Layer classification.'

Subclause 33.2.7, page 31, line 44
Change 'A Type 2 PSE performs Physical Layer classification of a PD ..' to read 'A Type 2 PSE that performs Physical Layer classification of a PD does so ..'.

Subclause 33.2.9, page 43, line 21
Change 'Where a PSE does not provide either of the Physical Layer classification functions specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs.' to read

Where a PSE does not provide Physical Layer classification functions (see 33.2.7), all PDs are treated as Class 0 Type 1 PDs until successful layer Data Link Layer classification is performed.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7** *P* **17** *L* **32** # 71

Patoka, Martin TI

Comment Type **TR** *Comment Status* **X** *33.2.7*

"A Type 2 PSE shall perform classification using Type 2
hardware Physical Layer classification and may optionally perform link layer Data Link Layer classification."

We had a motion November 2006 that a type 2 PSE may choose its extension, which I interpret to mean that an endspan need only perform L2 class. This was recorded in the motion aggregator.

SuggestedRemedy

An Type 2 endspan PSE must perform classification using Type 2
Physical Layer classification or Type 2 Data Link Layer classification. A midspan PSE must perform Type 2 Physical Layer classification.

Proposed Response *Response Status* **W**

see 180

Cl **33** *SC* **2.7** *P* **17** *L* **35** # 117

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *33.2.7*

Draft0.9:
It is not clear from the text that A Type 2 PSE must do at least Type 1 Physical Layer classification in order to read Class 4 PDs that are Type 2 PDs by definition.
Class 4 IS THE UNIQUE IDENTIFICATION MEANS as required by the 5 Criteria.
Therefore:
PSE Type 2 must do at least 1st finger Physical layer classification to read if it class 1,2,3 or 4.
PSE Type 2 may omits the 2nd finger if it is using Layer 2 classification.
A type 2 PDs must implement both Layer 2 AND Physical layer classification.

SuggestedRemedy

Add the following text at line 35:

"Type 2 PSE shall implement at least one classification event of the Physical Layer Classification as per table 33-4a, to uniquely identify if PD is Type 1 or Type 2. Type 2 unique signature is Class 4 and represents PD max. Power.
If PSE is equipped with Layer 2 classification, it may later communicate with PD type 2 for lower PD power requirements"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Class 4 is the unique identifier required for midspans and that is why PDs are required to display class 4, but an endspan PSE can choose to not class the PD at all and use L2 as the mutual identification method. Since PDs are required to do both, the outcome will be full power in both cases.

[pulled out of the 33.2.7.bucket]

Cl **33** *SC* **2.7** *P* **17** *L* **44** # 58

Patoka, Martin TI

Comment Type **T** *Comment Status* **D** *33.2.7*

"A Type 2 PSE performs Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

GIven that an endspan PSE may prefer to do L2 classification, this sentence should be ammended.

SuggestedRemedy

"A Type 2 PSE performs optional Physical Layer classification
of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

Proposed Response *Response Status* **W**

see 180
See 216

Cl **33** *SC* **2.7** *P* **17** *L* **44** # 216

Diab, Wael Broadcom

Comment Type **T** *Comment Status* **D** *33.2.7*

Second sentence needs to have the word may.

SuggestedRemedy

Please rewrite sentence from "A Type 2 PSE performs hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

"A Type 2 PSE may perform hardware Physical Layer classification of a PD by applying voltage and measuring current, as specified in 33.2.7.2a."

Proposed Response *Response Status* **W**

see 180

I disagree that the word may adds any value. See 117 for reasoning. See also 58

Cl **33** *SC* **2.7.1** *P* **18** *L* **1** # 48

Patoka, Martin TI

Comment Type **ER** *Comment Status* **D** *33.2.7*

"Type 2 PDs are required to implement hardware Physical Layer classification so that a Type 2 PSE implementing
only Type 2 hardware Physical Layer classification may simultaneously indicate indicates its presence
and identify identifies the Type 2 PD's power requirements."

This text places a PD requirement in a PSE requirement section.

SuggestedRemedy

Either turn this text into an informational note or strike.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Make it a note - no shall as this is the PSE section. There is a corresponding shall in the PD section.

See 162

Cl **33** *SC* **2.7.1** *P* **18** *L* **11** # 9

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X** *baseline*

Table 33-3 is a bit confusing and could be restructured to provide more informational content.

SuggestedRemedy

Replace Table 33-3 with attached table.

P802d3at_D0p9_table_33d3.fm
P802d3at_D0p9_table_33d3.pdf

Proposed Response *Response Status* **W**

see 163, 244

Cl **33** *SC* **2.7.1** *P* **18** *L* **16** # 163

Law, David 3Com

Comment Type **T** *Comment Status* **X** *33.2.7*

There are Type 1 and Type 2 PSEs, Type 1 and Type 2 PDs, and there is Type 1 and Type 2 hardware classification. It is therefore unclear what the Type values in the 'Usage' column in Table 33-3 is in reference to. It looks like it is meant to refer to PSE type but Type 1 isn't correct in 0 to 3 as classification is optional.

SuggestedRemedy

Consider removing 'Usage' column.

Proposed Response *Response Status* **W**

see 9, 244

Cl **33** *SC* **2.7.1** *P* **18** *L* **27** # 113

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *33.2.7*

Draft0.9:
According to the classification base line concept and associated motions the text should explicitly note that PD that asks more power then advertised in L1 hardware classification is not compliant.

The rational for this was to prevent interoperability issues when a Type 2 PD is connected to end span and get service while if connected to Midspan it will not work due to the fact that Midspan cant support L2.
As a result we mandate PD type 2 to support both L1 and L2 classification and specify that hardware classification results are max. Power values.

In addition it is already specified in the 802.3 specification that all numbers of class power are maximum numbers.

SuggestedRemedy

Add the following text right after Table 33:
"PD that asks more power then advertised in L1 hardware classification is not compliant to this standard".

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **18** *L* **42** # 59

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *33.2.7*

"The Type 2 PSE shall provide to the PI VClass as defined in Table 33–4a."

H/W L1 class is optional.

SuggestedRemedy

"The Type 2 PSE may optionaly provide an enhanced hardware classification to the PI which consists of the following sequence where levels are defined in Table 33–4a. The PSE provides strong sourcing current and weak sinking current.
* Apply Vclass
* Allow settling time
* Measure Iclass
* Apply Vmark
* Allow settling time
* Apply Vclass
* ...

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.7.2a** *P* **19** *L* **22** # 132

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *33.2.7*

Text allows PSE to drop port voltage to reset during 2-event classification. Text should disallow PSE from dropping port voltage during classfication.

SuggestedRemedy

IS:
If at any point during the classification sequence the PSE allows the voltage at the PI to enter the VReset range as defined in Table 33–4a, the PSE shall classify the PD as Class 0.

SHOULD BE:
The Type 2 Physical Layer PSE shall complete Physical Layer classification and transisiton to the POWER-ON state without allowing voltage at the PI to go below Mark Event Voltage (VMark). If at any point prior to POWER-ON, the PI voltage drops below VMark, the classification is invalid. Subseqent behavior is undefined.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Change text to:
The Type 2 PSE that uses T2PL class should complete Physical Layer classification and transisiton to the POWER-ON state without allowing voltage at the PI to go below Mark Event Voltage (VMarkmin). If at any point prior to POWER-ON, the PI voltage drops below VMark, the PSE shall consider the classification invalid. Subseqent behavior is undefined and is implementation specific.

Undefined or class 0?

See 194, 103

Cl **33** *SC* **2.7.2a** *P* **19** *L* **23** # 103

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *33.2.7*

Draft D0.9:

If PSEs PI voltage enters to Reset range prior to powerup then PD may lost its indication data

SuggestedRemedy

To add the following text after line 23:
"1. PSE shall maintain 7V minimum across the PI after classification phase is done until startup phase. If port voltage falls below 7V after classification phase is ended and PSE is starting up, the PSE may classify the PD as class 0."

Proposed Response *Response Status* **W**

see 132, 194

Cl **33** *SC* **2.7.2a** *P* **19** *L* **25** # 134

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **X** *33.2.7*

.af treated any PDs that classed with too much current (>51mA, ie. >class 4) as class 0.

Should .at treat such PDs as class 0 or class 4?

Today, the draft treats them as class 0. I would suggest they be treated as class 4.

Corrected text as follows:

SuggestedRemedy

IS:
If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0.

SHOULD BE:
If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 4.

Proposed Response *Response Status* **W**

see 166

Cl **33** *SC* **2.7.2a** *P* **19** *L* **35** # 201

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *33.2.7*

A PSE can legally detect and power on a PD without classifying a PD. This allowance should continue.

SuggestedRemedy

Replace the sentence at line-34 with:
If classification is not performed or the result of the first classification event is class 4, …

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **33** *SC* **2.7.2a** *P* **19** *L* **35** # 166

Law, David 3Com

Comment Type **T** *Comment Status* **X** *33.2.7*

Make it clear what classification a PD should have from a single class even that returns Class 4. The text currently says it should be treated as a Type 1 PD, but doesn't say of what class. I believe the PD should be classified as Class 0.

SuggestedRemedy

Suggest that the text 'In this case, the Type 2 PSE shall assume it is powering a Type 1 PD until successful link layer classification is performed.' be changed to read 'In this case, the Type 2 PSE shall classify the PD as Class 1'. (CE NOTE: should this be class 0?)

Proposed Response *Response Status* **W**

the text 'In this case, the Type 2 PSE shall assume it is powering a Type 1 PD until successful link layer classification is performed.' be changed to read 'In this case, the Type 2 PSE shall classify the PD as Class 0'.
see 134

Cl **33** *SC* **2.7.2a** *P* **19** *L* **40** # 181

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *33.2.7*

A PD should be able to ask for the power it requires.

Three independent classification mechanisms exist: type 1 and 2 Physical layer and type 2 Data Link Layer. Interoperability is ensured when a PD requests power from a PSE that can interpret the request. A type 2 PD can use type 1 Physical layer classification to request power.

SuggestedRemedy

Replace the sentence on line 40 with,
If the result of the first classification is any classes 0, 1, 2, 3, the PSE may omit the subsequent mark …

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8** *P* **7b** *L* **49** # 143

Johnson, Peter Sifos Technologies

Comment Type **TR** *Comment Status* **X** *t33-5*

Tmps, Table 33-5 Item 7b, is presented from the perspective of a PD, not a PSE, it seems. 60 msec is the Minimum Valid Load Current Time that a PD must sustain to assure the PSE will keep it powered. From the PSE's perspective however, Tmps is the MAXIMUM allowed Valid (Imin2) Load Interval over which the PSE does not have to reset its Tmpdo timer (and therefore delay a shutdown). Since this parameter is expressed as a minimum, it can be (and has been) interpreted as the Minimum Valid Load Time required to re-start shutdown timing.

SuggestedRemedy

Title the Parameter in 33-5, 7-b, "Valid DC MPS Signature Time Required to Restart Disconnect Shutdown Timing". "60 msec" should then become a MAXIMUM limit, not a MINIMUM limit.

Proposed Response *Response Status* **W**

Need to clarify text.

Cl **33** *SC* **2.8.1** *P* **25** *L* **50** # 178

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **X** *soa*

The requirement that "A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the Vport specification" essentially negates the broader purpose of specifying Iinrush, Tlim, and Ilim elsewhere in the specification. PSE's that enter a current limiting state, as defined by Iinrush, Ilim, and Tlim will in all likelihood drop below the Minimum Vport level since they are funtioning as current sources (400 to 450mA), not voltage sources in this mode. This behavior is time-bounded by Tlim, of course.

Since Iinrush, Ilim, and Tlim provide robustness within PoE to handle marginally compliant transient overload conditions, it seems unwise to undermine those requirements with this clause. Also, 33.2.8.8 now adds further criteria ("SOA" Type 2 PSE's) for removing power based upon transient overload current designed to protect PSE's and interconnect integrity. The relevance of that criteria would be undermined by this particular clause.

Finally, this clause is simply inconsistent and contradictory with 33.2.8.8 b).

SuggestedRemedy

Revise 33.2.8.1 as follows:

Replace:

"A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the Vport specification"

With:

"The Minimum Vport specification in Table 33-5 shall not apply to PSE's operating in a current limiting condition over the period Tlim as defined in 33.2.8.5 and 33.2.8.8."

Proposed Response *Response Status* **W**

see 137

Cl **33** *SC* **2.8.1** *P* **25** *L* **51** # 137

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **X** *soa*

A new statement is added:

"A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the VPort specification."

This is inconsistant with many other entries in the specification, for example Table 33-5, item 11, Short Circuit Time Limit, TLIM, 50ms minimum.

SuggestedRemedy

Remove the statement:

"A PSE in the power on state may remove power from the PI when the PI voltage no longer meets the VPort specification."

Proposed Response *Response Status* **W**

see 178

Cl **33** *SC* **2.8.4** *P* **26** *L* **37** # 195

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *Ipeak*

The formula for IPEAK ensures a constant PSE power of 17.6 W. To ensure interoperability the PSE needs to provide what the PD can demand.

The PD may demand 14.4 W. When the PSE is providing 44 V, the PSE must provide 17.6 W. However, when the PSE is providing 57 V, the PSE only needs to provide 16.0 W to support the same PD demand. This unnecessary power requirement increases when using PoE plus power levels. These requirements place an unnecessary burden on the PSE.

These comments also apply to 33.2.8.4a.

This comment is related to other comments on this same section and the PD table 33-12 and 33.3.5.2.

SuggestedRemedy

If the PD is a constant power load that can demand 400/350Iport more, then determine the PSE power for a given PD demand, divide this PSE power by the PSE voltage to get IPEAK. This is a quadratic equation.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.5** *P* **27** *L* **7** # 110

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *inrush*

Draft 0.9:
There is no definition of the requirements for ILIM between 0V to 10V.
The proposal below was part of maintenance request 1162.

SuggestedRemedy

Change 33.2.8.5 item e from:

e) During startup, for PI voltages between 10V and 30V, the minimum IINRUSH requirement is 60mA.
See Figures 33C.4, 33C.6.

To:
e) During startup, for PI voltages between 10V and 30V, the minimum IINRUSH requirement is 60mA. During startup, for PI voltages between 0V and 10V, the max IINRUSH requirement is as specified by Table 33-5, item 10.
See Figures 33C.4, 33C.6 and 33C.6.1.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.5** *P* **27** *L* **9** # 121

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *annex*

Draft0.9:
In many ocasions the normative text send the reader to see figures 33C.4 and 33C.6 which contains valuble data.
These drawings should be at the normative text as it was in early drafts of 802.3af and were moved to the informative section due to editing considerations.

SuggestedRemedy

Move figures 33C.4 and 33C.6 to the normative section at the location where they are mentioned for the first time.

Proposed Response *Response Status* **W**

see 50

Cl **33** *SC* **2.8.6** *P* **27** *L* **11** # 186

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *soa*

The specification requires that a PSE remove power based on maximum ICUT and Tovld thresholds. This does not ensure interoperability or meet the safety specifications, and therefore, forces a design requirement.

SuggestedRemedy

Allow the existing requirement or figure 33-9a SOA requirements to specify what is required for compliance.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.6** *P* **27** *L* **11** # 50

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X** *annex*

Overload is used in a particular way, and the requirement is difficult to understand. Also, confusion persists about the relationship of the ranges.

SuggestedRemedy

add definition:
"Overload is defined as the load current range between the maximum current defined in 33.2.8.4 and the short circuit current defined in 33.2.8.8"

Move figure 33C-6 from the informative into this section to support the normative text. Create a second figure to support .at.

Proposed Response *Response Status* **W**

see 121

Cl **33** *SC* **2.8.8** *P* **27** *L* **33** # 185

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *soa*

This section needs to be modified in order to permit PSE to reach current levels just below the SOA described in figure 33-9a.

SuggestedRemedy

If a PSE provides current that meets system safe operating (SOA) requirements, IEC 60950, and PD minimum power needs, then safety and interoperability are met with fewer design requirements imposed. Within the region between PD current needs and SOA current limits, a PSE system selects the design (current limit, current cut-off, and duration) that meets its markets needs. See Vport ad hoc current limit presentations for the latest proposed system current vs time limits.

Suggested remedy:
Type-1 PSE can power as described in this section.

Add, Type-2 PSEs
Remove the requirement to remove power within TLIM, and require that the PSE meet the SOA limits.
Remove the sentence "Measurement to be taken after 1 ms to ignore initial transients."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **27** *L* **33** # 61

Patoka, Martin — TI

Comment Type **T** *Comment Status* **X** *annex*

The term "short circuit" is not defined, arising to much confusion about table 33-5. Also, there has been much discussion about the foldbacl of 33.2.8.5. Many veterans believe that the inferred foldback applies to short circuit as well as startup.

SuggestedRemedy

Add definition: "The short circuit condition occurs when the PSE output is loaded beyond the overload range (Icut_max) and some form of hardware limiting occurs to keep the maximum output current below Ilim_max."

I have suggested 33C-6 be move to normative text, so the reference should change.

I recommend that the foldback limits of 33.2.8.5 be moved here and an output I/V curve be provided. These have been discussed in maintenance.

Proposed Response *Response Status* **W**

Cl **33** *SC* **2.8.8** *P* **27** *L* **41** # 108

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *annex*

Draft0.9:
The specification allows foldback current limit implementations in startup mode as defined by 33.2.8.5.
MR request 1162 material and maintenance group attached drawing shows that the intent of the specification was to allow the same implementations during short circuit condition as well. However items d and e of 33.2.8.5 was not copied to 33.2.8.8 as should have done.

SuggestedRemedy

1. Move drawing 33C.4 or its updated version as a result of the Vport ad-hoc work to the normative section as it was in the early drafts of the IEEE802.3af.
2. Move drawing 33C.6 or its updated version as a result of the Vport ad-hoc workto the normative section as it was in the early drafts of the IEEE802.3af.
3. Add drawing 33C.6.1 to 33.2.8.8

4. Replace the following text:

The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC input voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
See Figure 33C.4 and Figure 33C.6.

With the proposed text: (items d and e are additions to previous text)
The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:
a) Max value of the PI current during short circuit condition.
b) Max value applies for any DC output voltage up to the maximum voltage as specified in item 1 of Table 33-5.
c) Measurement to be taken after 1ms to ignore initial transients.
d) During short circuit condition, for PI voltages above 30V, the ILIM requirement is as specified in Table 33-5, item 10.
e) During short circuit condition, for PI voltages between 10V and 30V, the minimum ILIM requirement is 60mA as long as system decides to keep the port ON, and the maximum requirement is as specified in Table 33-5, item 10.
During short circuit condition, for PI voltages between 0V and 10V, the minimum ILIM requirement is 0mA and the maximum requirement is as specified in Table 33-5, item 10.
See Figures 33C.4, 33C.6 and 33C.6.1."

5. Add the following notes after 33.2.8.8-e:

Notes:

1. Items d and e in 33.2.8.8 allows implementation of foldback
current limit type in which ILIM requirement is decreased if Vport is

decreased below pre specified value.

2. Short circuit condition definition in IEEE802.3af is a case in which the port voltages is dropped below normal operating voltages as defined by table 33-5 items 1 and 2 due too load fault conditions that exceeds table 33-5 item 8"

6. Add the following note text after 33.2.8.5-e:

Note: items d and e in 33.2.8.5 allows implementation of foldback current limit type in which Iinrush requirement is decreased if Vport is decreased below pre specified value.

Foldback current limit is optional in the standard.

IMPACT ON EXISTING NETWORKS:

No impact. It is optional.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **27** *L* **43** # 28

LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **X** *soa*

Is there any reason not to make SOA curve applicable to Type 1 PSEs as well as Type 2 PSEs? All safety and existing peformance studies obviously made use of Type 1 equipment. Further, the SOA curve is well outside of the ILIM max defined for Type 1, therefore it should be impossible for a compliant Type 1 device to violate this new SOA requirement.

SuggestedRemedy

Strike "Type 2"

Proposed Response *Response Status* **W**

Cl **33** *SC* **2.8.8** *P* **27** *L* **43** # 78

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X** *soa*

I am not sure how to solve this issue, but the assertion to remove power immediately upon PI current exceeding the limit makes me concerned about the response to a large transient causing the output FET to turn off and then inductance taking over and blowing things up. The test for this is going to be a challenge.

SuggestedRemedy

Change the term "immediately" to something more specific.

Proposed Response *Response Status* **W**

see 96

Cl **33** *SC* **2.8.8** *P* **27** *L* **43** # 96

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X** *soa*

Power can not tremoved "immidiatly" this term is not well defined.

SuggestedRemedy

Change to "Power shall be removed within 1msec from the PI of Type 2 PSE...."

Proposed Response *Response Status* **W**

see 78

Cl **33** *SC* **2.8.8** *P* **27** *L* **49** # 122

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *soa*

Change the Fusing equation in a way that refect all its parameters.
See "Fusing equation: how it was derived in 802.3af" presentation for September 2007 for more details.

SuggestedRemedy

Change from I=(0.025/t)^0.5
To: Iport=(K/t)^0.5
Where
Iport is the current at the PI
t is the duration that the PI sources Iport
K is a 25mJoul energy limitation of the port current when it is not in steady state normal operation.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.8** *P* **28** *L* **32** # 23

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X** *soa*

Figure 33-9a title does not specify which PSE Type to which is applies, but the SOA curve applies only to Type 2 PSEs.

SuggestedRemedy

Replace title with:

'Type 2 PSE PI Safe Operating Area'

Proposed Response *Response Status* **W**

see 28
someone also commented that it could apply to type 1 also (Law?)

Cl **33** *SC* **2.8.9** *P* **28** *L* **39** # 11

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X** *soa*

When violating the SOA curve in Figure 33-9a, TLIM is too long to wait for power removal. The current normative text in this section should apply only to Type 1 PSEs and Type 2 PSEs w/ ILIM current limiting.

SuggestedRemedy

Change text to read:

If a short circuit condition is detected by a Type 1 PSE or a Type 2 PSE implementing ILIM current limitation, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33-5. See Figure 33C.4 and Figure 33C.6.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.8.9** *P* **28** *L* **39** # 111

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *soa*

Draft0.9:
33.2.8.9 text is true for the case that system (PSE and PD) are within their normal voltage operating range however it is not clear from the text.
It is clear from figure 33C.4 and 33C.6 which are located in the informative section.

SuggestedRemedy

Replace 33.2.8.9 text from:

"If a short circuit condition is detected, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33-5. See Figure 33C.4 and Figure 33C.6."

to:

For PI voltages within PI normal operating voltage range as defined by table 33-5 item 1, If a short circuit condition is detected, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33-5.
See Figure 33C.4, Figure 33C.6. and Figure 33C.6.1"

For PI voltages below or above Vport normal operating range as defined by table 33-5 item 1, If a short circuit condition is detected, power removal from the PI may begin at any time of t<TLIM and be complete by TOff, as specified in Table 33-5.
See Figure 33C.4, Figure 33C.6. and Figure 33C.6.1"

Proposed Response *Response Status* **W**

see 50, 121

Cl **33** *SC* **2.9** *P* **29** *L* **20** # 242

Diab, Wael Broadcom

Comment Type **T** *Comment Status* **X** *33.2.7*

This is not accurate as it does not include the Data Link Classification.

SuggestedRemedy

Please rewrite the following sentence to either one of these:

"Where a PSE does not provide either of the Physical Layer classification functions specified in 33.2.7, all PDs are treated as Class 0 Type 1
PDs."

TO

"Where a PSE does not provide the classification function specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs."

OR

"Where a PSE does not provide either of the Physical Layer or Data Link Layer classification functions specified in 33.2.7, all PDs are treated as Class 0 Type 1 PDs."

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.9** *P* **29** *L* **26** # 148

Law, David 3Com

Comment Type **T** *Comment Status* **X** *baseline*

The text states that '.. and the mechanism for obtaining that additional information, is beyond the scope of this standard ..'. I do not believe that is true anymore due to the link layer classification protocol.

SuggestedRemedy

Reword to acknoledge link layer classification.

Proposed Response *Response Status* **O**

Cl **33** *SC* **2.9** *P* **29** *L* **26** # 16

LANDRY, MATTHEW SILICON LABORATO

Comment Type **TR** *Comment Status* **X** *baseline*

It unclear to me why using historical power consumption information should not be a valid means of managing power allocation. The sentence starts by saying it is out of scope, but then goes on to start placing restrictions on what is allowed. Furthermore, how would one even test compliance to this normative exclusion?

SuggestedRemedy

Strike the phrase:

"with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD."

Proposed Response *Response Status* **W**

is this Thompson text? I don't remember the origin.

Cl **33** *SC* **3.1** *P* **33** *L* **42** # 124

Darshan, Yair Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *4p*

The note in line 42 precludes the following applications:
1. Using two pairs to power a 10/100BT PD and using the other 2P in the same cable to power a 2nd 10/100BT PD.

2. Using two power sources one coming from Midspan and other coming from the switch to a single PD with separate power lines for redundancy and/or power application.

The standard should not preclude implementations that are using standard compliant 2P system.

Theoretically a PD can get N x 2P power sources while each of the 2P system is well defined by the standard and the standard should not preclude it since it is implementation issue and it is not a source of interoperability issues.

SuggestedRemedy

Change from:

"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard."

to:
"NOTE-PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode are not precluded by this standard as long as the requirements of this standard are kept for each mode."

Other equivalent wording is possible.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.1.a** *P* **34** *L* **13** # 97

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **D** *33.2.7*

The current text may cause wrong interpretations.

The problem with the current text is the wording "..the PD will appear to the PSE as Type 1 PD until..."
Instead saying that the PD will consume up to type 1 power max power level (it is type 2 PD due to its class 4 signature)

Rational:
If a Type 2 PSE implements only type 1 layer 1 classification and it reads class 4 which is type 2 PD only, it should appear to the PSE as class 4 PD which is type 2 PD that have the potential to require up to 29.5W however it will consume up to 12.95W until layer 2 is established.

SuggestedRemedy

Change from:
"Table 33-12 specifies the electrical characteristics of Type 1 and Type 2 PDs. When a PSE exhibiting only Type 1 Physical Layer classification powers a Type 2 PD, the PD will appear to the PSE as a Type 1 PD until the PSE successfully performs Data Link Layer classification thereby identifying itself as a Type 2 PSE."

To:
"Table 33-12 specifies the electrical characteristics of Type 1 and Type 2 PDs. When a PSE exhibiting only Type 1 Physical Layer classification powers a Type 2 PD, the PD will consume max. type 1 power levels until the PSE successfully performs Data Link Layer classification thereby identifying itself as a Type 2 PSE"

Proposed Response *Response Status* **W**

PROPOSED REJECT.

This is the PD section. From the PD point of view it has only discovered a Type 1 PSE.

Cl **33** *SC* **3.3** *P* **37** *L* **11** # 62

Patoka, Martin — TI

Comment Type **T** *Comment Status* **X** *annex*

Voltage and current offsett in table 33-8 are ambiguous.

SuggestedRemedy

Move a copy of figure 33C-20 to and annotate to show Ioffset. The value of Ioffset is not very restrictive since it is typically negative as shown in the figure. The voltage and current offset need to be defined as being related to the projection of the (two point) line-fit between 2.7V and 10.1V.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4** *P* **38** *L* **1** # 238

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

Related to my previous comment on restructuiring this section, I would suggest the following text

SuggestedRemedy

Rename title of section 33.3.4 to PD Classifications

AND

insert the following text in the general section:

"A PD may be classified by the PSE based on Physical Layer classification information, Data Link classification or a combination of both provided
by the PD. The method of classification will depend on the Type of the PD and the Type of the PSE.

Type 1 PDs shall implement a Physical Layer classification as described below.

Type 2 PDs shall implement both a Physical Layer classification and a Data Link Classification as described below"

AND

Retain and restructure current text per my previous comment into sub-clauses

Proposed Response *Response Status* **W**

Add note in PD section to see new Class section in 33.2.7. Use suggested text to help craft new section.

See Law 170.

Cl **33** *SC* **3.4** *P* **38** *L* **1** # 237

Diab, Wael — Broadcom

Comment Type **ER** *Comment Status* **X** *33.2.7*

This is analogous to my comment on th PSE section.

This section is very confusing. We dive into Physical Layer classification and then do Data-Link Layer Classification. I would suggest that we make 33.3.4 a general introduction to classification. We then take 33.3.4 and 33.3.4a and make them subclauses of this new geenral section.

For the content of the general section on classification, I will submit a seperate comment (my previous comment in the .csv file).

SuggestedRemedy

I would suggest that we make 33.3.4 a general introduction to classification. We then take 33.3.4 and 33.3.4a and make them subclauses of this new geenral section.

Proposed Response *Response Status* **W**

See Law 170
see 51, 238

Cl **33** *SC* **3.4** *P* **38** *L* **1** # 51

Patoka, Martin — TI

Comment Type **ER** *Comment Status* **X** *33.2.7*

The presence of LL classification is harder to understand with the transfer of the requirement to 33.6.

SuggestedRemedy

Change title of 33.3.4 to: PD classifications.

Add sentence to line 5:

A type 2 PD that receives a type 1 physical layer classification, or partial type 2 physical layer classification shall behave as a type 0 PD.

Add paragraph at line 6 similar to:

A type 2 PD must respond to type 2 data link layer classification messsages as defined in section 33.6.

Proposed Response *Response Status* **W**

see Law 170
see 238, 237

Cl **33** *SC* **3.4.1** *P* **38** *L* **11** # 177

Jones, Chad — Cisco

Comment Type **T** *Comment Status* **X** *legacy dll*

The statements "However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3." and "Type 2 PDs shall return a Class 4 classification signature in accordance with the maximum power draw..." (line 49) forces Type 2 PDs to only draw more than 12.95W. Why is it illegal for me to make a Type 2 PD that is Class 2 then uses LLDP to further refine the power consumption, say down to 5W? If I am forced to advertise Class 4 there will be situations where my PD could be powered by a PSE but won't be because the PSE has more than 7.0W but less than 15.4W left in reserve.

SuggestedRemedy

The text in 33.3.4.1 and 33.3.4.2 needs reworked to reflect this operating condition.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **23** # 12

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **T** *Comment Status* **X** *pd33.2.7*

The 'Usage' column in Table 33-10 seems unnecessary. Normative text already forces Type 1 PDs to use Class 0-3, and Type 2 PDs to use Class 4.

SuggestedRemedy

Remove 'Usage' column from Table 33-10.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **24** # 190

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *legacy dll*

Table 33-10 is not clear. Why is a range of maximum stated? Does a class 2 PD need to draw at least 3.84 W?

A type 2 PD should be able to produce all classes.

SuggestedRemedy

Only state the maximum class power allowed. For example, a class 2 PD can draw up to 6.49 W.

Allow a type-2 PD to request the power it needs. That is, if it needs class-2 power levels it can do this directly using a type-1 PD Physical layer classification mechanism.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.1** *P* **38** *L* **39** # 234

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **D** *baseline*

Is the intention of the note here to be cannot or shall not? There is nothing preventing someone from building a PD that is not compatile with the draft, hence cannot is not accurate.

SuggestedRemedy

Suggest changing cannot to shall not

Proposed Response *Response Status* **O**

Will be resolved by 38

Cl **33** *SC* **3.4.1** *P* **38** *L* **9** # 174

Jones, Chad Cisco

Comment Type **T** *Comment Status* **X** *legacy dll*

The text makes no statement about Type 1 PDs using Data Link Layer classification. For sure, manufacturers will do this.

SuggestedRemedy

Add the sentence: "A Type 1 PD may optionally choose to implement Data Link Layer classification."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **38** *L* **47** # 52

Patoka, Martin TI

Comment Type **ER** *Comment Status* **X** *annex*

The concept of physical layer classification is difficult to general readers to understand. This compounded by the 2 event technique.

SuggestedRemedy

A figure such as containned in stanford_1_0707 page 12 should be incorporated into this section to clarify the whole subject. It is important to put it in the normative section to support the text.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **38** *L* **49** # 13

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X** *legacy dll*

Type 2 PDs don't necessarily have to exhibit >12.95W power consumption. That makes the phrase 'in accordance with the maximum power draw as specified by Table 33-10' rather misleading.

SuggestedRemedy

Delete the phrase.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **39** *L* **14** # 147

Law, David 3Com

Comment Type **T** *Comment Status* **X** *33.2.7*

There are actually two types of classification. [1] A PSE's classification of a PD. [2] A PD's classification of the PSE. The text seems to call all this PD hardware classification and while it is that mechanism that is used by the PD to classify the PSE I think we need to make that distinction clear in the text. Does the text 'Once a PD has been powered by a Type 2 PSE' imply that the PD has to detect that the current sourced by the PSE has exceeded the maximum for a Type 1 PSE - although even that doesn't guarantee it is Type 2 PSE power. The only real test that is available is that a Type 2 hardware classification or link layer classification has completed.

SuggestedRemedy

Perfom the following change: [a] Delete the first sentence of the third paragraph of subclause 33.3.4.2. Text currently reads 'Until successful Type 2 hardware classification or link layer classification has completed, a Type 2 PD's PSE Type state variable is set to Type 1.'. [b] Delete subclause 33.3.4.2.2. [c] Insert new subclause 33.3.4a, renumber as necessary. The content of this new subclause should cover the areas in [a] and [b] as well as clarify the text.

33.3.4a PSE type classifiction

A Type 2 PD shall classify the PSE Type as either Type 1 or Type 2. The default value of PSE Type shall be Type 1. After a successful Type 2 hardware classification or link layer classification has completed the PSE Type shall be set to Type 2. The PD shall reset the PSE Type to Type 1 when the voltage at the PI is less than or equal to VReset_lo max. Once a Type 2 hardware classification or link layer classification has completed a Type 2 PD shall reset the PSE Type to Type 1 if the voltage at the PI is less than or equal to VReset_hi min.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.4.2** *P* **39** *L* **15** # 235

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **D** *baseline*

The following sentence adds no value as the prior states the required, which is that these are externally observable parameters

SuggestedRemedy

Delete

"Equivalent implementations that present the same external behavior are allowed."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

21.5 contains a pointer to 1.2 that contains language similar but more complete than this sentence.

Cl **33** *SC* **3.4.2** *P* **39** *L* **39** # 196

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *legacy dll*

A type-2 PD should be able to request the power it needs.
A type-2 PD should be able to use type-1 physical layer classification.

SuggestedRemedy

Replace the existing sentence with:
A Type 2 PD shall return the same class signature irrespective of the number of classification voltage probes performed by the PSE.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **42** *L* **24** # 191

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *inrush*

The peak operating current specified in this section is Pport_max/Vport. It is not clear that Pport_max is the power the PD is classified to because the Iport max of table item 4 contradicts this. For example, a class 3 PD can draw 6.49 W and with a 36 V input will draw 6.49/36 = 180 mA. The value in item 4 states 210 mA.

Also see a related comment on this same parameter. It is also not clear which Iport is being referenced-table 33-12 has items 4 and 5 with the same name.

SuggestedRemedy

The task force needs to review these values and state what ensures interoperability.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5** *P* **43** *L* **12** # 67

Patoka, Martin TI

Comment Type **T** *Comment Status* **X** *backfeed*

Table 33-12 item 10: Backfeed voltage
see also 33.3.5.10 P45 line 24.

The maximum allowed bridge reverse current is 2.8V/100K = 28uA. This requirement is too stringent and appears to prevent the use of schotty diodes. Given that we are doubling the current, efficiency and component temperature rise are adversely impacted. THere is no reason to limit the implementation of a PD to preclude the use of Schottky diodes.

SuggestedRemedy

Decrease the resistance to 9.09k. this was selected based on a B2100 diode 2A, 100V schottky at 125C reverse leakage at 60V (.3ma).

Proposed Response *Response Status* **W**

Cl **33** *SC* **3.5.1** *P* **43** *L* **19** # 54

Patoka, Martin TI

Comment Type **ER** *Comment Status* **D** *baseline*

"The PD shall turn off at a voltage less than VPort minimum and greater than or equal to VOff."

"The specification for VPort in Table 33–12 is for the input voltage range after startup, and it includes loss in the cabling plant."

The terms "off" and "startup" are not defined.

SuggestedRemedy

after the first sentence add:

"Startup begins upon application of Vport per table 33-12 and concludes at the end of the inrush period per 33.3.5.3."

this relies on the additions to the inrush paragraph.
change the sentences to:

"The PD shall not draw more current than its Class current per table 33-11 at voltages less than Vport min."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Heartburn with shall in second 'definition', "class signature current'

Cl **33** *SC* **3.5.2** *P* **43** *L* **24** # 258

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X** *cable*

Why are we discussing the resistance of the cabling here? I think we should either refer to the worst case setup using the cabling types or find a way to test the PD at its input

SuggestedRemedy

see comment

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.2** *P* **43** *L* **25** # 144

Bennett, Ken — Sifos Technologies, In

Comment Type **T** *Comment Status* **X** *baseline*

The measurements of Average Power, which include series resistors in the Annex 33C, are existing recommendations. The Annex states that other test circuits are possible, so long as compliance with Clause 33 are adequately demonstrated. Using the words "Shall be Measured" in Clause 33.3.5.2 changes this recommendation to a requirement for existing measurement techniques, which may already use adequately demonstrated alternatives.

SuggestedRemedy

Remove the two sentences containing the words "shall be measured".

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.3** *P* **43** *L* **39** # 68

Patoka, Martin — TI

Comment Type **T** *Comment Status* **X** *inrush*

In order to have the inrush current agree with the Vport specification, the PD should not startup at voltages less than Vport min. Otherwise inrush current may be drawh at voltages in the detection and classification ranges. Figure 33C-1 and startup dv/dt 33C.1.8, as well as many other figures imply that the PD does not draw current at less than 33V. Since 33.2.8.5 does not require the PSE to provide ANY current at 0V out, figure 33C-1 can best be described as a test of the foldback characteristic. That is, a capacitor at 0V applied to the PSE output may never charge - and is not required to do so. Requiring PSEs to supply inrush current into a short is potentiually a burdensome cost adder to the PSE. This then leads to the ability to allow the PSE a fast turn-off into a short.

SuggestedRemedy

Add the following sentence:

"PDs shall not draw inrush current at voltages less than Vport min."

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.5.4** *P* **43** *L* **46** # 184

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *baseline*

The value of Iport_max created by the formula-using PD Pport_max-does not match the value provided in table 33-12. For example, class 0 PD power is 12.95 W maximum and 12.95W/44V = 294 mA, not the 400 mA shown in table 33-12, item 4.

SuggestedRemedy

The PD formula provides approximately the correct answers when the PSE Pport_max values are scaled by 400/350 for the system classified power.

Table 33-12 values should match values created by the formula-rounding appears to have been used.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.6** *P* **45** *L* **41** # 14

LANDRY, MATTHEW — SILICON LABORATO

Comment Type **T** *Comment Status* **X** *baseline*

Items (c) and (d) do not provide any new information, and are really just repetition of items (a) and (b).

SuggestedRemedy

Strike items (c) and (d) and replace with the following statement:

A PD that does not maintain the MPS components a) and b) above may have its power removed within the limits of TMPDO as specified in Table 33-5.

Proposed Response *Response Status* **O**

Cl **33** *SC* **3.6.1** *P* **46** *L* **13** # 15

LANDRY, MATTHEW SILICON LABORATO

Comment Type **T** *Comment Status* **X** *baseline*

The itemized list is generally confusing. The whole point is that a PD with >180uF input capacitance may have difficulty meeting the DC MPS during a voltage transient.

SuggestedRemedy

Replace with a general CAUTION statement:

CAUTION--A PD with CPort > 180uF may not be able to meet the IPort specification in Table 33-13 during the maximum allowable port voltage droop (i.e. 57V to 44V in series with 20 ohms for a Type 1 PSE and 57V to 50V in series with 12.5 ohms for a Type 2 PSE). Such a PD should increase its IPort min or make other such provisions to ensure meeting the DC maintain power signature.

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.4** *P* **49** *L* **1** # 193

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *baseline*

This specification is not consistent with its common mode noise measurement requirements. Clause 33 specifies a range of 1 MHz to 100 MHz for a PSE. Other clauses are for a MDI signal pairs and have no concept of measurement BW.

Testing during clause 33development ensured data integrity with the constraints imposed. Reducing the BW of existing clause common mode measurements should not reduce the compliance of legacy systems. Requiring PSE to meet other clauses below 1 MHz places an unnecessary cost burden on the system.

SuggestedRemedy

Modify other clauses or place a statement in clause 33 that allows the Ethernet MDI to use the clause 33 common mode requirements whether PoE power is present or not.

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.7** *P* **51** *L* **44** # 81

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X** *baseline*

75 ohms is not defined at any particular frequency.

SuggestedRemedy

Most ports that have such termination are AC coupled to maintain DC isolation, thus they will not be 75 ohms at DC. We need to spec this better.

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.8** *P* **53** *L* **52** # 88

Darshan, Yair Microsemi Corporation

Comment Type **T** *Comment Status* **X** *baseline*

Draft D0.9

We need to clearly define that Midspan should provide signal continuity for 1G Midspan as well.

SuggestedRemedy

Change line 53 from"A Midspan PSE inserted into a channel shall provide continuity for the signal pairs."

To "A Midspan PSE inserted into a channel shall provide continuity for the signal pairs for 10/100 and 1000BT Midspan device".

Proposed Response *Response Status* **O**

Cl **33** *SC* **4.8** *P* **54** *L* **5** # 211

Thompson, Geoff Nortel

Comment Type **ER** *Comment Status* **D** *cable*

Comment about 2 pair Cat 5 cabling is misleadingly acceptive.

SuggestedRemedy

Add text:
"The specification of two pair midpan PSEs is beyond the scope of this document."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Add text:
"The specification of two pair midspan PSEs is beyond the scope of this document."

Cl **33** *SC* **4.8.1.4** *P* **55** *L* **1** # 82

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **D** *cable*

Category 5 is obsolete now that 1000BASE-T is supported

SuggestedRemedy

Change to Category 5E

Proposed Response *Response Status* **O**

Cl **33** *SC* **5.8** *P* **56** *L* **25** # 200

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **X** *cable*

The cable current limits selected should provide temperature margin above design limits of the broader market. Ambient values do not need to be specified but values used to calculate system interoperability parameters should reflect broad market requirements.

SuggestedRemedy

Survey the task force members to determine an acceptable ambient operating range for cables. Calculate parameters dependent on ambient temperature using the results of this survey.

Proposed Response *Response Status* **O**

Cl **33** *SC* **5.9** *P* **56** *L* **36** # 69

Patoka, Martin — TI

Comment Type **T** *Comment Status* **X** *baseline*

"a) Power classification and power level in terms of maximum current drain over the operating voltage range, 44V to 57 V, applies for PD only"

"d) “PSE” or “PD” as appropriate"

Since we have new and incompatible PD/PSE combinations, labelling the PSE and PD type would be of value

SuggestedRemedy

"a) Power classification, type (e.g. 1 or 2) and power level in terms of maximum current drain over the operating voltage range, 44V to 57 V, applies for PD only"

"d) “PSE” or “PD” and type (e.g. 1 or 2) as appropriate"

Proposed Response *Response Status* **O**

Cl **33** *SC* **5.9** *P* **56** *L* **36** # 89

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X** *baseline*

Draft D0.9

Update a) : If it for PDs only it should be from 36V to 57V.

SuggestedRemedy

Change a) from " Power classification and power level in terms of maximum current drain over the operating voltage
range, 44V to 57 V, applies for PD only"

To: "Power classification and power level in terms of maximum current drain over the operating voltage range, 36V to 57 V, applies for PD only"

Proposed Response *Response Status* **O**

Cl **33** *SC* **6** *P* *L* # 268

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X** *dll*

We need to consider what happens when there is a loss of communication more carefully. Simply throttling the power back to the HW level does not make sense as the device is hosed

SuggestedRemedy

At the very least the PSE should support the last negotiated state not the HW state as it is not guranteed what the device will do if the power is throttled back.

Additionally, we can look at mechanisms like power cycling within certain time limits that we specify to try and get the agent up and running.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.2** *P* **61** *L* # 266

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X** *dll*

The TLV descriptions are a summary of what is in ANSI/TIA 1057. In addition to a risk that at some point these two standards may differ, the information needs to be elaborated on

SuggestedRemedy

Either do this whole thing by reference or incorporate the entire descriptions from ANSI/TIA 1057-2006

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.2.1** *P* **61** *L* **43** # 43

Patoka, Martin TI

Comment Type **E** *Comment Status* **X** *dll*

"The minimum status TLV definition follows the format defined in ANSI/TIA-1057"

The paragraph number may change by document revision

SuggestedRemedy

Add the document revision, data, etc.

Proposed Response *Response Status* **W**

See 217

Cl **33** *SC* **6.2.1** *P* **61** *L* **43** # 217

Diab, Wael Broadcom

Comment Type **E** *Comment Status* **X** *dll*

Can we reproduce the ANSI TLV in the 802.3 document?

SuggestedRemedy

Please reproduce the TLV in the 802.3 document, or at the very least circulate with the review package

Proposed Response *Response Status* **W**

Bring this is with Law.

CE Note: comment was missing comment type. CE set it to E.

See 240

Cl **33** *SC* **6.2.1** *P* **61** *L* **43** # 240

Diab, Wael Broadcom

Comment Type **ER** *Comment Status* **X** *dll*

Do we have a release from ANSI/TIA to copy material into our draft?

SuggestedRemedy

If needed, please work with the staff or alert them to this issue

Proposed Response *Response Status* **W**

see 217

Cl **33** *SC* **6.3.2** *P* **63** *L* **27** # 198

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **X** *dll*

The PD power in not completely specified.

SuggestedRemedy

The PD power should represent its peak 1 second average power.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.4** *P* **64** *L* **6** # 84

Dove, Daniel ProCurve Networking

Comment Type **TR** *Comment Status* **X** *dll*

State diagram has a number of undefined variables

SuggestedRemedy

Define all variables used in the state diagram.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.4.1** *P* **65** *L* **14** # 145

Law, David 3Com

Comment Type **TR** *Comment Status* **X** *33.2.7*

Subclause 33.2.7.2a Type 2 hardware classification permits a Type 2 PSE to perform a single classification if it supports link layer classification. It however then requires that a PD that is classified as Class 4 is treated as a Type 1 PD until link layer classification is performed. I assume the link layer classification is then allowed to increase the power up to the Type 2 PD levels.

Based on the above, if a communications failure causes the PSE to revert to the initial hardware classification, in this case a PD that has increase its power through link layer classification it would have its power allocation cut back in the PSE to the Type 1 maximum. Since the PD may have no idea this is happening it may continue to draw the additional power it though it still had allocated - this in turn could cause the PSE to shut off the PD since it is now exceeding its 'requested' power.

SuggestedRemedy

Change the text so that in event of loss of communications the allocated power will remain at whatever level the last link layer classification was.

Proposed Response *Response Status* **O**

Cl **33** *SC* **6.4.1** *P* **65** *L* **7** # 267

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X** *dll*

The "collision" mechanism needs to be thought out a little more. Specifically, the cases that occur. For example, if the PD is requesting more power and PSE is requesting less power may be a different situation than if both are requesting more power. The timers may not be the best way to resolve the conflict

Also, the term collision is confusing and should be avoided.

SuggestedRemedy

Seperate state machines for the PSE and PD should be done. In each state machine, if a new request is received a behaviour can be defined

In this paradigm we can identify what would constitute a conflict that needs to be resolved.

Proposed Response *Response Status* **O**

Cl **33** *SC* **Table 33-12** *P* **40** *L* **18** # 104

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *t33-12*

Draft D0.9:

Table 33-12 items 1: 40V (acctually it is 39.71V) is the correct number for steady state operation however in order to meet the 7.6% low transient support as specified in table 33-5 item 2a, the PD should design and work at 36V minimum as well.
In addition, the ad hoc have decided to use the same voltage thresholds used in 802.3af PD for 802.3at PD in order to simplify the specification.

Rational and some mathematics to support the above:

a) PSE voltage during transient: 50V-50*7.6% = 46.2V
b) PD voltage at the PI:
Vpd=(Vpse+(Vpse^2-4*R*Ppd)^0.5)/2.
For Ppd=29.5W,
R=12.5 ohms
Vpd=(46.2+(46.2^2-4*12.5*29.5)^0.5)/2=35.93V ==> 36V.
c) At this point the port current will be 29.5W/35.93V=0.82A.
In addition: PSE's Icut_min must be equal or higher then 0.82A.

See attached presentation for more details.

SuggestedRemedy

1. Table 33-12 item 1 for type 2 PD:
Change PD minimum operating voltage to 36V.

2. Table 33-5 item 8:
Add additional row for type 2 PSE specifying that Icut_min=41000/Vport for overload caused by PSE voltage down transient up to 250usec.

3. Add in the additional information column in 33.2.8.6:
"The PSE shall not turn off the port if Iport is less then or equal to 820mA for a time duration of leass then or equal to 250uSec."

Notes (an other reasons why 820mA, 50msec, 5% duty is a good thing):
1. This is not a positive current transient caused by PSE dv/dt. It is cuased by PSE voltage drop.
Per other comments, Tcut min. should be 50msec min. so this requiremnet for 820mA , 250usec is already covered.
3. PD shall not limit its input below 820mA for 250usec duration.
Per other comments PD may require 820mA for max. 50msec , 5% max duty cycle.

Proposed Response *Response Status* **O**

Cl **33** *SC* **Table 33-3** *P* **18** *L* **11** # 244

Diab, Wael — Broadcom

Comment Type **TR** *Comment Status* **X** *33.2.7*

Please either delete the table in its entirety or modify the right hand most column

SuggestedRemedy

Either delete the entire table

OR

change the title of the right hand column to read "Power Ranges Available at output of PSE" and modify each row accordingly:

0 ... 0 - 15.4W
1 ... 0 - 4.0W
2 ... 4.0 - 7.0W
3 ... 7.0 - 15.4W
4 ... Type 1...Assign to Class 0
4 ... Type 2...0 - 36W

Proposed Response *Response Status* **W**

see 9, 163

Cl **33C** *SC* **1.7** *P* **85** *L* **6** # 93

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **X** *annex*

We need to update this part for supporting tests for foldback current limit tests in more general way as done for the startup mode.
(Comments from the maintanance group per MR # 1162.)

SuggestedRemedy

Change the following in Annex 33C clause 33C.1.7:

1. In Figure 33C.7 upper part: add a box labeled "variable load" in series to S1
2. Replace test procedure PSE-7 item 3 text from:

"3) Verify that Iport is within the limits shown in Figure 33C.4"

With "3) Change the variable load in order to verify that Iport is within the limits of Figures 33C.4 and 33C6.1. Please note that the variable load type (resistive, constant voltage or other) depends on different PSE implementations."

Clause 33C.1.4 PSE-4:
Change item 3 in PSE 4 from "Verify that ..in Figure 33C.4" to "Verify that ..in Figures 33C.4 and 33C.6.1"

Change the note in the last two sentences in clause 33C.1.4 after item 6 in PSE-4:
From: "Test setup……expected per Figure 33C.4."
To: "Test setup……expected per Figure 33C.4 and 33C.6.1."

Proposed Response *Response Status* **O**