Current Foldback for Type 2 PSE

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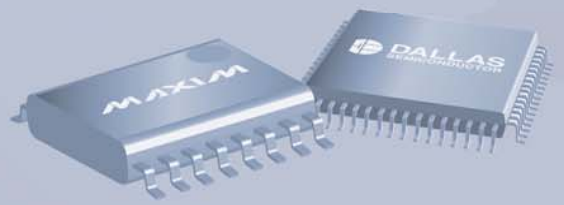
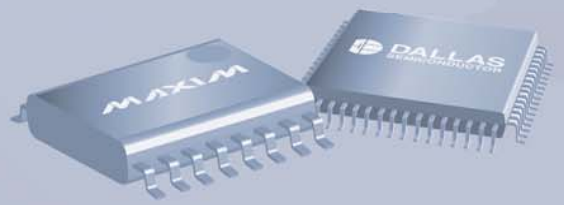


Current Foldback for Type 2 PSE

- **Design Targets:**
  - Keep PSE switch (MOSFET) power dissipation to within its SOA
  - Allows PSE to sustain port power (at reduced current) during transient over load condition

- **PSE Requirements:**
  - PSE port voltage range: 50V – 57V
  - PSE $Iport_{MAX}$ = 720mA at 50V
  - PSE $Ilim_{MAX}$ = 720mA x 400/350 = 823mA at 50V
    - → PSE must provide at least 823mA at Vport = 50V
    - → PSE can reduce its current limit (foldback) when Vport < 50V
    - → To control precisely the power dissipation in the MOSFET, it's better to specified the current limit foldback as a function of Vds.



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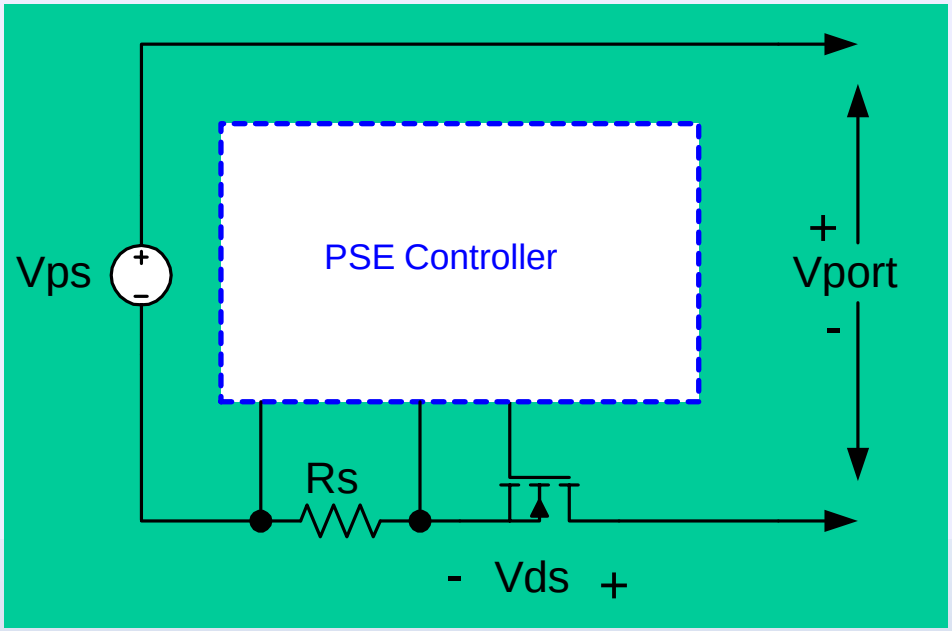


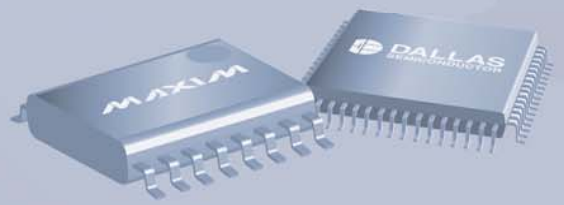
Vds = Vps – Vport

(neglect voltage drop across Rs)

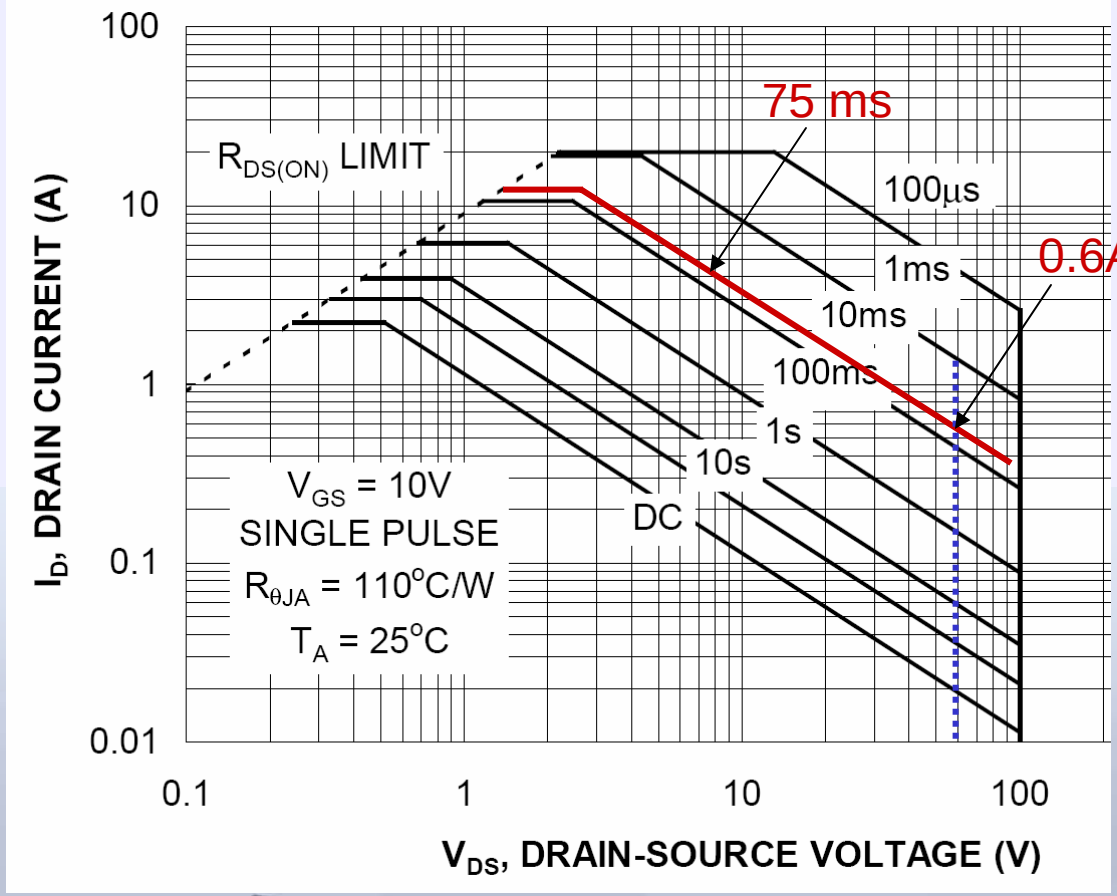
Vps = 57V maximum

Vport = 50V minimum

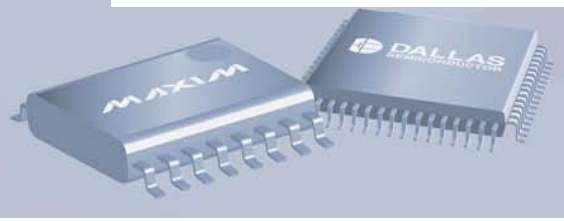
→Vds = 57V – 50V = 7V minimum before the controller can start folding back



Maximum Safe Operation Area – 100V, 120mΩ MOSFET



This is roughly a constant power curve which limit this MOSFET power dissipation to ~30W for 75ms



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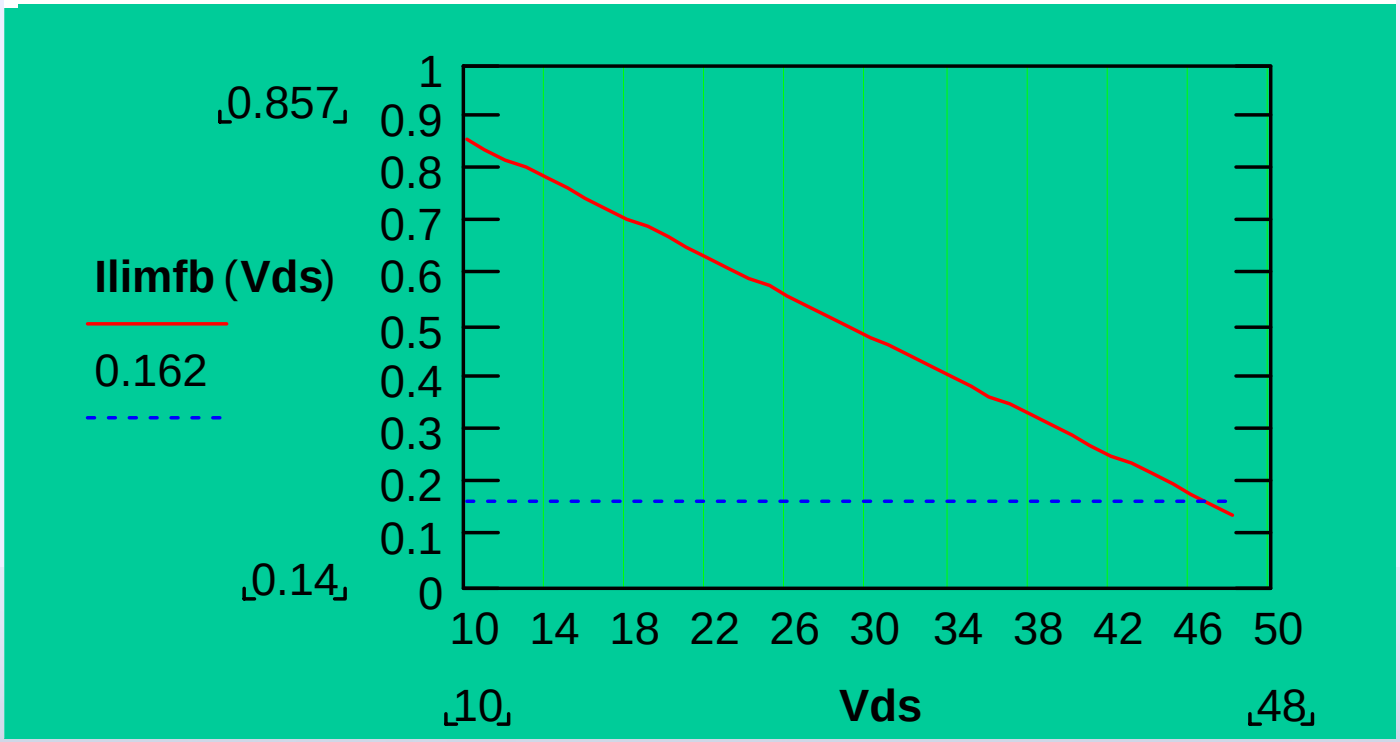
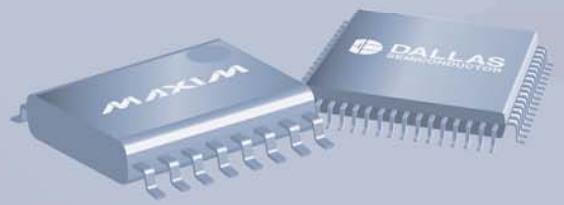


Example: PSE current limit as a linear function of Vds



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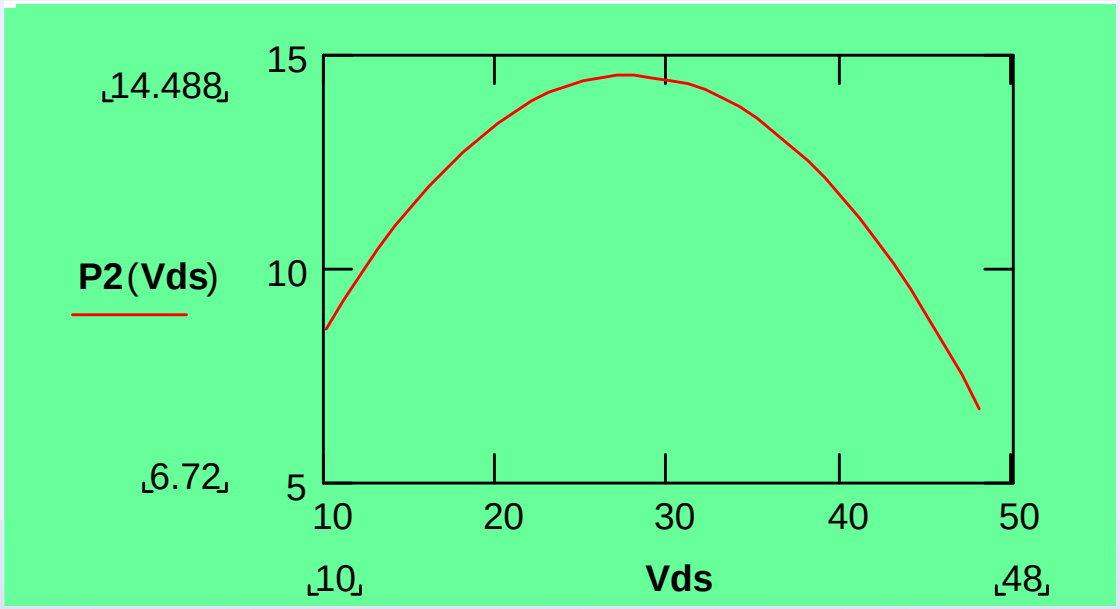
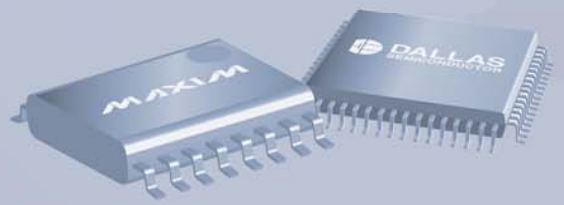


MOSFET power dissipation as a function of Vds. Peak power dissipation is 14.5W at Vds = 28V



Current Foldback for Type 2 PSE

- **Summary:**
  - In a type 2 PSE, A simple current foldback implementation can help maintain the PSE MOSFET in its safe operating area.
  - Current foldback allows the PSE to sustain port power during transient condition.