PoE+ System Current Limit Consideration for Input Transient and PD Load Step

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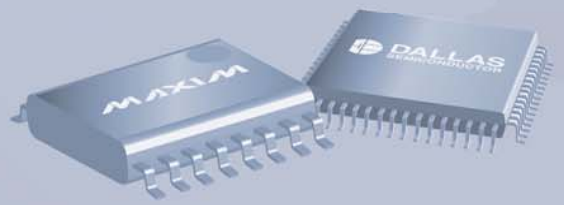
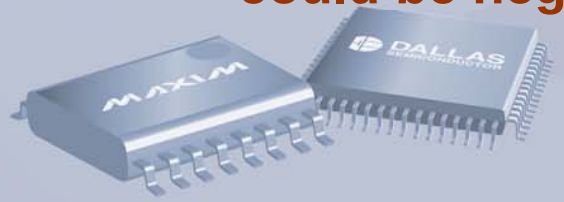
Maxim Integrated Products



PoE+ System Consideration

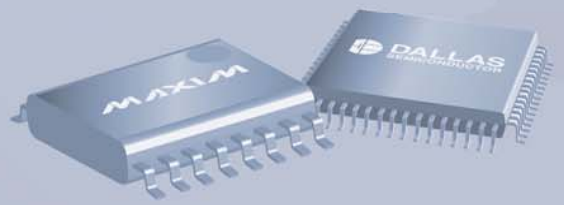
- **PoE+ System Requirements:**
  - System Inter-Operability
  - Allow Safe Maximum Possible Power Delivered from PSE to PD
  - Adhere to the Maximum Current Allowed *:
    - In the Cable
    - In the Connector
    - In the Patch Panel
    - In the LAN Magnetics
  - Backward Compatible w/ 802.3af Legacy Devices
  - Support 180uF capacitor on PD
  - Simplify Compliant Testing

*Note: Maximum current value for cable, connector, and patch panel are determined by heating effect which causes by DC/rms current. Low level transient current that lasted less than a few seconds does not cause significant heating and could be neglected



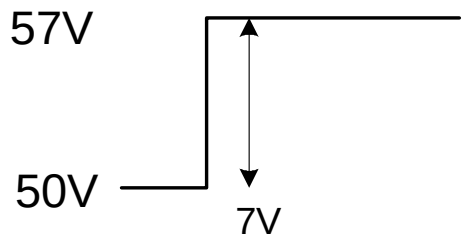
PoE+ System Consideration

- **PSE Requirements:**
  - Handle Input Power Supply Voltage Transient
  - Protect Port Short Circuit Condition
  - Provide Maxim Power to the PD as Allowed by PoE+ System
- **PD Requirements:**
  - Input Ripple Current
  - Load Step Transient

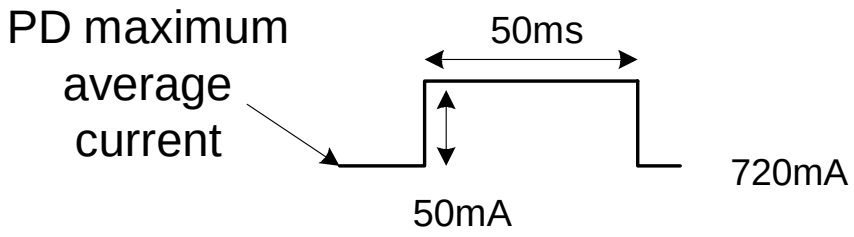


PoE+ System Consideration

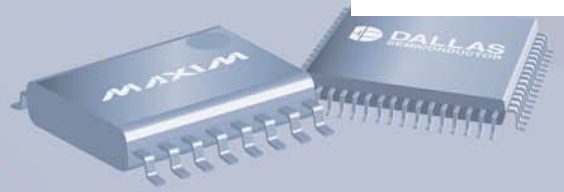
This Presentation focus on input voltage transient and PD load step



PSE Input Supply Voltage Transient



PD Current Load Step (Seen from PD's Input)

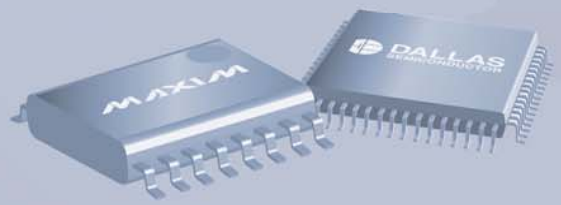


PSE - 802.3 af & at; Table 33-5

		802.3af		802.3at		
		min	max	min	max	
Output Voltage	Vport	44	57	50	57	V
Overload Current	Icut	15.4W/ Vport	400	36W/ Vport*	TBD (823?)*	mA
Output Current Limit	Ilim	400	450	TBD (823?)*	TBD (926?)*	mA
Current Limit Timeout	Tlim	50	75	50	75	ms

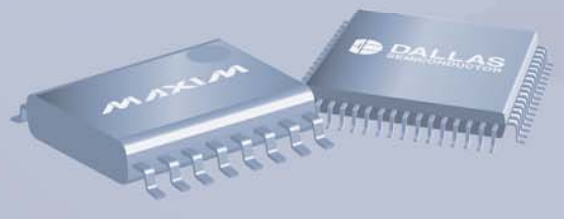
* PD can draw an average current up to Icut min: 350mA for af and 720mA for at

* Scaled up from 720mA/350mA ratio



PD - 802.3 af & at Table 33-12

		802.3af		802.3at		
		min	max	min	max	
Input Voltage	Vport	36	57	40	57	V
Port Power	Pport		12.95		29.52	W
Inrush Current	Iinrush		400		400	mA
Peak Operating Current 50ms, 5% Duty Cycle max	Iport		400		TBD	mA
DC or RMS Current @ 37V @41V @57V	Iport		350 - 230		- 720 520	mA

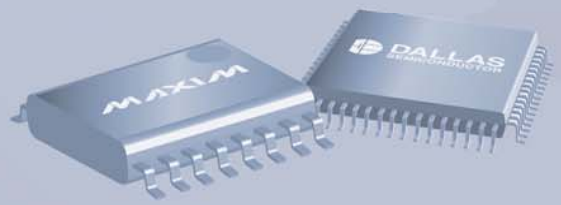


Note: For PoE+ system

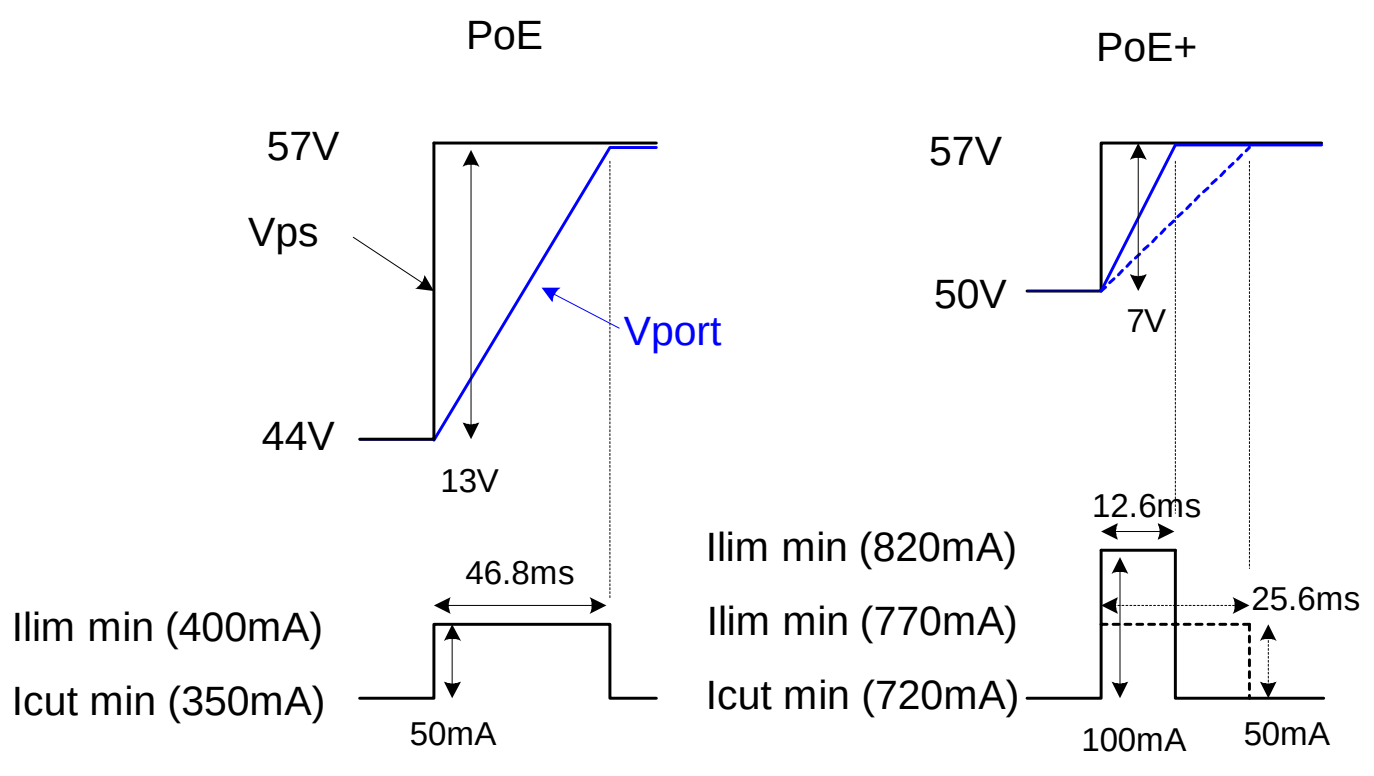
1. Input voltage step is from 50V to 57V (7V) versus 44V to 57V (13V) in af.

2. Using the same ratio of Ilim min / Icut min. The Difference (Ilim min – Icut min) is (823 – 720) = 103mA versus (400 – 350) = 50mA in af.

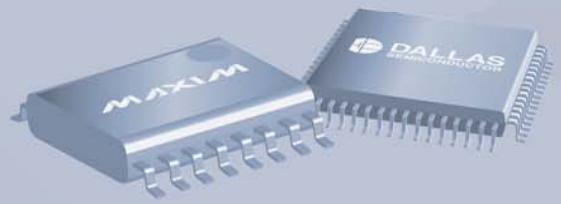
Using the same 50ms Tlim limit → In PoE+ system, during an input voltage transient: There is more current charging the PD's 180uF capacitor and less voltage step to charge the capacitor to, so there is extra current and time to handle a simultaneous PD load step.



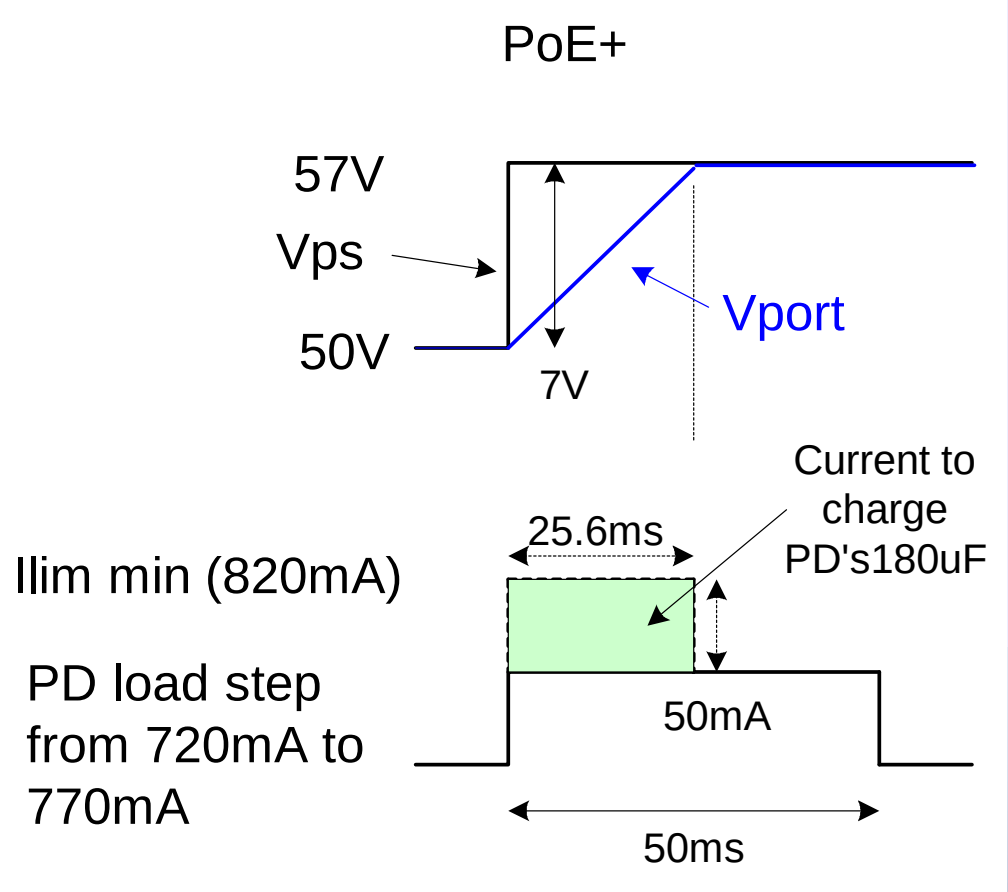
Input Voltage Transient:



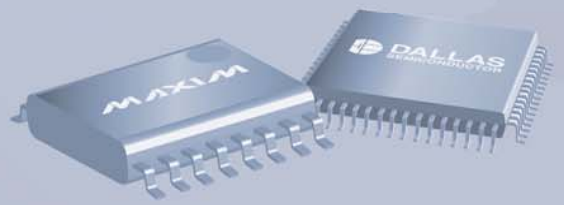
In PoE+ system, there is plenty of head room to handle input transient and PD load step at the same time



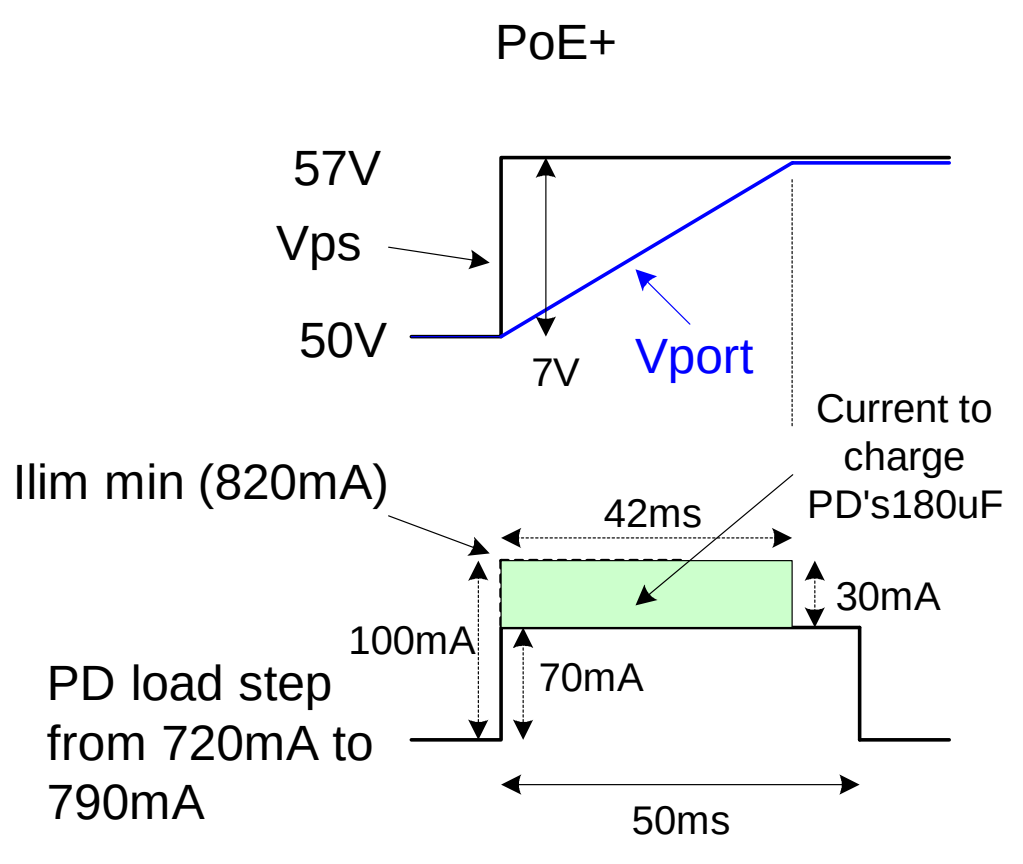
Input Voltage Transient & PD Load Step:



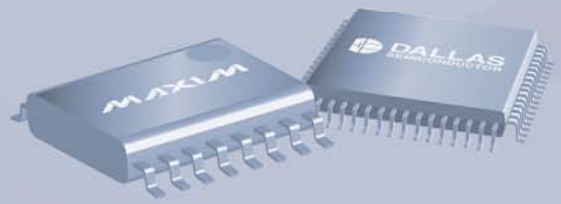
System operates perfectly throughout a simultaneous input voltage transient and PD load step. The PD load step is 50mA above its maximum average current for 50ms.



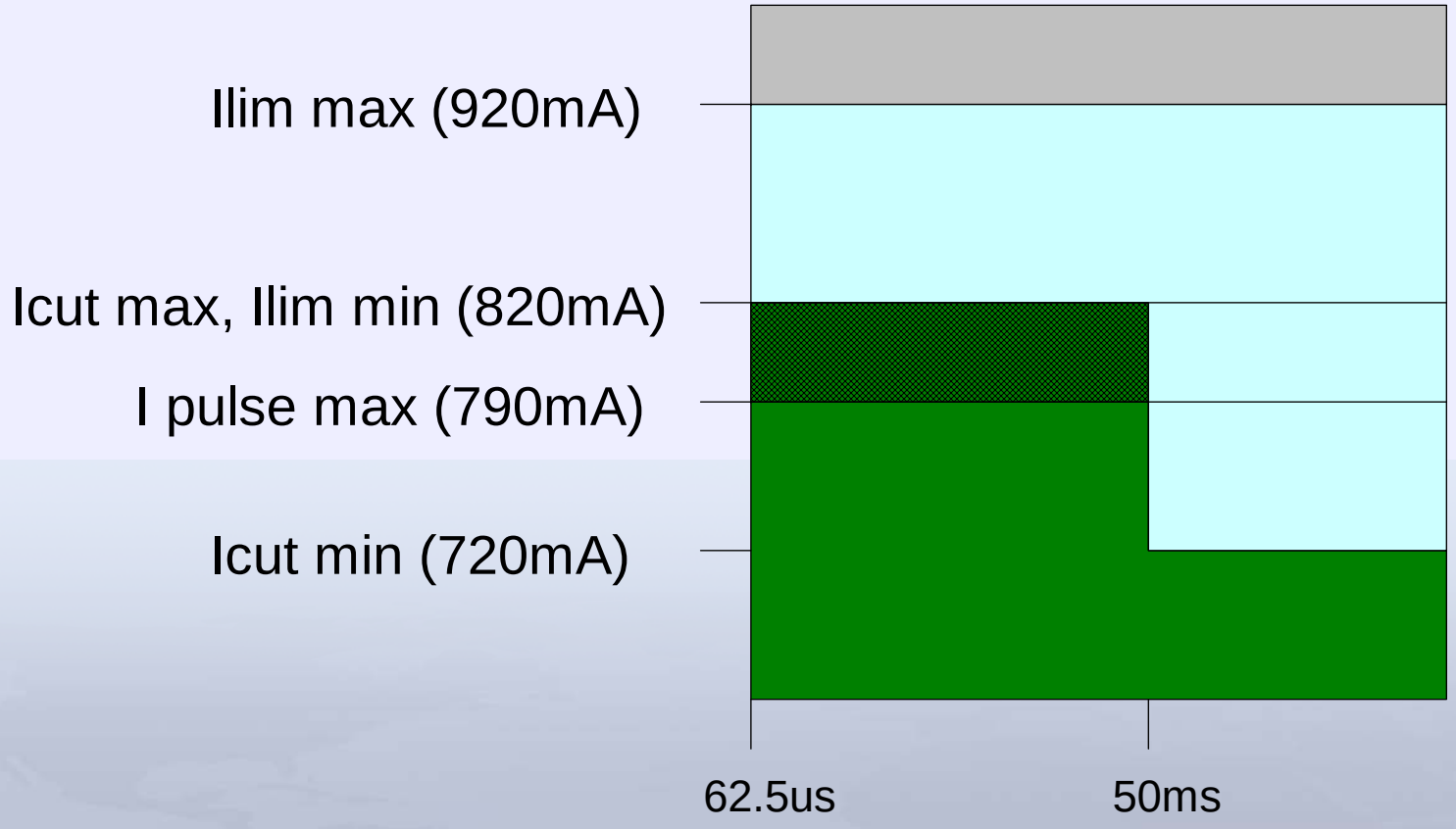
Input Voltage Transient & PD Load Step:

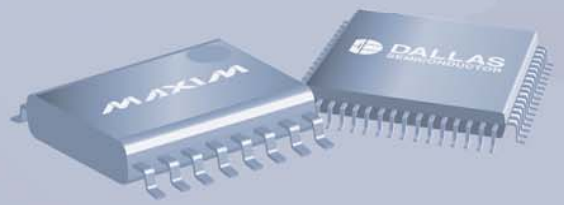


System operates perfectly throughout a simultaneous input voltage transient and PD load step. The PD load step is 70mA above its maximum average current for 50ms.



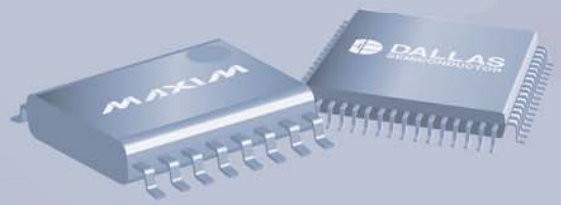
Proposal - Graphical Illustration





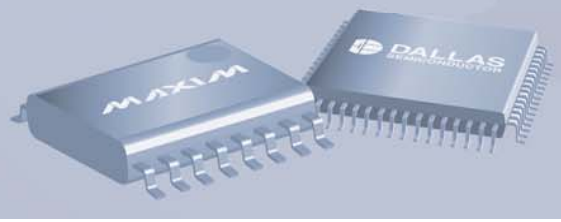
Proposal for PSE - 802.3 af & at; Table 33-5

		802.3af		802.3at		
		min	max	min	max	
Output Voltage	Vport	44	57	50	57	V
Overload Current	Icut	15.4W/ Vport	400	36W/V port	823	mA
Overload Time Limit	Tovld	50	75	50	75	ms
Output Current Limit	Ilim	400	450	823	926	mA
Current Limit Timeout	Tlim	50	75	50	75	ms

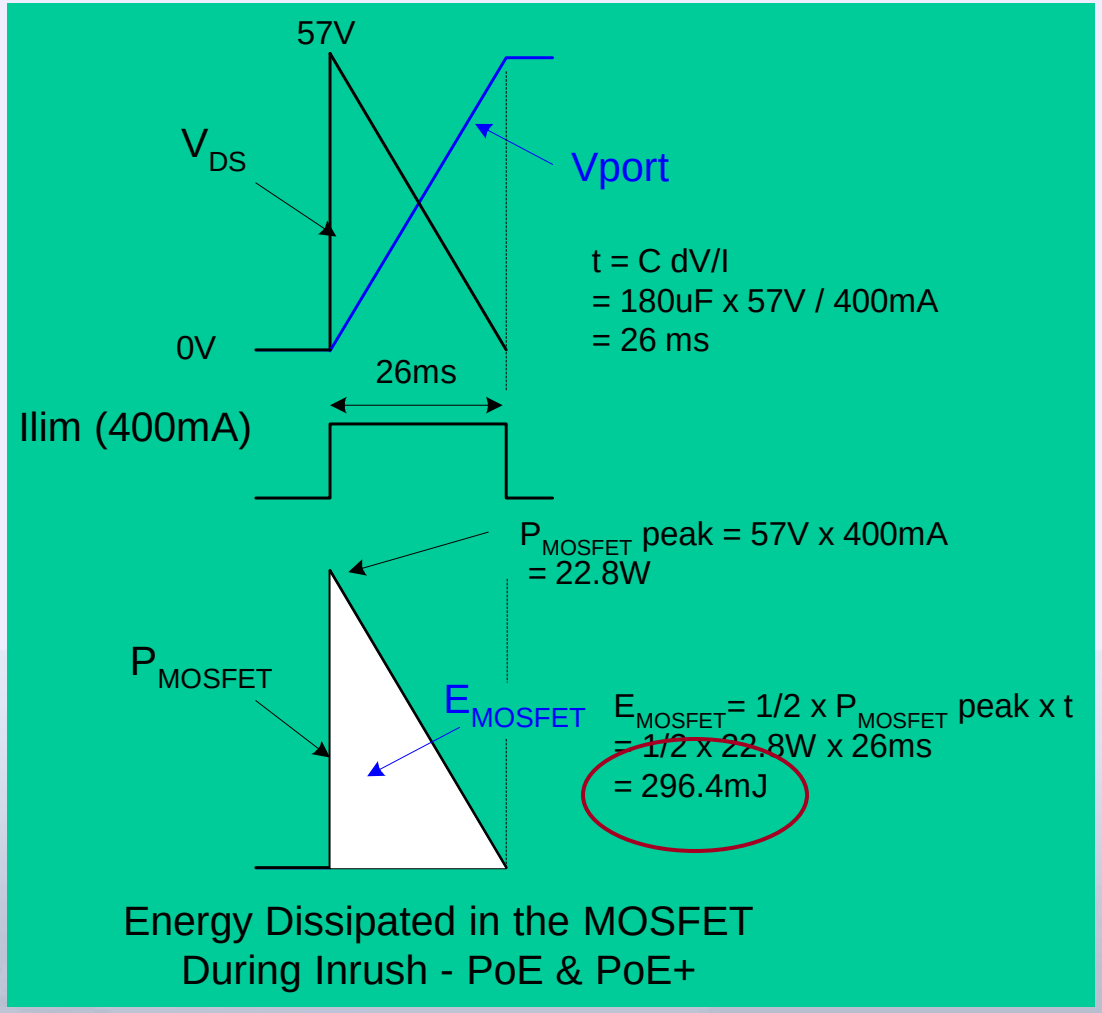


Proposal for PD - 802.3 af & at Table 33-12

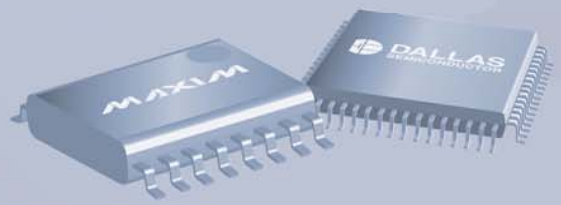
		802.3af		802.3at		
		min	max	min	max	
Input Voltage	Vport	36	57	40	57	V
Port Power	Pport		12.95		29.52	W
Inrush Current	Iinrush		400		400	mA
Peak Operating Current 50ms, 5% Duty Cycle max	Iport		400		~~823~~ 790	mA
DC or RMS Current @ 37V @41V @57V	Iport		350 - 230		- 720 520	mA



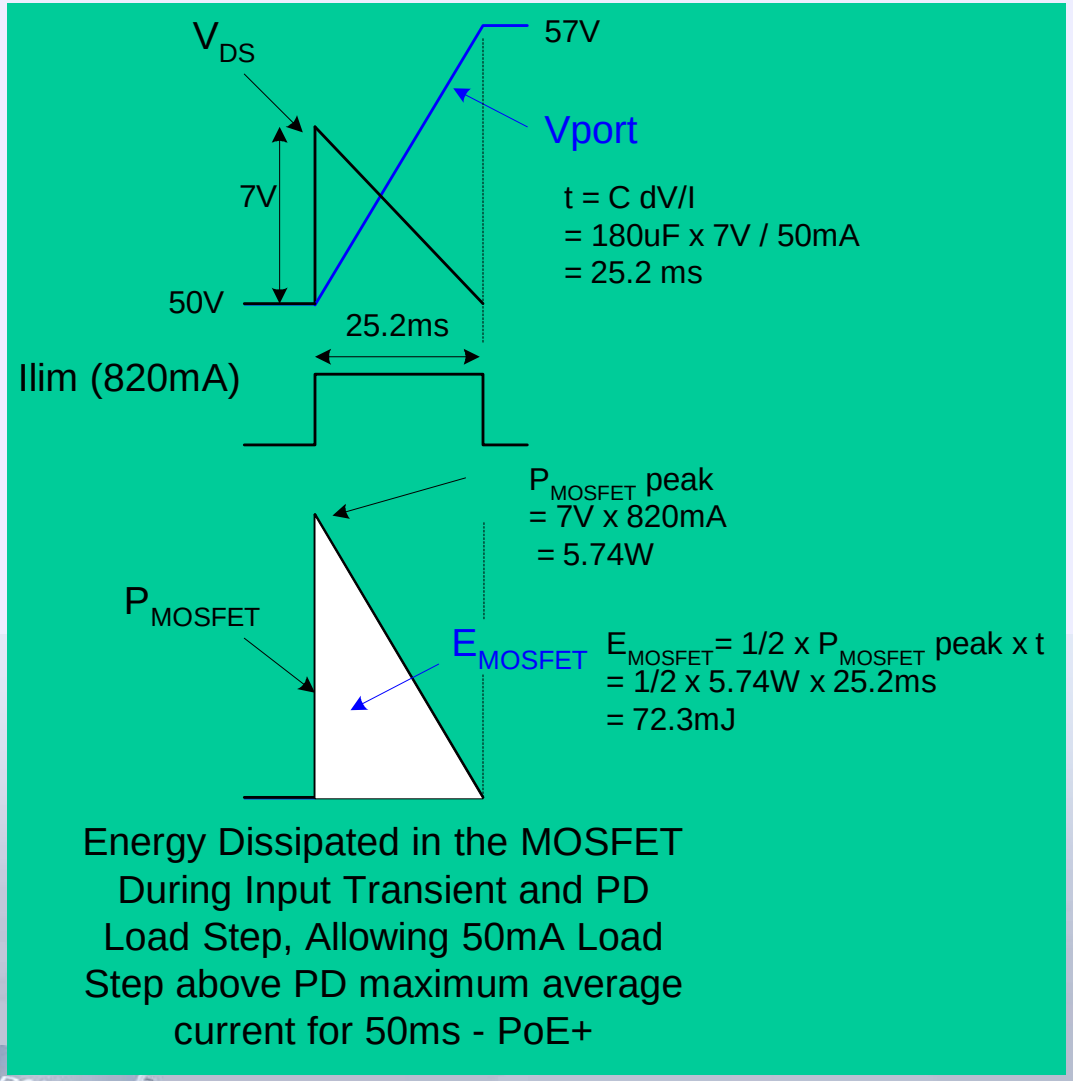
MOSFET Power Dissipation Calculation



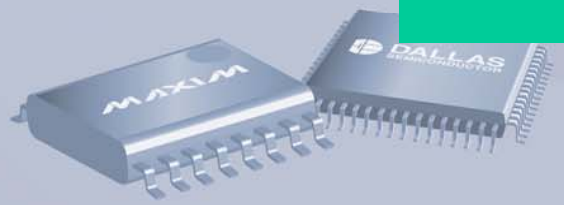
Energy Dissipated in the MOSFET
During Inrush - PoE & PoE+



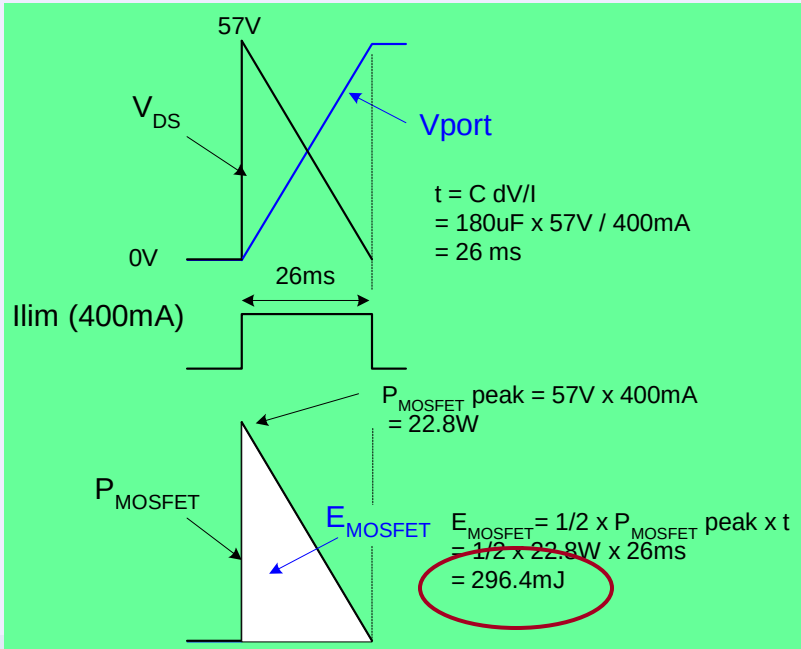
MOSFET Power Dissipation Calculation



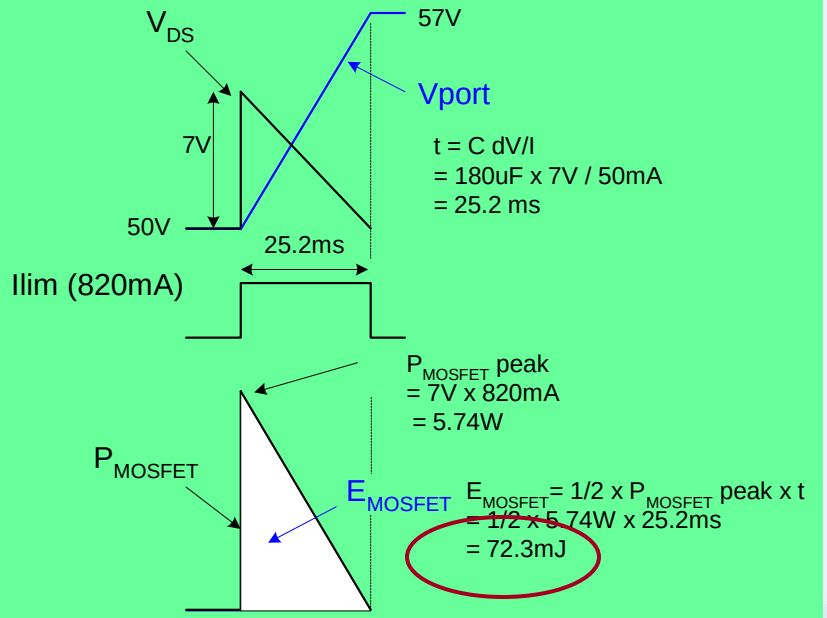
Energy Dissipated in the MOSFET During Input Transient and PD Load Step, Allowing 50mA Load Step above PD maximum average current for 50ms - PoE+



MOSFET Power Dissipation Calculation

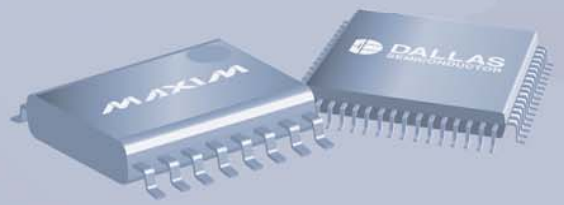


Energy Dissipated in the MOSFET During Inrush - PoE & PoE+



Energy Dissipated in the MOSFET During Input Transient and PD Load Step, Allowing 50mA Load Step above PD maximum average current for 50ms - PoE+

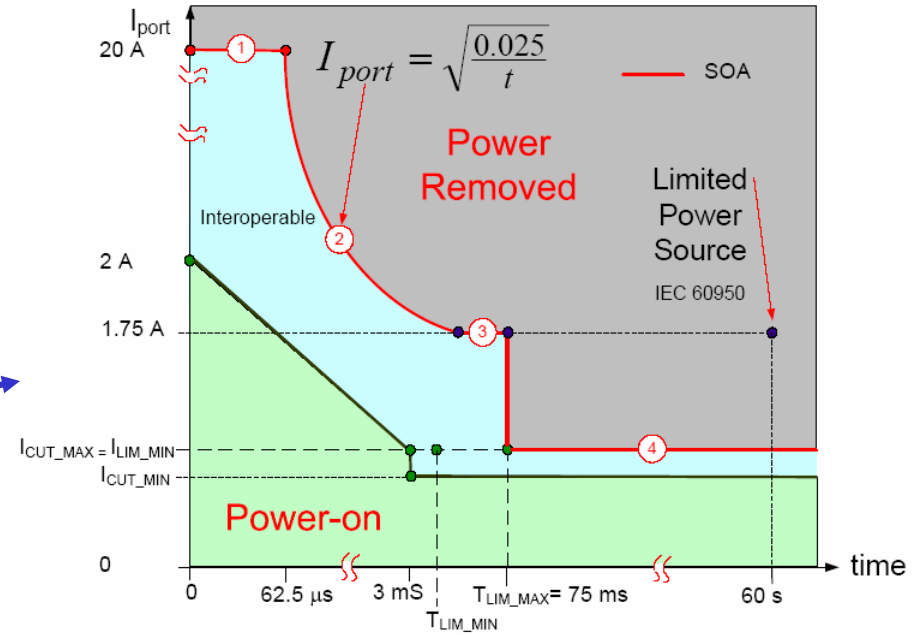
→ MOSFET Power Dissipation Dominates During Inrush Period

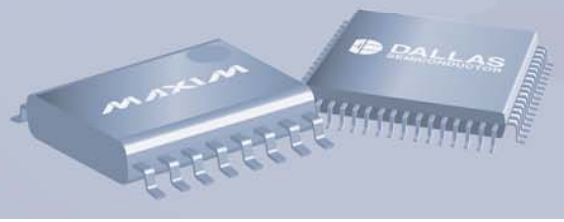


PoE+ System Consideration

- **Question:**
  - **Does High Pulse Current (2A for 6ms) Affect the LAN Magnetics?**
    - **Core Saturation?**
    - **Data Corruption?**

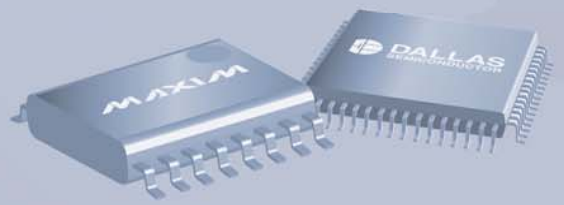
Graph is from the Vport Ad-Hoc presentation





Summary: For PoE+ System

- PSE Current Limit Based Can Easily Handle Simultaneous Input Voltage Transient and PD's Load Step
- PSE Current Limit Assures Port Current ≤ 926mA for ≤ 75ms
- PSE Current Limit Based Eases Compliant Testing
- Power Dissipation in the MOSFET is Highest During Inrush Period, not During Input Transient
- Question: If Port Current is not Limited, Does High Pulse Current (2A for 2ms) During Input Transient Affect the LAN Magnetics?
  - Core Saturation?
  - Data Corruption?



Appendix

- **Motor Load Current, at PD load side, un-filtered**