Vport ad hoc Current Limits
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Three ad hocs with an average attendance of 19 people since the last IEEE meeting.
People that attended since the last IEEE meeting are shown in **bold.**

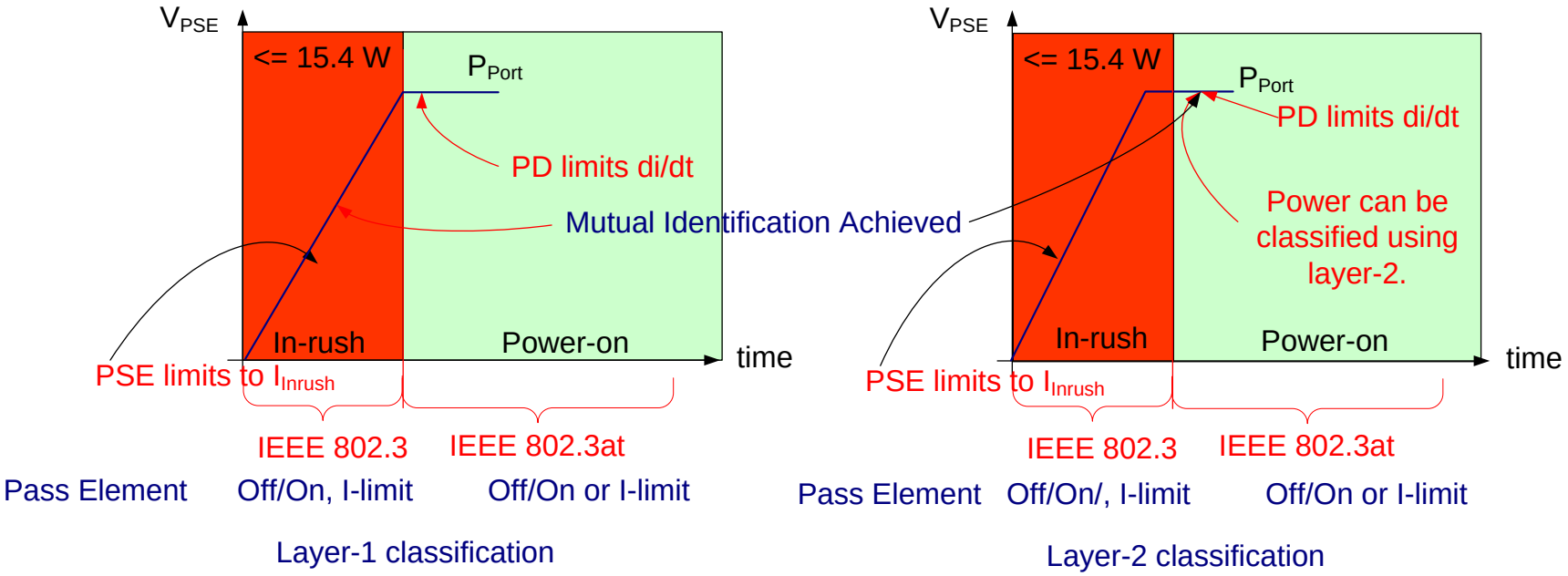
Agenda

- **Review current limit development.**
- **Motion for adoption of current limits.**
- **Next step.**

IEEE 802.3 vs IEEE 802.3at

- **Reuses the legacy in-rush current limits.**
- **Raises power-on currents.**
- **Limits PD di/dt rates during power-on.**
- **Opens up the design space to allow:**
  - **Scaled legacy current thresholds**
  - **Aggressive fold back**
  - **An energy based limit**

System In-rush and Power-on



Parameter		802.3	802.3at
I_{LIM}	max.	$\frac{450}{400}\frac{400}{350}\frac{P_{Port}}{V_{Port}}$	New
	min.	$\frac{400}{350}\frac{P_{Port}}{V_{Port}}$	
I_{CUT}	max.		
	min.	$\frac{P_{Port}}{V_{Port}}$	

System Concerns being addressed by I_{LIM}

- **Situations that lead to a PSE dv/dt rate that causes excess PD current demand.**

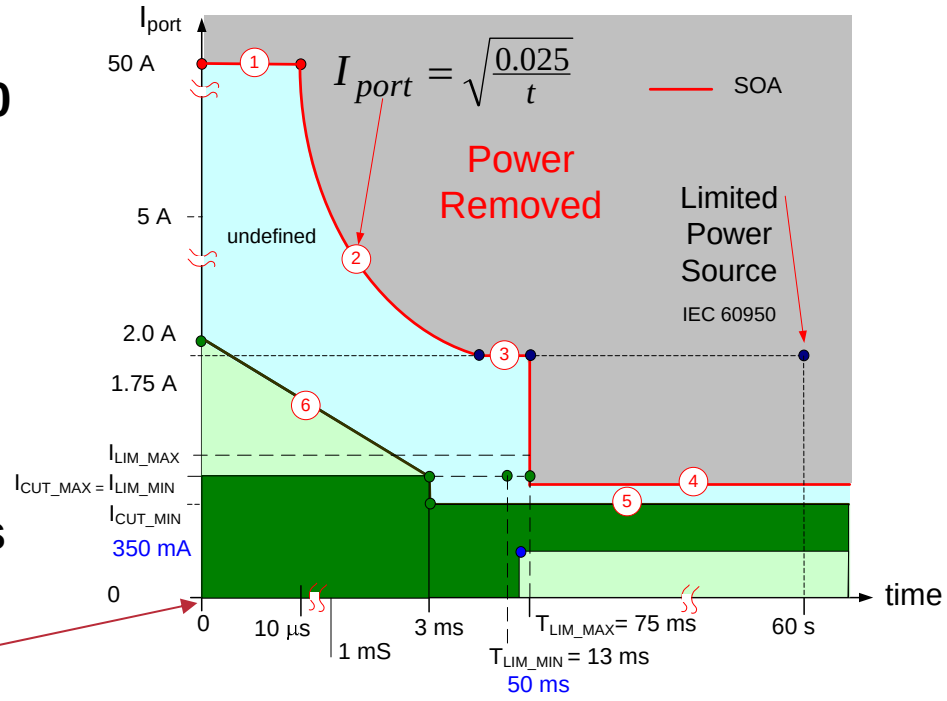
  Multiple PDs reducing their load.

  A PSE supply voltage change. ex/ Switching in a new power supply to deal with a power supply failure.

Creating the PSE SOA

(1) Peak PSE Current

- **Maximum PSE voltage change 50 to 57 V; 7 V.**
- **Minimum path resistance $R_{distribution} + R_{port} + R_{channel} = 0.08 + 0.9 + 0.8 = 1.78\ \Omega$**
- **Peak current = 7/1.78 = 3.9 A This is for an instantaneous change—which is not allowed.**
- **A 50 A current peak corresponds to a path resistance of 0.140 Ω**
- **t = 0 when I_{port} first exceeds I_{CUT_MIN}.**



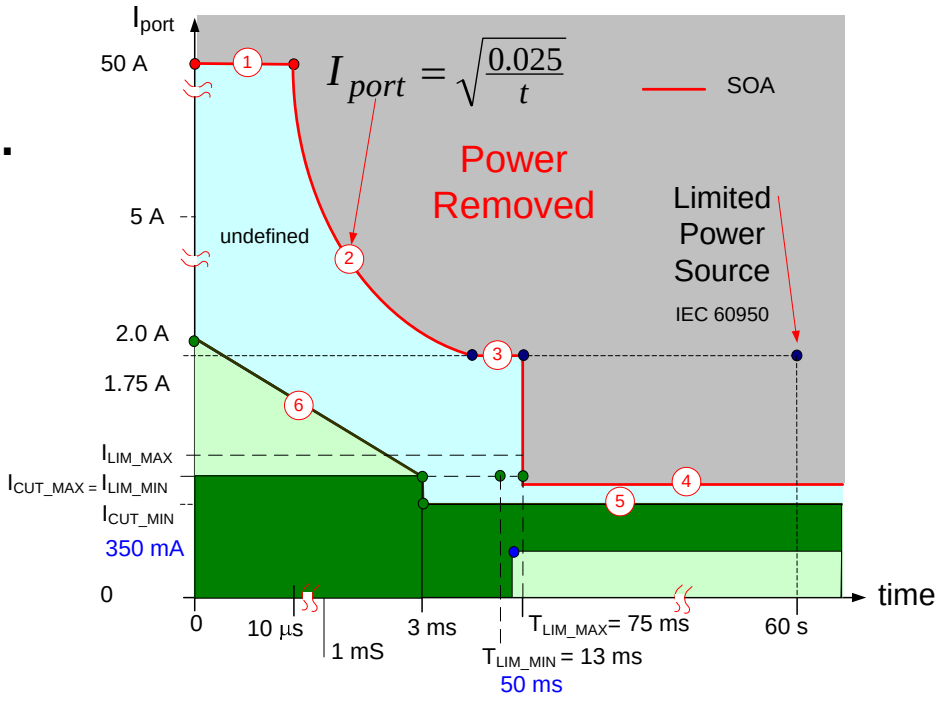
SOA = Safe Operating Area
The PSE droop transient permitted is to 46.2 V but is at a slow rate 0.03 V/µs.

Creating the PSE SOA

(2) Trace fusing equation

- **Is valid from section 1 to section 3.**
- **Compliance shall be tested from t = 1 mS.**

  t < 1 ms, PSE designers test for short-circuit events to ensure the reliability of their design.

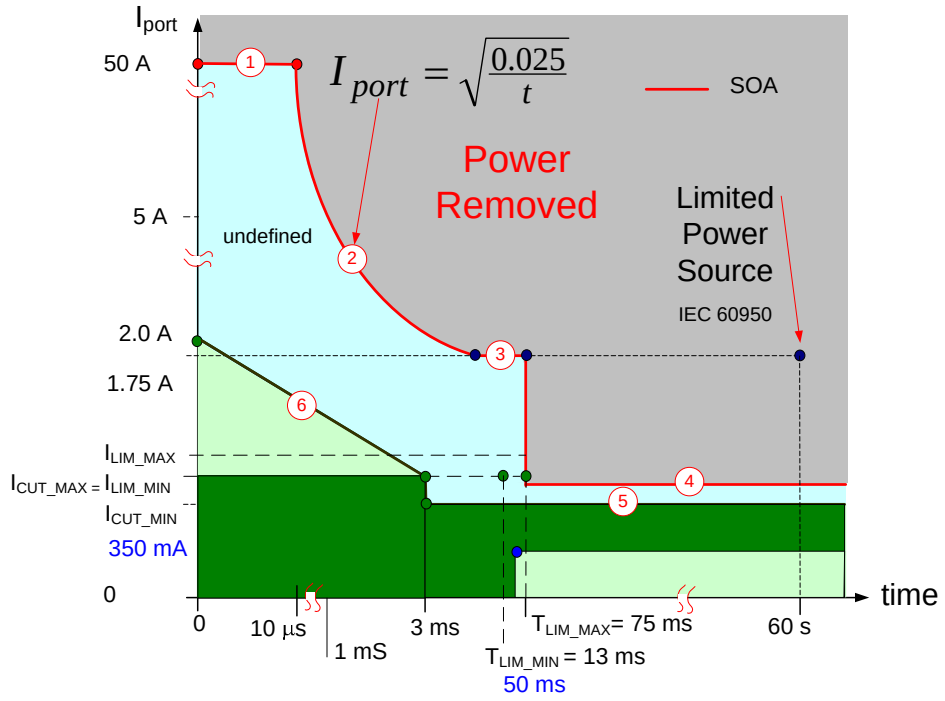


The source and parameters for the trace fuse equation are not documented. The equation was based on a time-scaled-version of I_{LIM}. The curve produced appears to be conservative (errors on the side of no damage by a factor greater than 10).

Creating the PSE SOA

(3) LPS implied limit

- **100 VA for 60 s over the operating range of 50 to 57 V.**
- **100/57 = 1.75 A**



Creating the PSE SOA

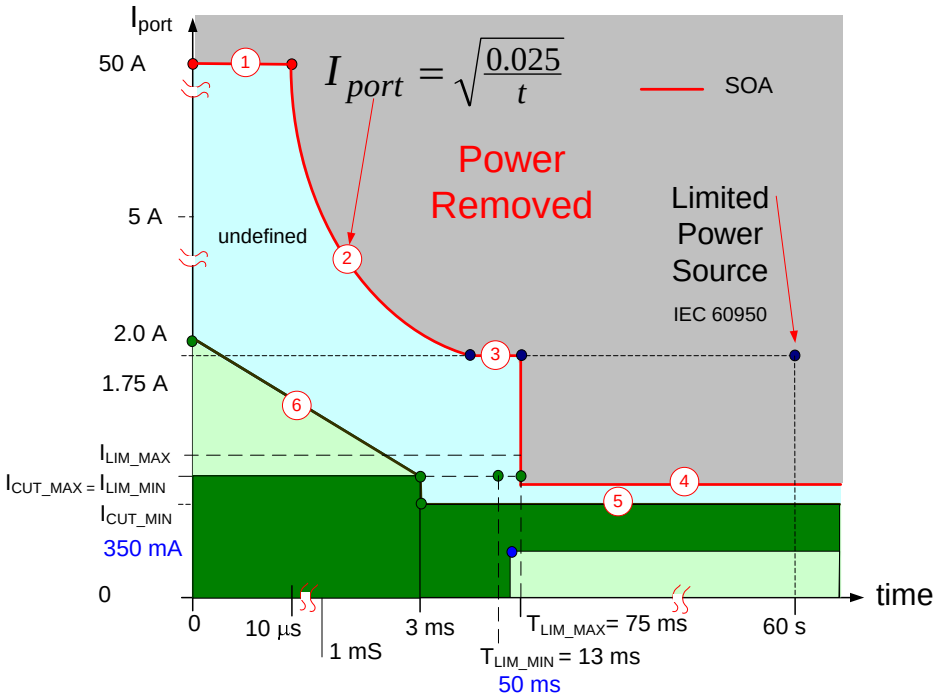
(4) Average Current

- There are no controls on how often a PSE voltage may change due to PD load changes.
- The repetition of the worst-case event is unlikely.
- Preserve existing system tolerances,
  $I_{LIM\_MAX}/I_{CUT\_MIN} = 450/350$

  $I_{LIM\_MIN}/I_{CUT\_MIN} = 400/350$

  $I_{segment\text{-}4} = I_{CABLE}\ 400/350$
- The long term system cable average is I_{CUT_MIN}.

Standards do not specify noncompliant solutions.



$I_{LIM\_MAX} = 720 \times 450/350 = 920\ mA$

$I_{CUT\_MIN} = I_{CABLE} = 720\ mA$

$T_{LIM\_MIN} = f(I_{LIM}, I_{CUT})$

Creating the PSE SOA

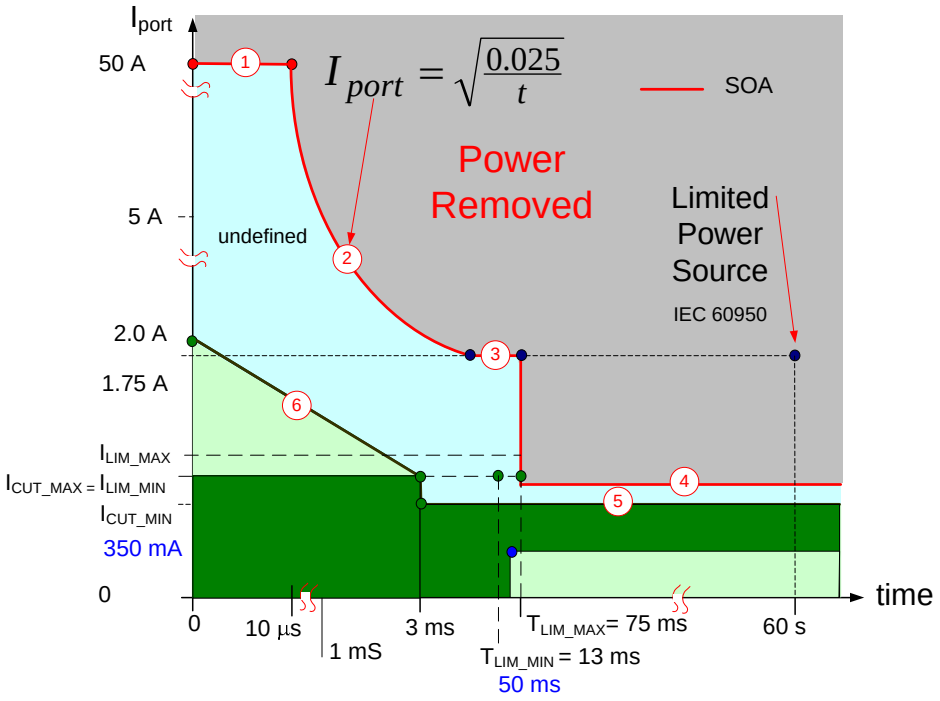
- **The PSE SOA curve ensures that:**
  - **IEC 60950 limits are met.**
  - **System damage does not occur.**
  - **The PD receives the power it has requested.**
  - **A large design space has been created.**
  - **It is independent of the cable interoperability limits.**

Straw Poll: Do you support the SOA curve?
Y: > 20 N: 0

Creating the PD Current Boundary

(5) Average Current

- **The PD is designed to draw less than I_{CUT_MIN} with a static port voltage.**
- **PD power compliance may be checked over a period of 1 s, or using the green boundary.**
- **A PD design must remain within the green zone.**



Note that segment 5 is less than I_{CUT_MIN} when a PD has current transients above I_{CUT_MIN} in order to ensure that class power is not exceeded.

Creating the PD Current Boundary

- **We need to reassess the need to mandating a PD current limit.**
- **Consider reusing the legacy requirement of imposing a PD current limit only when the PD capacitance exceeds 180 μF.**
- **This change permits PD:**

  Current transients due to dv/dt and/or load demands.

  Simplifies many designs (no current limit).

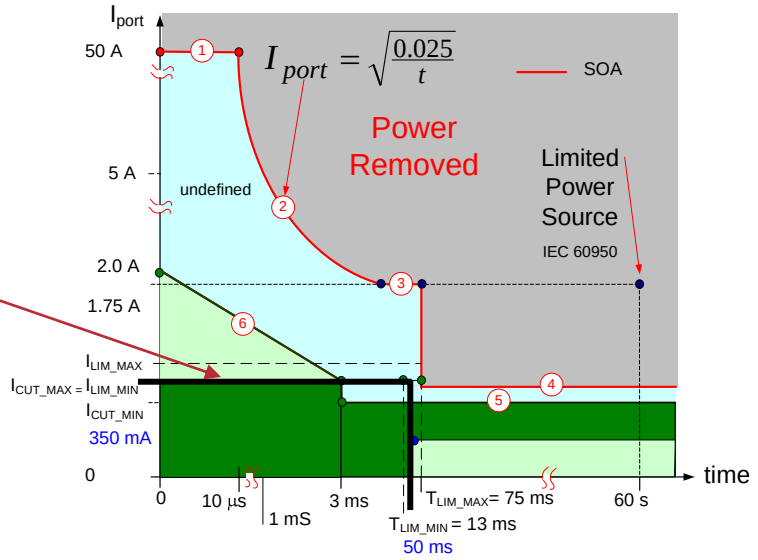
  Permits practical PDs to draw the maxim power.

Creating the PSE SOA

- **A current limiting PSE**

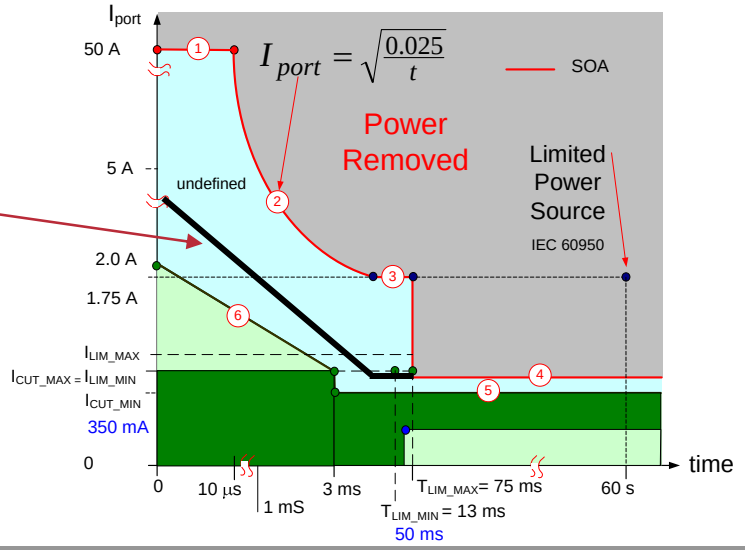
  Provides I_{LIM} for T_{LIM}

  PD power is removed above T_{LIM} or when Pclass has been exceed for 1 s.



- **An energy limiting PSE**

  Provides enough power to ensure the system can operate within the green zone. PD power is removed above the energy base limit.



System with a PSE voltage transient

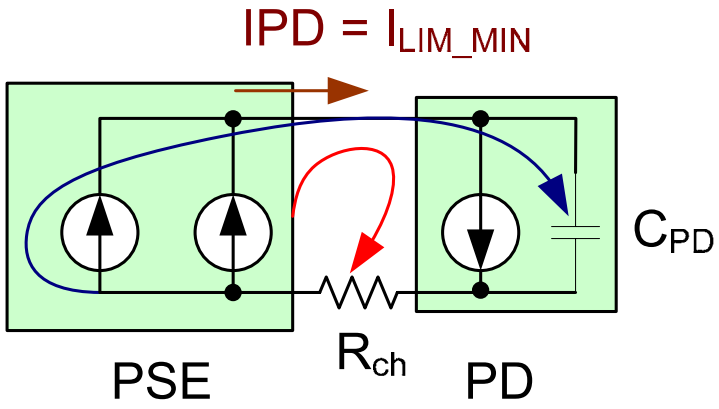
- **A PSE voltage increases due to a significant load drop or PSE supply backup.**
- **The PSE charges the PD until the system voltages stabilize.**
- **Both types of PSEs may result in the same PD charge profile when the path resistance between the PSE and PD are high.**
- **PSE methods differ when PD current demand is not limited by the path resistance.**

  A current limiting PSE charges up the PD at a constants current I_{LIM}.

  A energy limiting PSE charges up the PD at a current value determined by system resistance. This method is faster and places less stress on the PSE pass element.

$$R_{path} = R_{channel} + R_{PSE\_TH} + R_{PD\_TH}$$

Simplified System in Current Limit

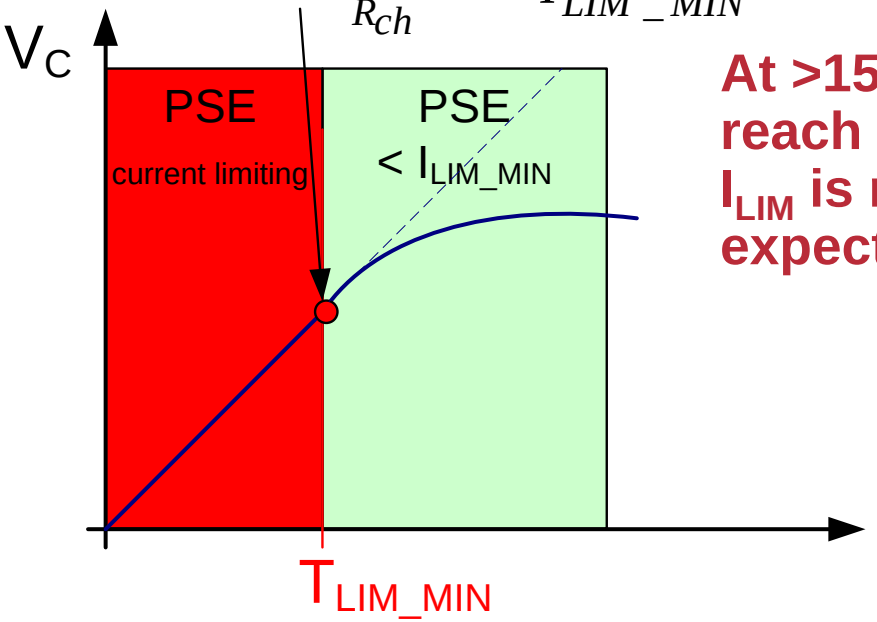


$I_{CPD} = I_{LIM\_MIN} - I_{CUT\_MIN}$

$$C_{PD}\frac{dv}{dt} < I_C$$

$$dt > C_{PD}\frac{dv}{I_C}$$

$$\frac{V_{PSE} - V_{PD}}{R_{ch}} = I_{LIM\_MIN}$$



At >15 m reach I_{LIM} is not expected

Short channel

Rch = 0, Constant I_{PD}
IEEE 802.3 T_{LIM} = 47 ms
IEEE 802.3at, T_{LIM} = 12.6 ms

Long channel

Rch = 20 or 12.5 Ω, Constant I_{PD}
IEEE 802.3 T_{LIM} = 43 ms
IEEE 802.3at, T_{LIM} = 10.4 ms

This simplified case assumes the PD always draws ICUT_MIN.

IEEE 802.3 Concern

- **A PD can legally draw 400 mA for 50 ms. Table 33-12, Item 4. A PSE can legally provide 400 mA for 50 ms. Table 33-5, Item 10 and 11.**
- **A system permitting this will not ensure interoperability when the PD is drawing its maximum allowable current and a PSE voltage transient occurs.**
- **A system with the PSE centered within the middle of its allowable range is not interoperable!!!**

$$C\frac{dv}{dt} = i = 180\mu F\ \frac{57V - 44V}{62.5mS} = 37.4mA = I_{PD} - 400mA, I_{PD} = 437mA$$

- **Proposed Solution:**
  Recommend that no more than I_{CUT_MIN} be drawn by a PD with a static port voltage.

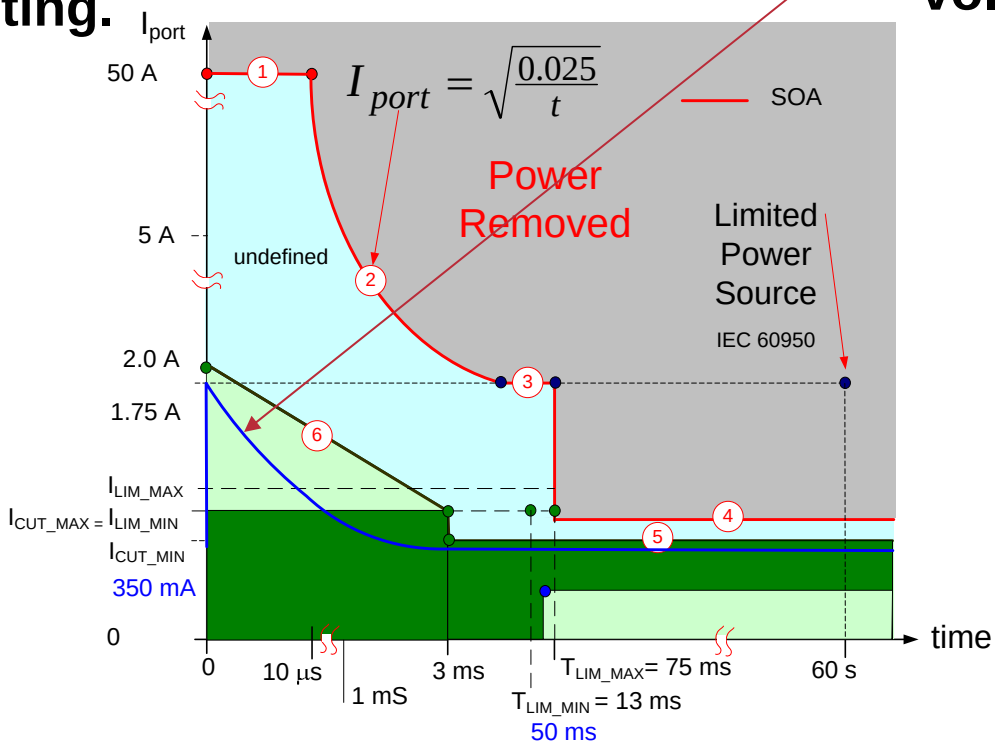
  IEEE 802.3at will use correct methods to begin with.

The previous IEEE Task Force may have allowed I_{CUT_MAX} (PSE) to ensure circuits could accommodated this current value, but expected no more than I_{CUT_MIN} to be drawn normally by the PD.

Energy based PSE does not current limit

The PSE pass element is on and not current limiting.

The PD is charging up to the new PSE voltage.

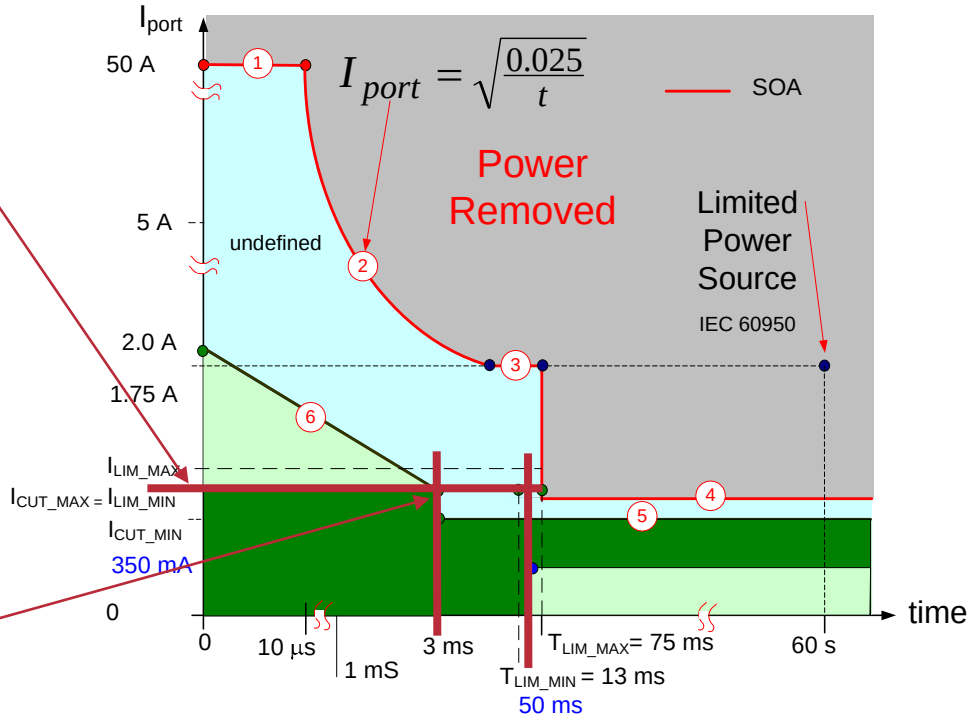


The light green boundary has 45% average margin above the simulated system needs.

Creating the PD Current Boundary

A PD can not draw demand more than I_{LIM}, because a current limiting PSE does not provide more than I_{LIM}.

A PD can not demand power at I_{LIM_MIN} longer than T_{LIM}, because an energy limiting PSE may not provide power for more than 3 ms.

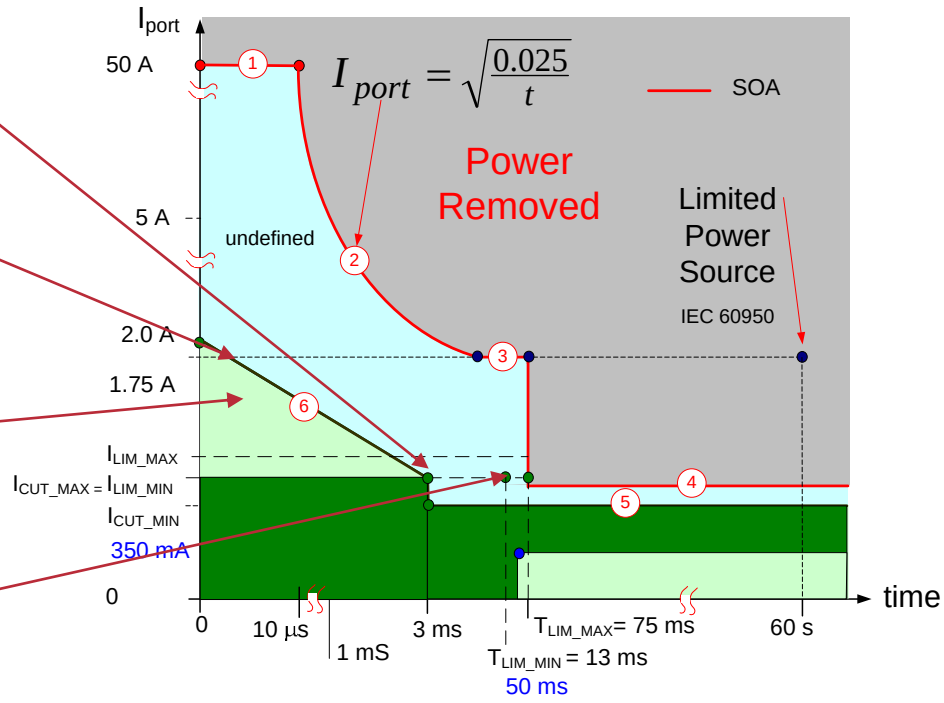


Creating the PD Current Boundary

A PD can demand I_{CUT_MAX} for 3 mS.

A PD may demand up to segment-6 current due to a MDI dv/dt increase.

PSEs using energy based power transfer methods shall operate within this region.

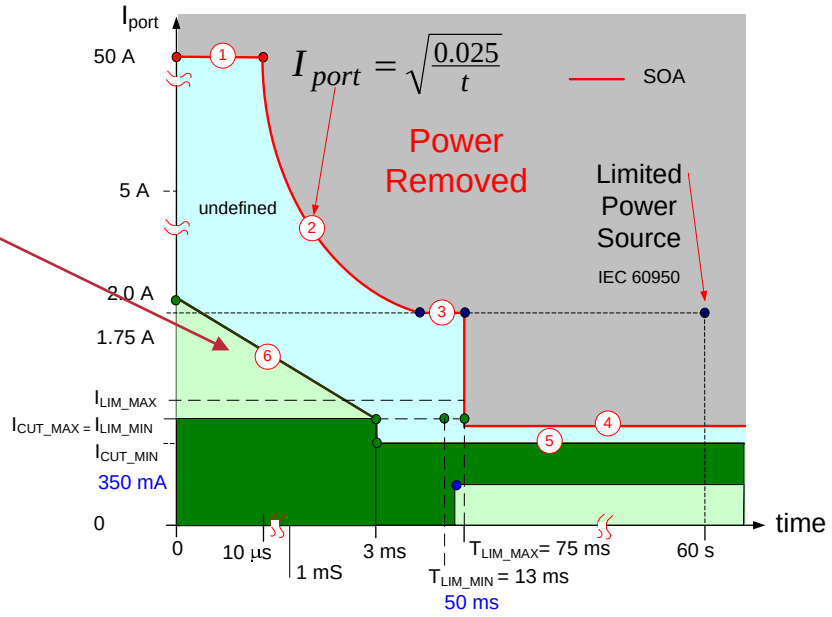


PSEs using current limiting shall supply a constant current of at least I_{LIM_MIN} for at least T_{LIM_LIM}. $T_{LIM\_MIN} = F(I_{LIM\_MIN}, I_{CABLE})$

Creating the PD Current Boundary

(6) Transient Current

- **A PD may draw I_{CUT_MIN} for 3 ms with a static port voltage. A PD may use the margin between where it operates and where the specification permits a PD to operate for its demand current.**
- **The specification should provide a system model to use.**

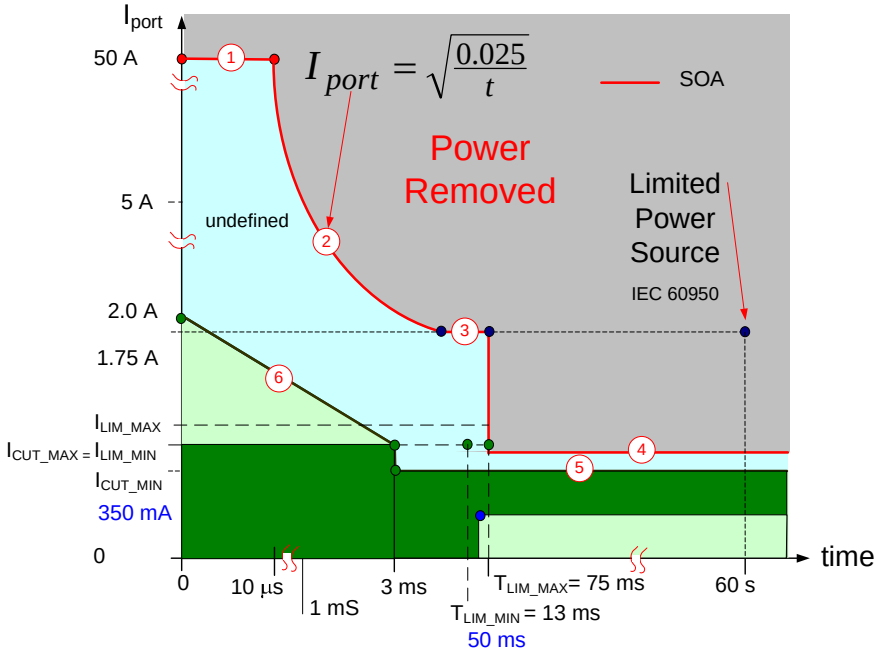


Does the group want to have T_{LIM} include the extra 3 ms?

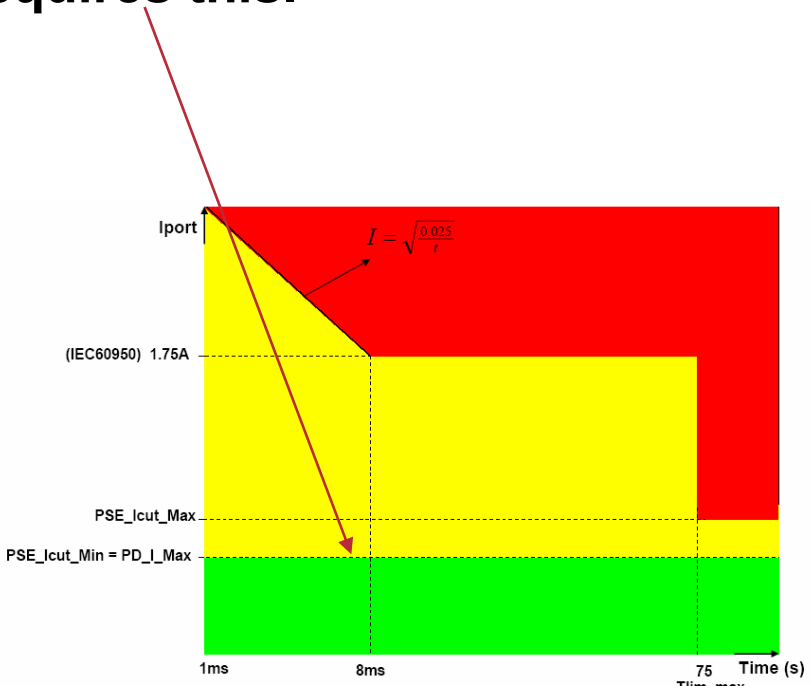
A PSE could supply I_{LIM_MIN} for T_{LIM_MIN} + 3 ms, and this would increase interoperability because a PD could then demand a load of I_{LIM_MIN} for 3 ms and support a worst-case MDI dv/dt.
The value selected for T_{LIM} can reflect this consideration.

Creating the PD Current Boundary

The Geneva PD Motion passed to requires this.



Option-A



Option-B

A PD that imposes a current limit needs to ensure that the limit selected permits a PSE to fully charge its Cpd before the PSE could remove its power.

Creating the PD Current Boundary

Advantages of PD current limit.

A simpler specification and system operation.

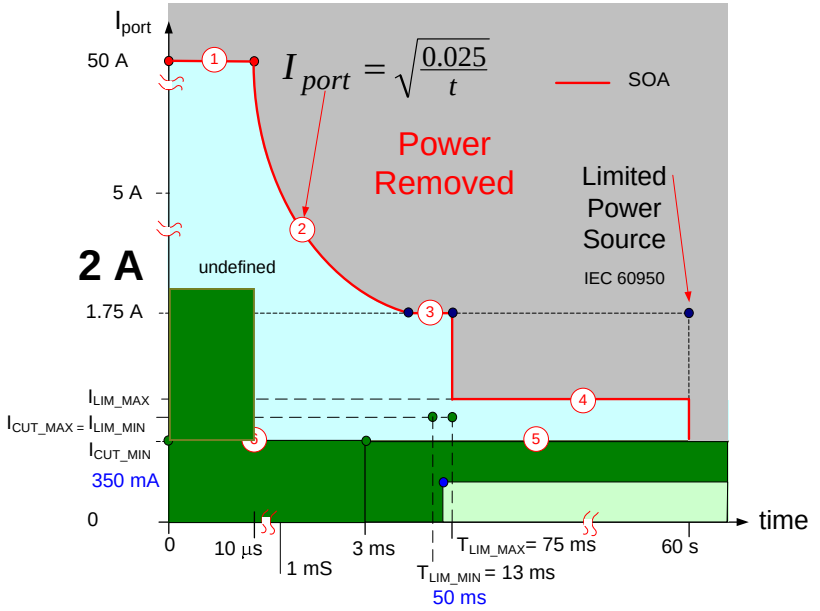
No I_{CUT}, I_{LIM}, T_{CUT}, T_{LIM}

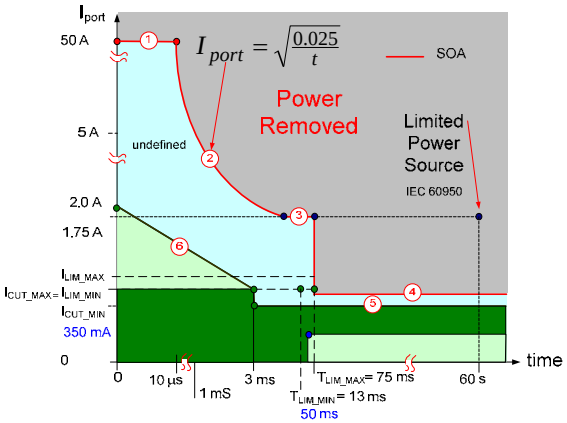
PSE dv/dt transients are handled by the PD.

PSE only monitors the SOA.

All known PD vendors (9) limit current at the PD now.

- No transient power above average, and the upper power limit is impaired by the tolerance of the current limit.





Do we want a PD current limit requirement?

If so, is a current limit of I_{CUT_MIN} acceptable?

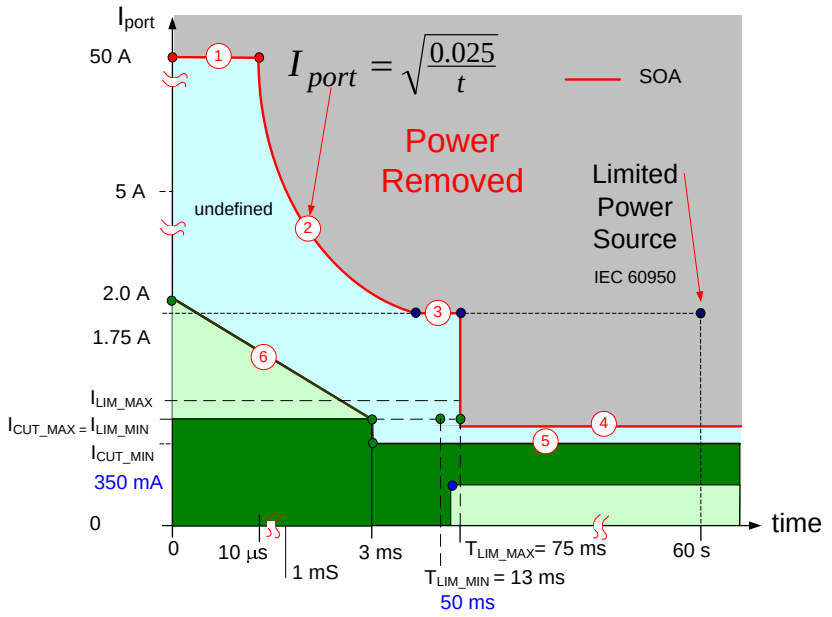
Poll

Under static port voltage conditions, a PD will not draw more than I_{CUT_MAX} for longer than 3ms.

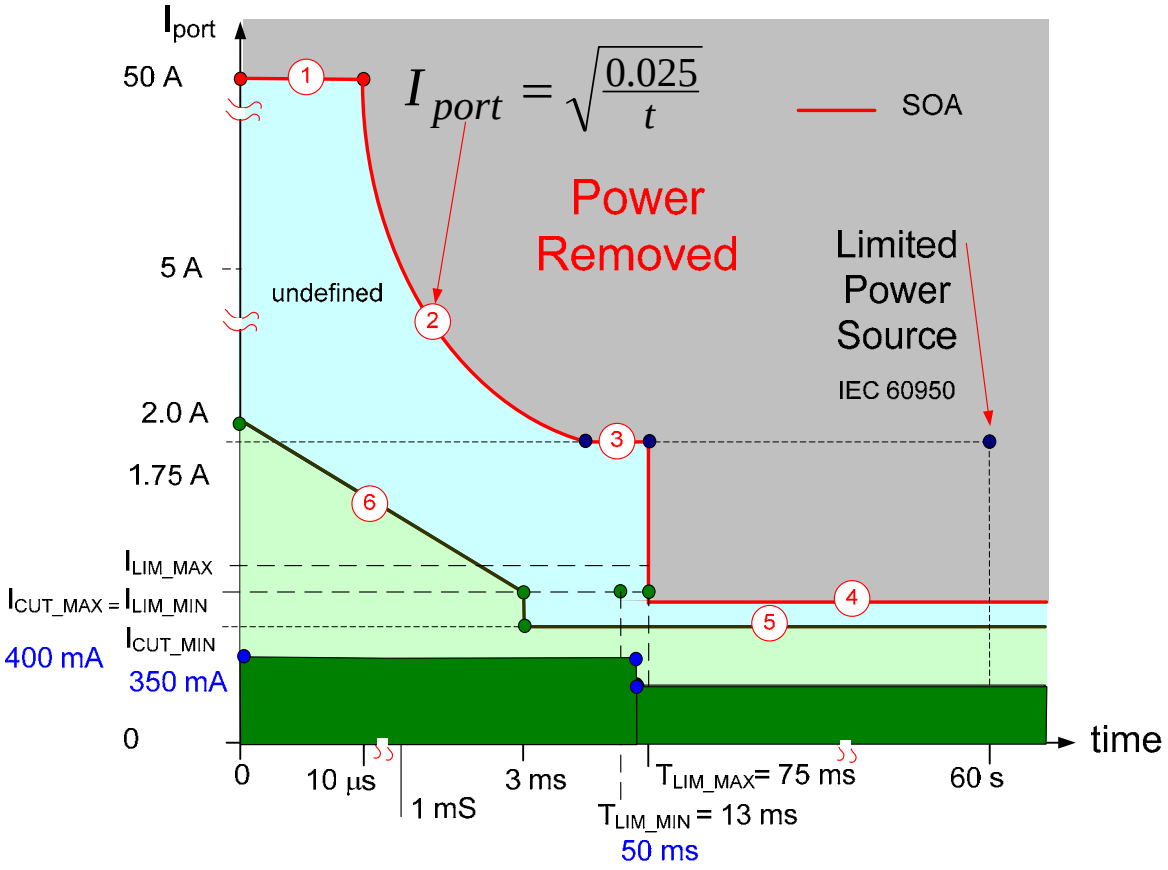
Yea: 9

Nay: 6

Abstain: 4

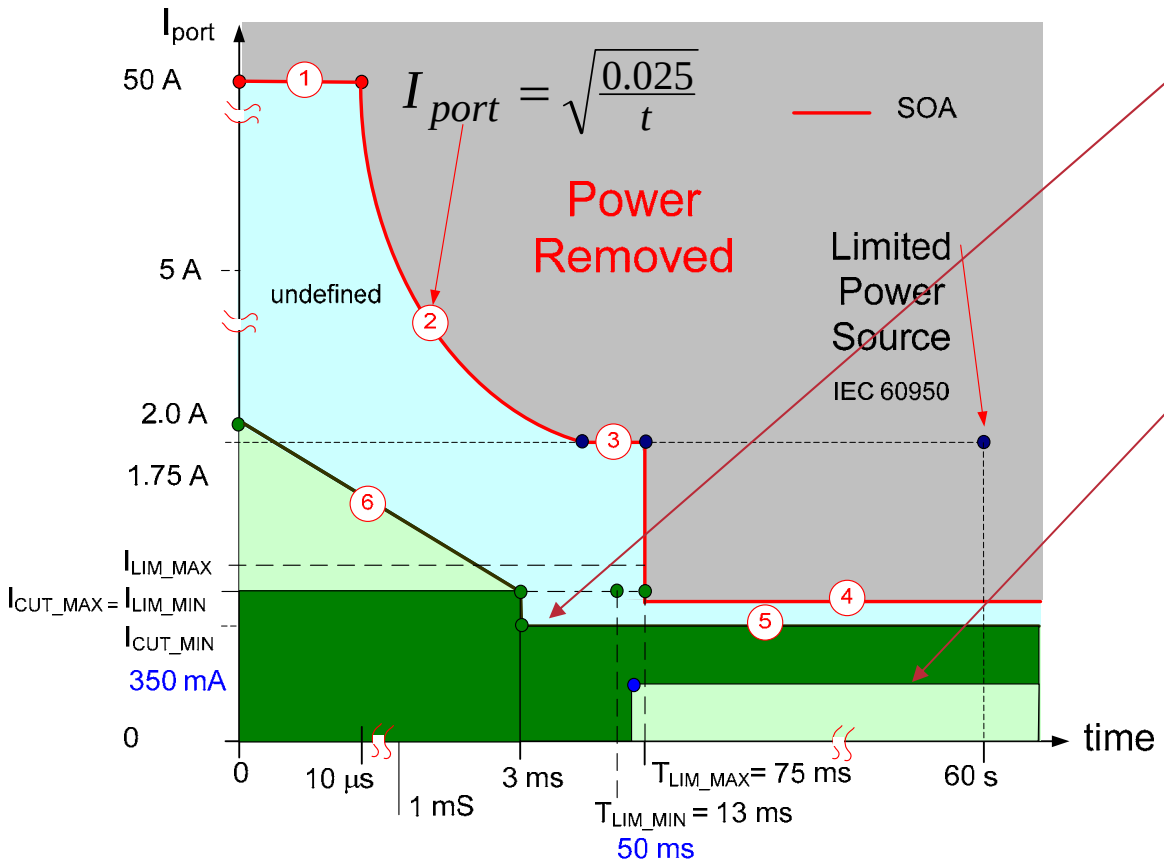


Creating the PD Current Boundary



This shows a legacy PD within the proposed AT curve.

Creating the PD Current Boundary



A type-2 PSE will over provision power for a type-1 PD.

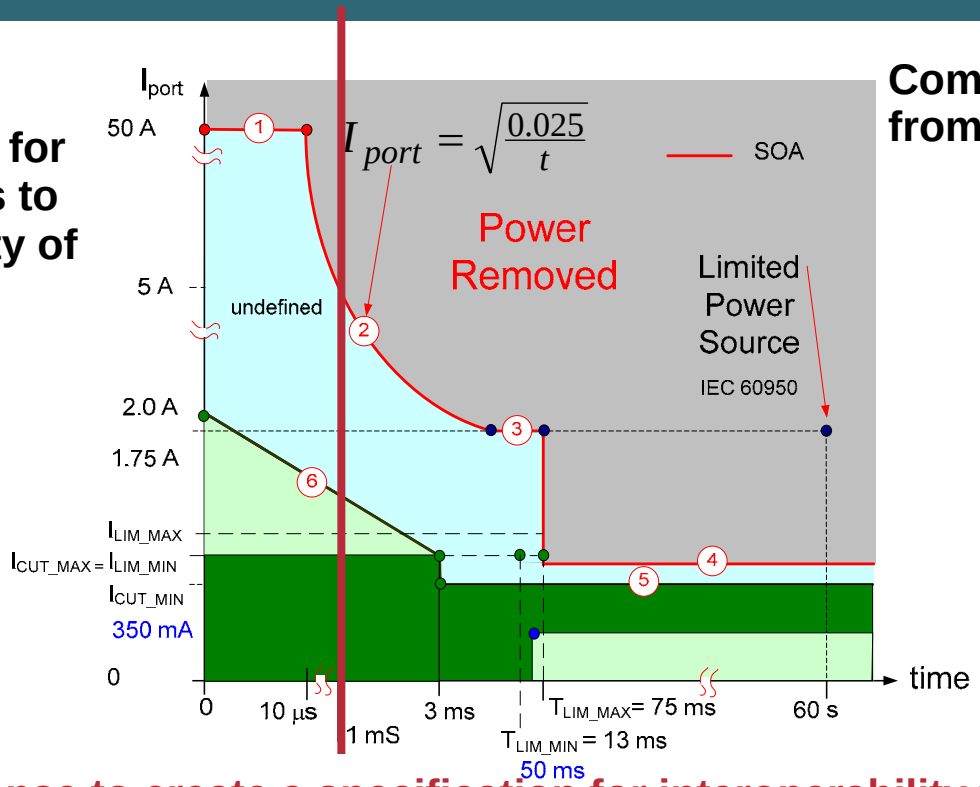
A type-1 PD may have it power removed above 350 mA.

This shows a proposed type-2 PSE AT/legacy curve.

Poll Type 2 PSEs may optionally power Type 1 PDs with Type 2 current limits
Y: 20 N: 0 A: 2

Creating the PSE SOA

t < 1 ms
PSE designers test for short-circuit events to ensure the reliability of their design.



Compliance shall be tested from t = 1 mS.

Does it make sense to create a specification for interoperability that is not tested? Is the follow text acceptable?

Have the IEEE specification:

Change the compliance time from 1 ms to 10 µs.

The current versus time curve is provided as a guideline below 10 µs and interoperable systems should support these guidelines.

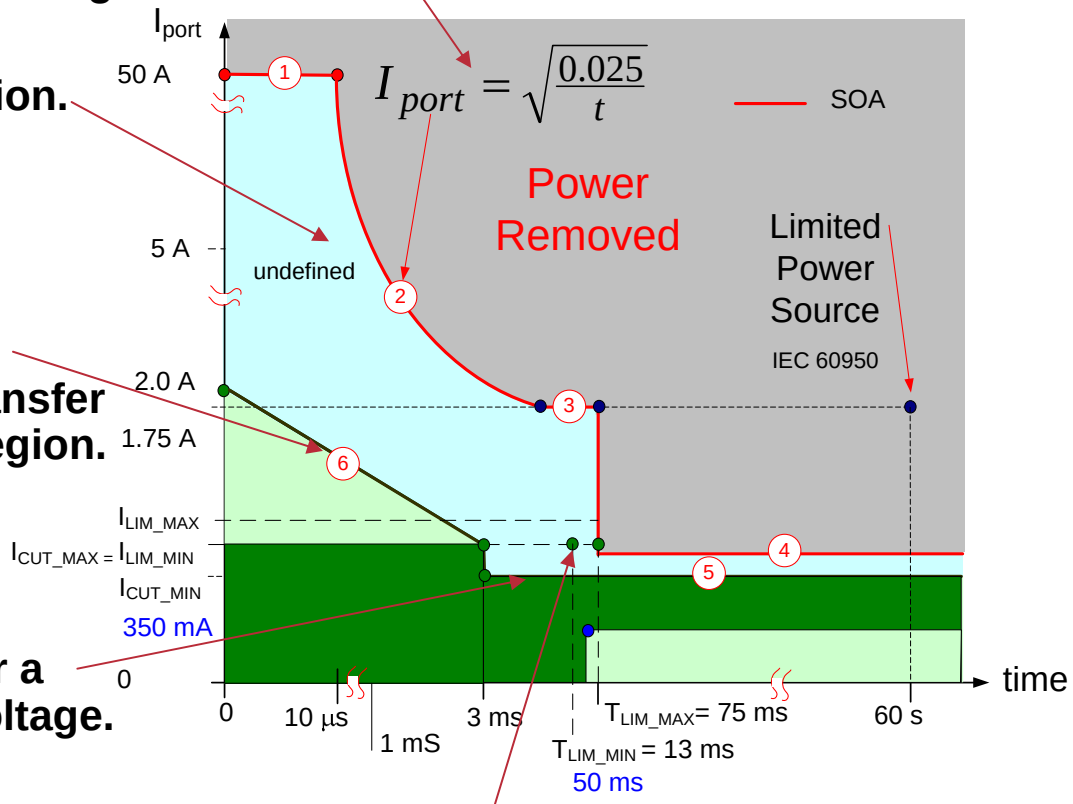
Understanding the Current Limit Curve

PSEs shall turn-off power before this region is entered.

PSEs can turn-off power in this region.

PDs may operate in this region.

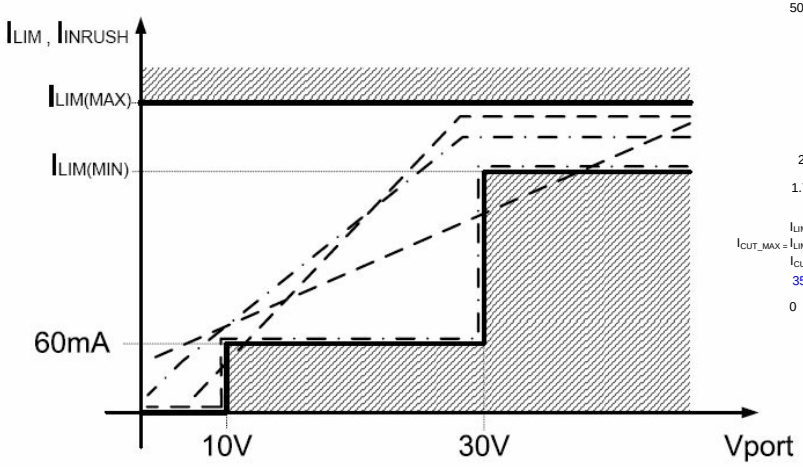
PSEs using energy based power transfer methods shall operate within this region.

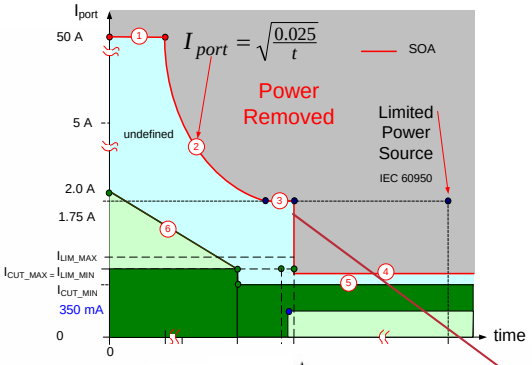


PDs shall operate below I_{CUT_MIN} over a 1 second period with a static PSE voltage.

PSEs using current limiting shall supply a constant current of at least I_{LIM_MIN} for at least T_{LIM_LIM}. $T_{LIM\_MIN} = f(I_{LIM\_MIN}, I_{CABLE})$)

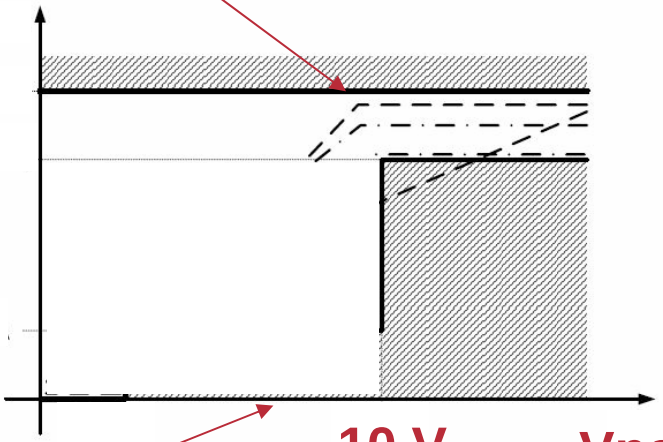
PSE SOA





Upper limit changes and is defined by the SOA

In-rush & Power-on as defined in IEEE 802.3



Power-on IEEE 802.3at

A maximum change of 7V for a duration of > 250 μs is possible for an interoperable system.

Change the focus from V_{PSE} to the voltage drop across the PSE pass element.

Poll

A load that results in greater than 10V across a compliant PSE pass element may have power removed.

Yea: 9

Nay: 0

Abstain: 0

Motion

Move that IEEE P802.3at adopt the SOA "shall remove power" proposal outlined in schindler_1_0719.pdf page 9.

P: Fred Schindler S: Yair Darshan

All present; Y: 29 N: 0 A: 3

802.3; Y: 21 N: 0 A: 1 => PASS

Move that Type 2 PSEs may optionally power Type 1 PDs with Type 2 current limits.

P: Fred Schindler S: Yair Darshan

All present; Y: 24 N: 0 A: 3

802.3; Y: 18 N: 0 A: 2 => PASS

Motion

Move that a PSE in the power on state may remove MDI power when the MDI voltage is out of specification.

P: Fred Schindler S: Yair Darshan

All present; Y: 30 N: 0 A: 4

802.3; Y: 19 N: 0 A: 0 => PASS

Next Step

- **???**

Based on V15 Spreadsheet.

Collected Worst-case Current Limits

Load drop: 47/48 ports, short channel 5 μF, 29.5 W PD.

PSE voltage ramp: short channel 180 μF, 29.5 W PD.

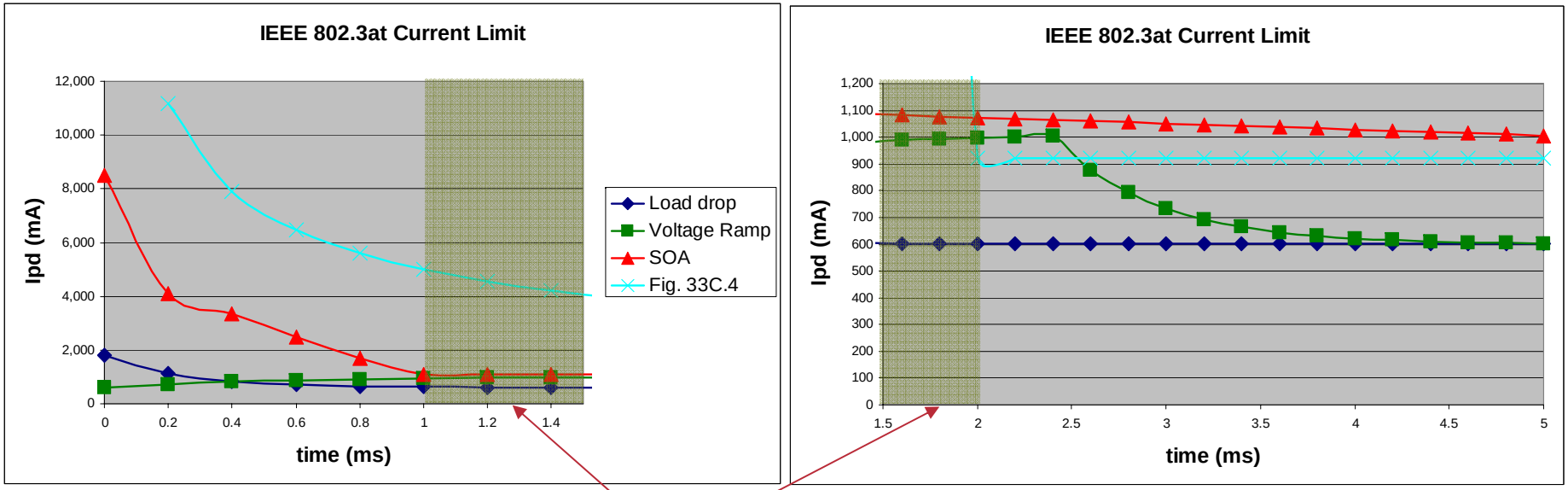
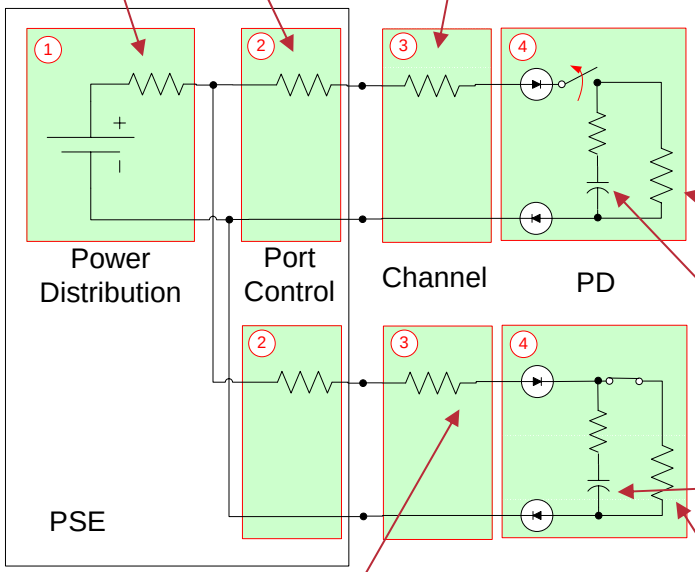


Fig. 33C.4 undefined, 1 ms < t < 2 ms

48 ports, $R_{distribution}$ = 80 mΩ, Rport = 0.9 Ω, $R_{channel}$ = 0.8 Ω (short),
C_{PD_ON} = 5 μF (no ESR), SOA for 805 size resistor 1 Ω in parallel with 1 Ω,
1 A fuse (1.98 A^2s), Generic NCH MOSFET, V_{DS} = 10 V @ I_D = 14 A

Use Case: PSE load drop



60 – 80 mΩ

0.9 – 3.2Ω / n

0.8 – 12.5Ω / n

1. All PDs draw maximum power.
2. All but one PD reduces power demand to zero.
3. The PSE distribution voltage ramps up.
4. The remaining on PD has current injected into it.

$\frac{(49.3)^2\ \Omega}{29.5n}$

This is a don't care when the load is dropped.

(5 – 180 μF)

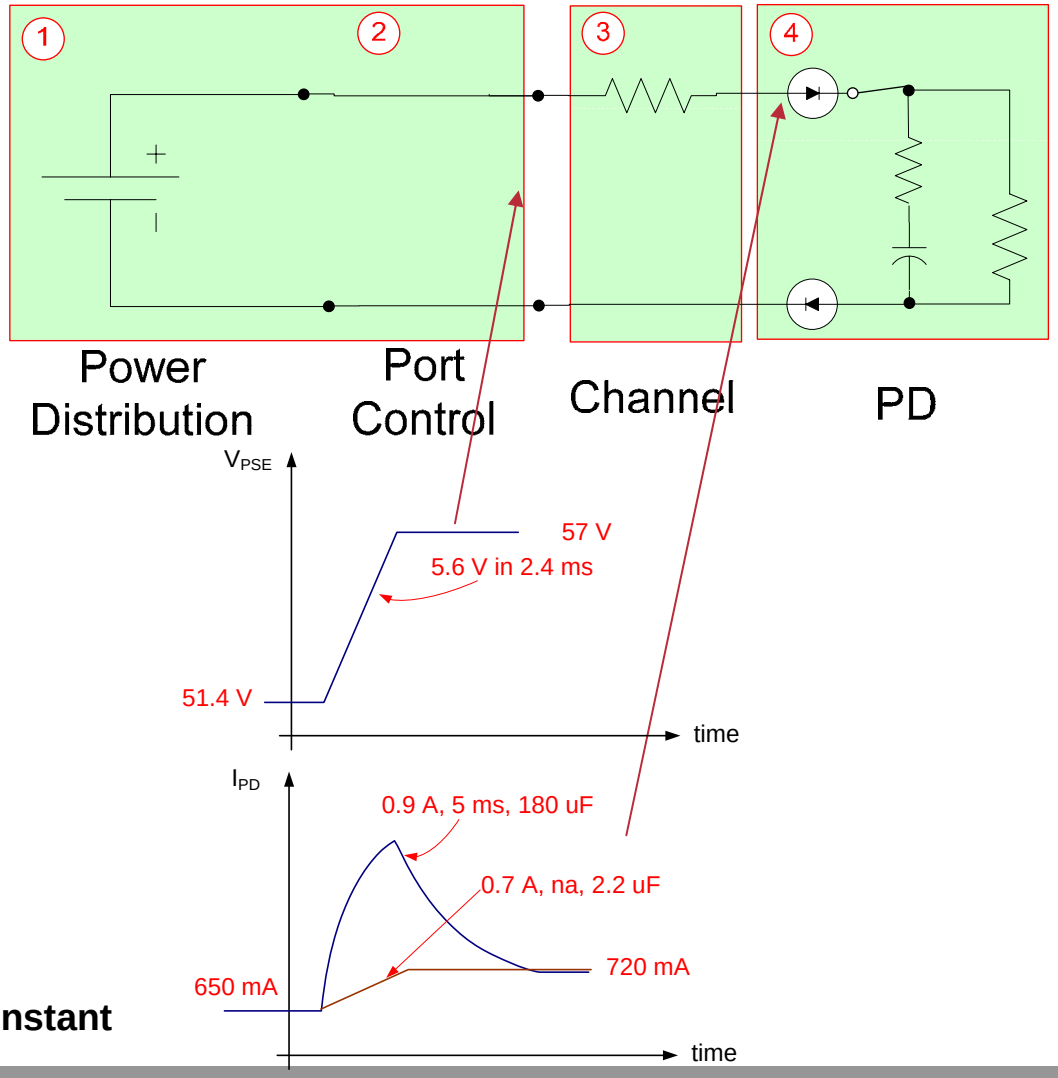
0.8 – 12.5Ω

$\frac{(49.3)^2\ \Omega}{29.5}$

Worst-case: 5 μF (no ESR), load dropped.

A PSE providing 50 V at 600 mA with PDs consuming 29.5 W.

Use Case: PSE power supply backup



Current, time constant

Worst-case: 180 µF.

Simplified System in Current Limit

Short channel
Rch = 0, Constant I_{PD}
IEEE 802.3 T_{LIM} = 47 ms
IEEE 802.3at, T_{LIM} = 12.6 ms

Long channel
Rch = 20 or 12.5 Ω, Constant I_{PD}
IEEE 802.3 T_{LIM} = 43 ms
IEEE 802.3at, T_{LIM} = 10.4 ms

IEEE 802.3

$$T_{LIM} > C_{PD}\frac{dv}{I_C}$$

$$T_{LIM} > 180\mu F\,\frac{57-44}{400-350}$$

$$T_{LIM} > 47ms$$

IEEE 802.3at

$$T_{LIM} > 180\mu F\,\frac{57-50}{820-720}$$

$$T_{LIM} > 12.6ms$$

IEEE 802.3, Table 33-12 item 3, Iport_peak = 400 mA.

$$dv_{MIN} > R_{ch}I_{LIM}$$

$$dv_{MIN} > 20\Omega \times 400mA$$

$$dv_{MIN} > 8V$$

$$V_{PSE} = 57V, V_{PD} = 57 - 350mA \times 20\Omega V = 49$$

$$T_{LIM} > 180\mu F\,\frac{49-44-8}{400-350}$$

$$T_{LIM} > 43ms$$

$$dv_{MIN} > 12.5\Omega \times 820mA$$

$$dv_{MIN} > 10.3V$$

$$V_{PSE} = 50V, V_{PD} = 41V\,@\,720mA$$

$$V_{PSE} = 57V, V_{PD} = 48V\,@\,720mA$$

$$T_{LIM} > 180\mu F\,\frac{57-41-10.3}{820-720}$$

$$T_{LIM} > 10.4ms$$

93% of ad hoc okay this model (13/14).