IEEE802.3at Task Force

Vport ad hoc

PD input current vs PSE negative voltage transient Technical Analysis

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Yair Darshan
Microsemi Corporation

Objectives

- To analyze the PD input current behavior under system dynamic source and load changes.
- Suggest values to TBD parameters in DraftD/0.9

PSE Voltage Transient Below Vport

- Table 33-5 item 2a
  - 7.6% below Vport for 250usec max.
- Worst case:
  - Vport=50Vdc
  - Vport_tran_lo=50-50*0.076=46.2V
- PD voltage in this case

$$Vpd = \frac{Vpse + \sqrt{Vpse^2 - 4 \cdot Rcable \cdot Ppd}}{2} = \frac{46.2 + \sqrt{46.2^2 - 4 \cdot 12.5 \cdot 29.52}}{2} = 35.9V$$

  - PD minimum input voltage is 36V similar to 802.3af hence item 2a need to be changed to 7.5% to match all numbers.
- PD current in this case for up to 250usec.

$$Ipd = \frac{29.52W}{36V} = 0.82A$$

- PD must be allowed to consume 0.82A up to 250usec .

PSE Voltage Transient Below Vport – Cont.

- It means that any PD current limit function threshold must be above 820mA for at least 250usec.
- The same is true for PSE current limit function.

Conclusions

Add to Table 33-12 item 1 a separate line V_tran_lo as per table 33-5 item 2b for Type 2 PD: Minimum operating PD voltage 36V for time duration defined in **33.2.8.2b.**

Discussion

- Please add corner case to the minutes and it will be explained at the meeting tomorrow (Sep 12,2007) (Today).

Motion

- Move that the IEEE 802.3at Task Force adopt presentation darshan_2_0907.pdf slide 5 to be incorporated in the next P802.3at draft.
- M: Y. Darshan S: F. Schindler
- Technical 75%
- Y: 21, N: 0