# Current Limit Versus Energy Limit Based PSE

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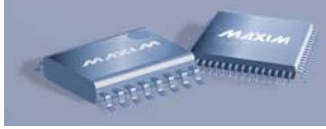
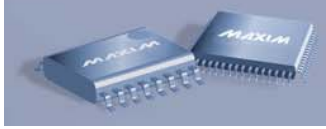
Maxim Integrated Products



# Review of PoE+ System Consideration

- **PoE+ System Requirements:**
  - System Inter-Operability
  - Allow Safe Maximum Possible Power Delivered from PSE to PD
  - Adhere to the Maximum Current Allowed *:
    - In the Cable
    - In the Connector
    - In the Patch Panel
    - In the LAN Magnetics
  - Backward Compatible w/ 802.3af Legacy Devices
  - Support 180uF capacitor on PD
  - Simplify Compliant Testing

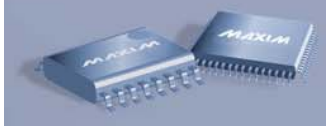
*Note: Maximum current value for cable, connector, and patch panel are determined by heating effect which causes by DC/RMS current. Low level transient current that lasted less than a few seconds does not cause significant heating and could be neglected



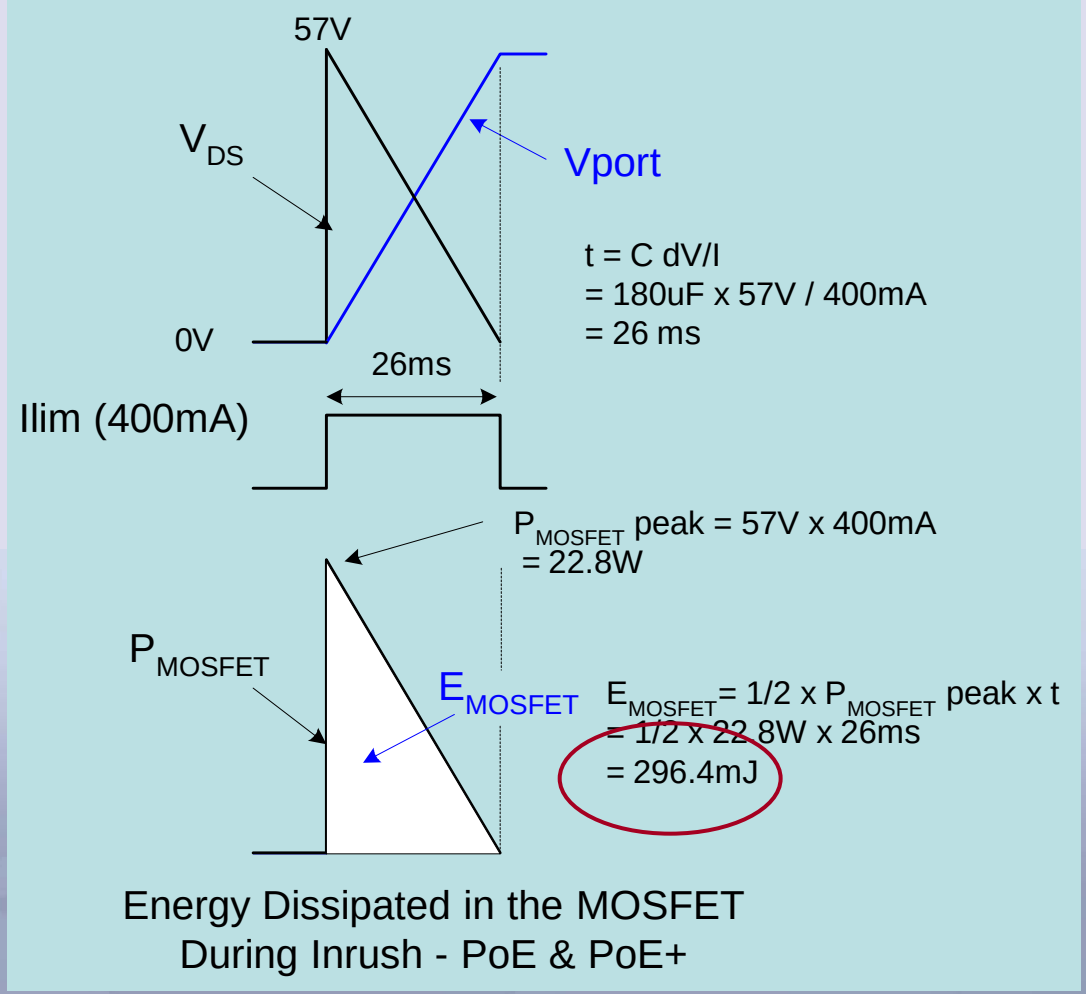
# Review of PoE+ System Consideration

- **PSE Requirements:**
  - PD Detection, L1 Classification, Optional L2 Classification
  - Handle Input Power Supply Voltage Transient
  - Protect Port Short Circuit Condition
  - Provide as Much Power as Possible to the PD, Limited only by the Cable Capability

- **PD Requirements:**
  - Provide Detection and Classification Signatures
  - Manage Input Ripple Current
  - Handle Load Step Transient
  - Utilize as Much Power as Possible from the PSE When the Application Requires

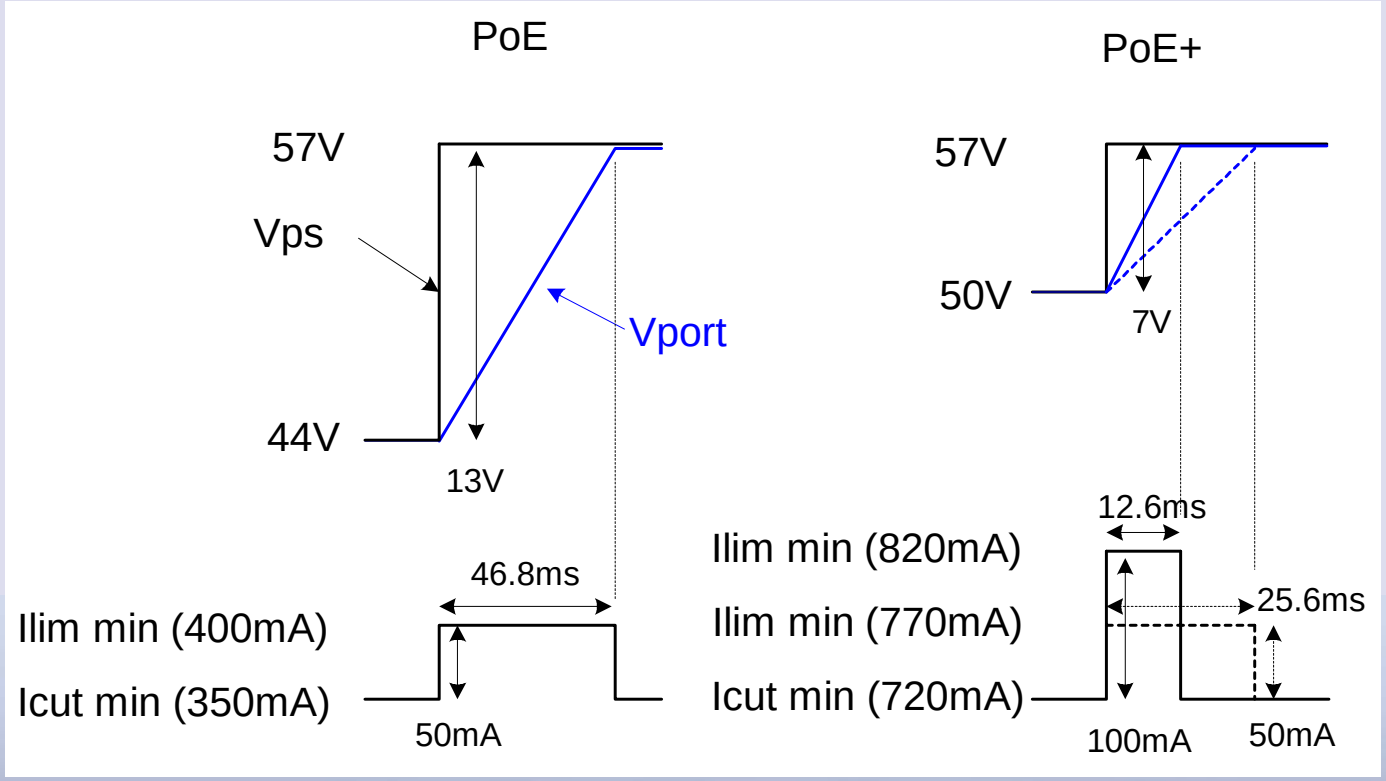


# MOSFET Power Dissipation – During Inrush Period for Both PoE and PoE PSEs



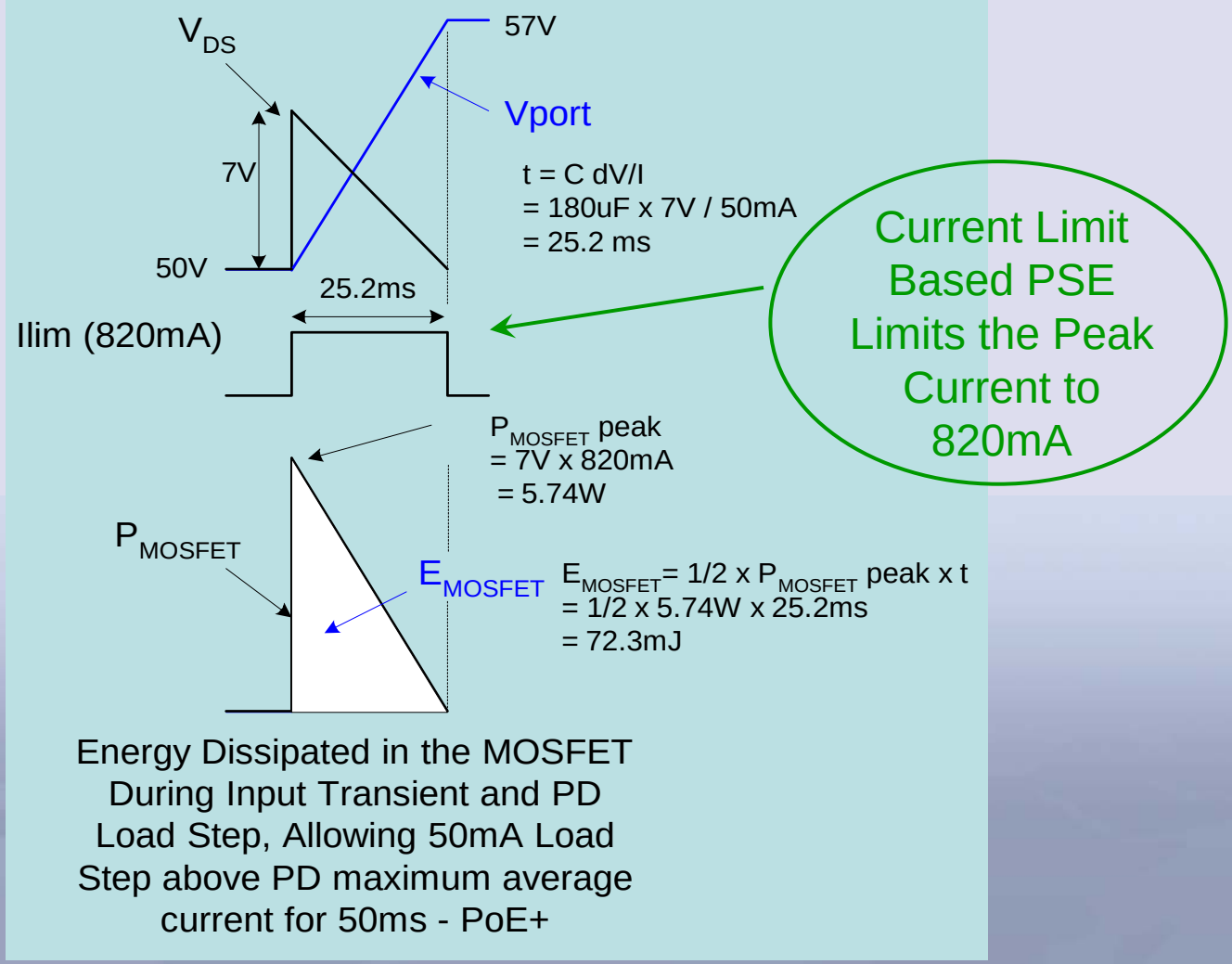

Energy Dissipated in the MOSFET
During Inrush - PoE & PoE+

# Current Limit Based - Input Voltage Transient:




**In PoE+ system, there is plenty of head room to handle input transient and PD load step at the same time**

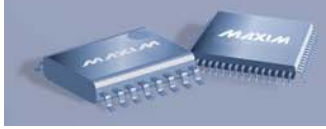
# Current Limit Based - MOSFET Power Dissipation – During Input Transient for PoE+ PSE



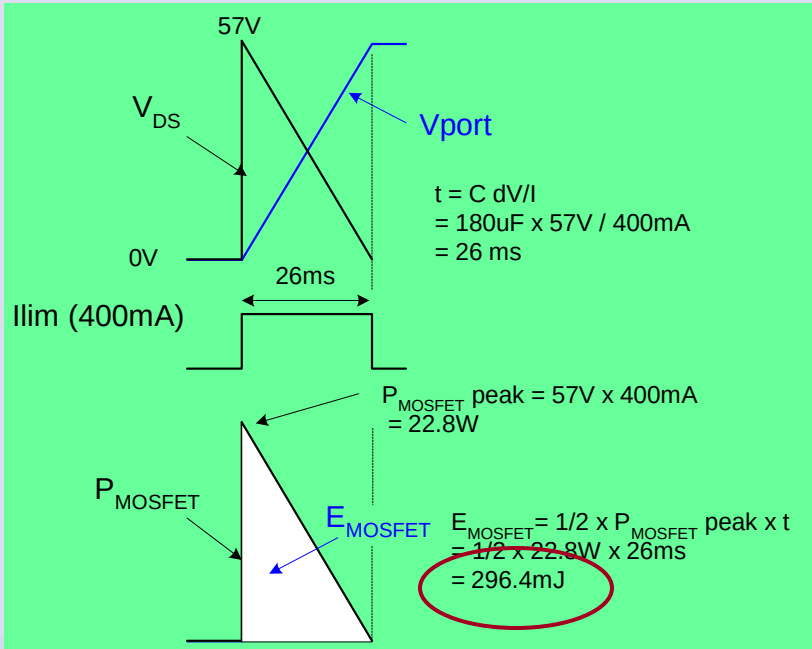

Energy Dissipated in the MOSFET During Input Transient and PD Load Step, Allowing 50mA Load Step above PD maximum average current for 50ms - PoE+

# Current Limit Based – Output Short Circuit

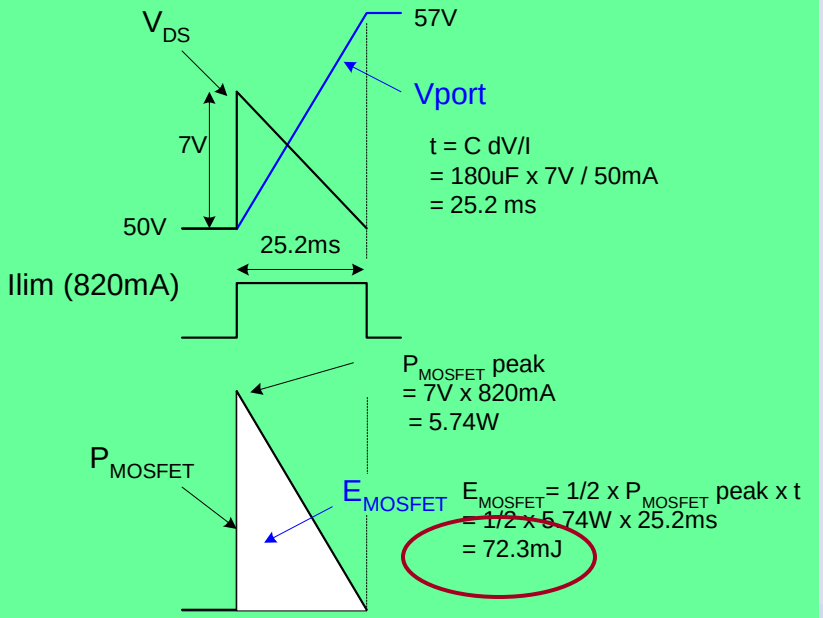
**Current Limit Based PSE Limits the Peak Current to 820mA**



# MOSFET Power Dissipation Calculation




Energy Dissipated in the MOSFET During Inrush - PoE & PoE+



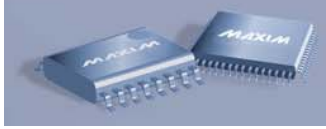

Energy Dissipated in the MOSFET During Input Transient and PD Load Step, Allowing 50mA Load Step above PD maximum average current for 50ms - PoE+

**→ MOSFET Power Dissipation Dominates During Inrush Period**

# Truth or Myth?

**Current Limit Based Causes Higher Power Dissipation in the Power MOSFET in PoE+ System? → Myth**

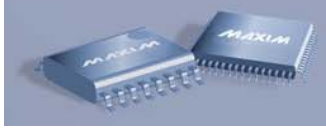
- **The Truth is:**
  - **Power Dissipation in the MOSFET is Largest During the Inrush Period. This Power Dissipation is the same for PoE and PoE+ Systems, Whether Current Limit or Energy Limit Based is used.**
  - **This Large Power Dissipation During Inrush is What Has Been Impeding the Integration of the Power MOSFET in the PSE Controller.**



# Energy Limit Based - Input Voltage Transient

- **Short Cable:**
  - Rcable = 1.0Ω (estimated: includes all PSE power path impedances)
  - Input Voltage Transient from 50V to 57V
  - dV/dt maximum = 3.5V/us
  - PD capacitance = 180uF
  - Peak Current Due to dV/dt = 180uF x 3.5V/us = 630A! → Peak Current is Limited Only by Rcable = (57V – 50V)/1.0Ω = 7A

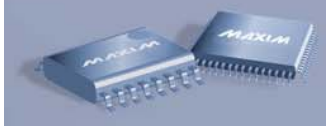
Energy Limit Based PSE Does Not Limit the Peak Current!



# Energy Limit Based - Output Short Circuit

- **Short Cable:**
  - **Rcable = 1.0Ω (estimated: includes all PSE power path impedances)**
  - **Input Voltage = 57V Maximum**
  - **→Peak Current is Limited Only by Rcable = 57V/1.0Ω = 57A**

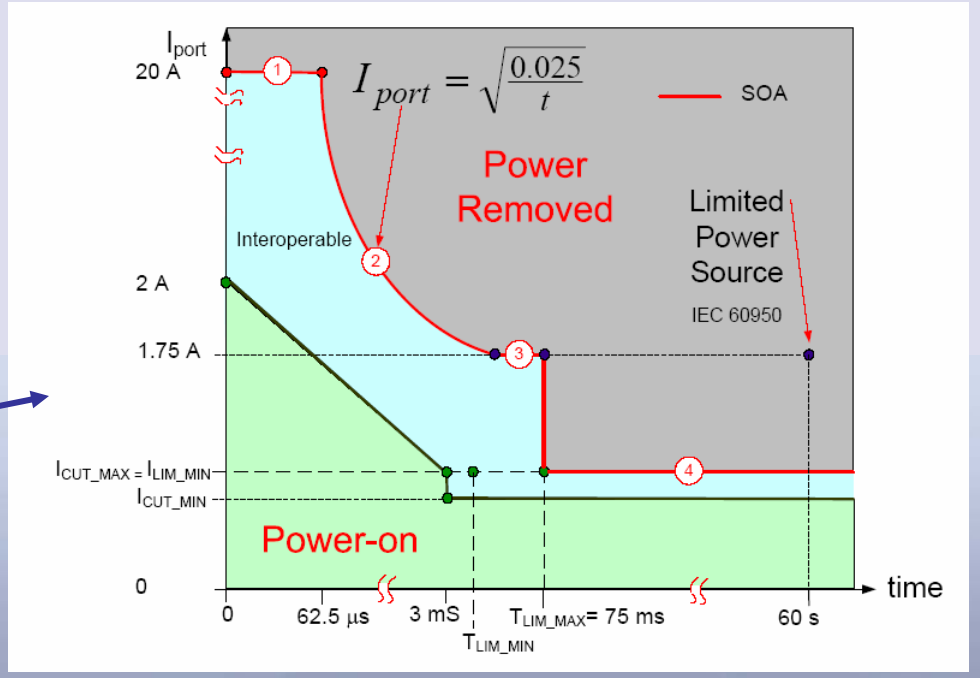
Energy Limit Based PSE Does Not Limit the Peak Current!



# Energy Based PSE - Testability

- **Energy Based PSE Dictates Complex Model for Testing**

Graph is from the Vport Ad-Hoc presentation

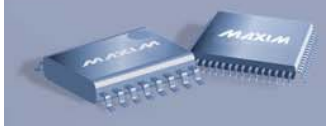


# Current Limit vs Energy Limit for PoE+ PSE

| | Current Limit | Energy Limit | Advantages/Problem |
|---|---|---|---|
| MOSFET Power Dissipation During Inrush | 246.4mJ | 246.4mJ | Same |
| Peak Current During Input Transient short cable | 820mA (920mA Maximum) | 7A | Current is guaranteed to be limited<br>High current peak can saturate and possibly damage the LAN Magnetics |
| Peak Current During Output Short Circuit | 820mA (920mA Maximum) | 57A | Current is guaranteed to be limited<br>High current peak can saturate the LAN Magnetics, possibly damage it and other such as connector and patch panel |
| Testability | Simple and same as 802.3af | Complex Curve | Energy Limit Based PSE Added testing complexity and cost |

## Conclusion: Energy Limit Based For PoE+ System

- **Energy Limit Based PSE Does Not Limit Peak Current During Input Transient → Possible LAN Magnetics Core Saturation and Data Corruption?**
- **Energy Limit Based PSE Does Not Limit Peak Current During Output Short Circuit → Possible Damage to Connector, Patch Panel, LAN Magnetics?**
- **Energy Limit Based PSE Creates Challenges For Compliant Testing**



## Conclusion: Current Limit Based For PoE+ System

- Current Limit Based PSE Can Easily Handle Simultaneous Input Voltage Transient and PD's Load Step
- Current Limit Based Assures PSE Port Current ≤ 926mA Maximum for ≤ 75ms During Input Transient
- Current Limit Based PSE Assures Port Current ≤ 926mA Maximum for ≤ 75ms During Output Short Circuit
- Current Limit Based PSE Eases Compliant Testing
- → Current Limit Based is the Recommended Technique to Limit the PSE Port Current in PoE+ System