Overload Behavior for Type-2 PD

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IEEE 802.3at Task Force

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Anoop Vetteth

Fred Schindler

Cisco

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Defining the PD Behavior

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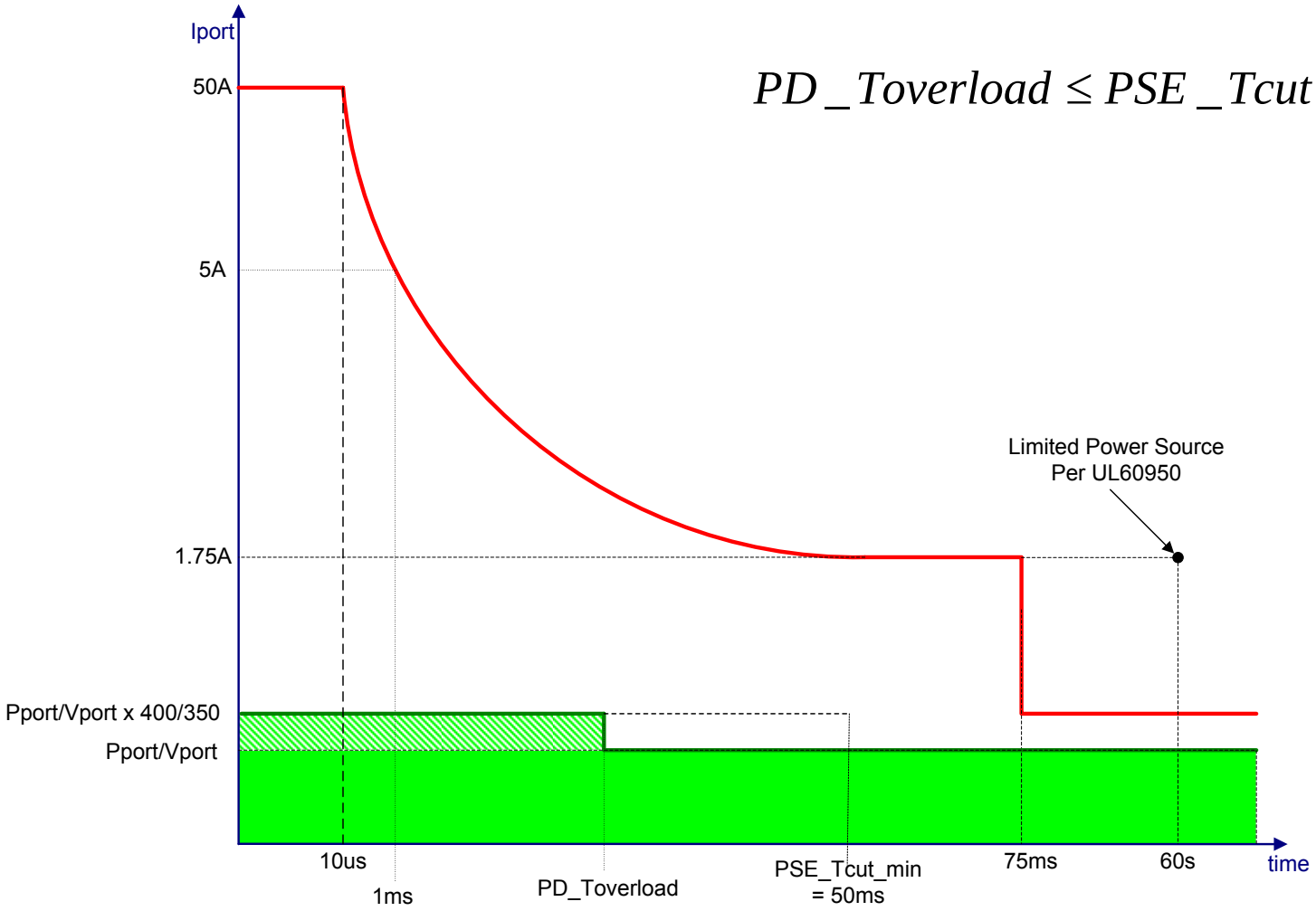
- **The PD behavior is defined independent of the PSE behavior.**
- **MDI behavior is defined.**
- **Current limiting is not mandated at the PD.**

PD Mask 1 (Static MDI Voltage)

$$PD\_Toverload \leq PSE\_Tcut\_\min$$



Worst case MDI behavior

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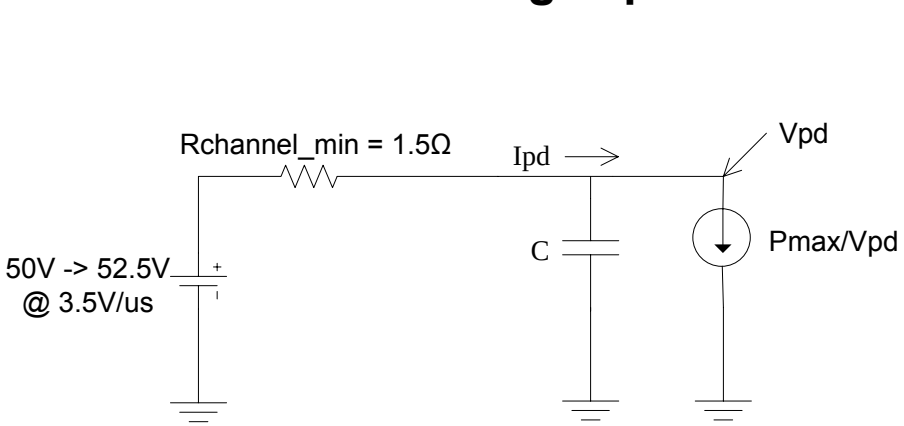
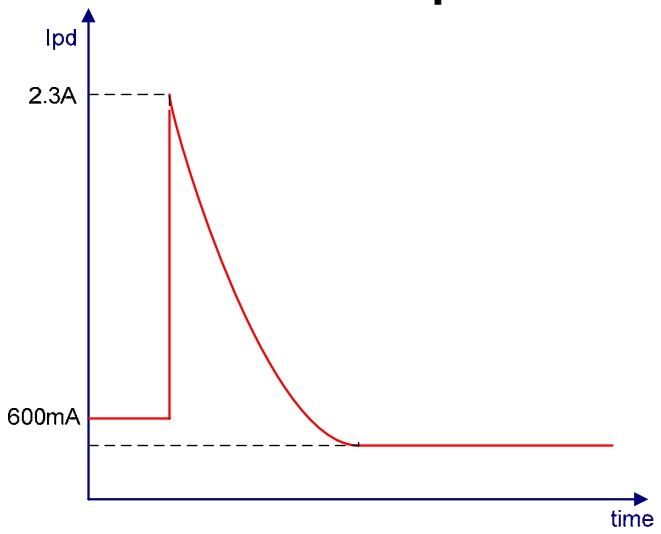
- The maximum permissible MDI dv/dt of 3.5V/µs is to guarantee data integrity.
- Worst case MDI transitions agreed upon by Ad-Hoc group are*:
  - Simultaneous load drop on multiple ports (instantaneous)
  - Power-supply failover (5.6V/2.4ms = 2250V/s)
- Simultaneous load drop on multiple ports has the fastest dv/dt rate.
- Power supply failover case takes more time to charge up the PD capacitor

*Refer to schindler_1_0307.pdf pages 4-6 (March 2007 Plenary).

Modeling worst case MDI dv/dt

Maximum MDI voltage spike for the simultaneous load drop case = 2.4V



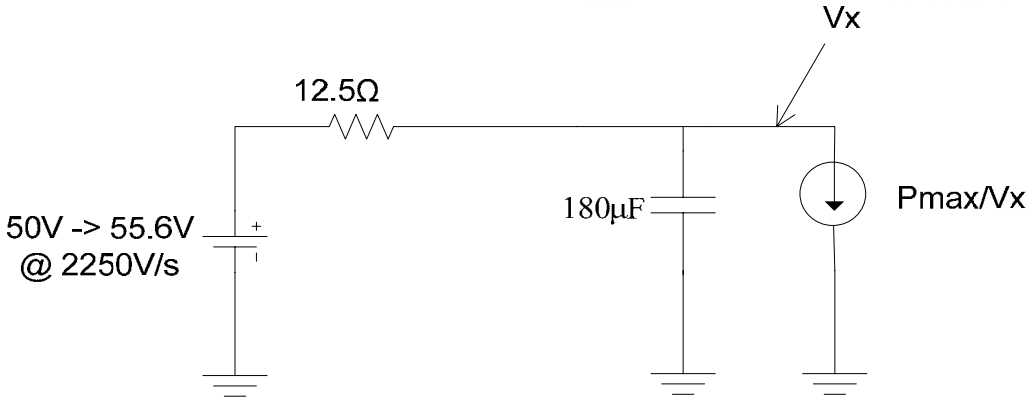


- **The above model assumes a minimum channel resistance of 1.5Ω between PSE power supply and PD MDI. This includes the following:**

  PSE transformer, PSE FET and Sense Resistor, Cable resistance, Power supply output resistance, PSE fuse.

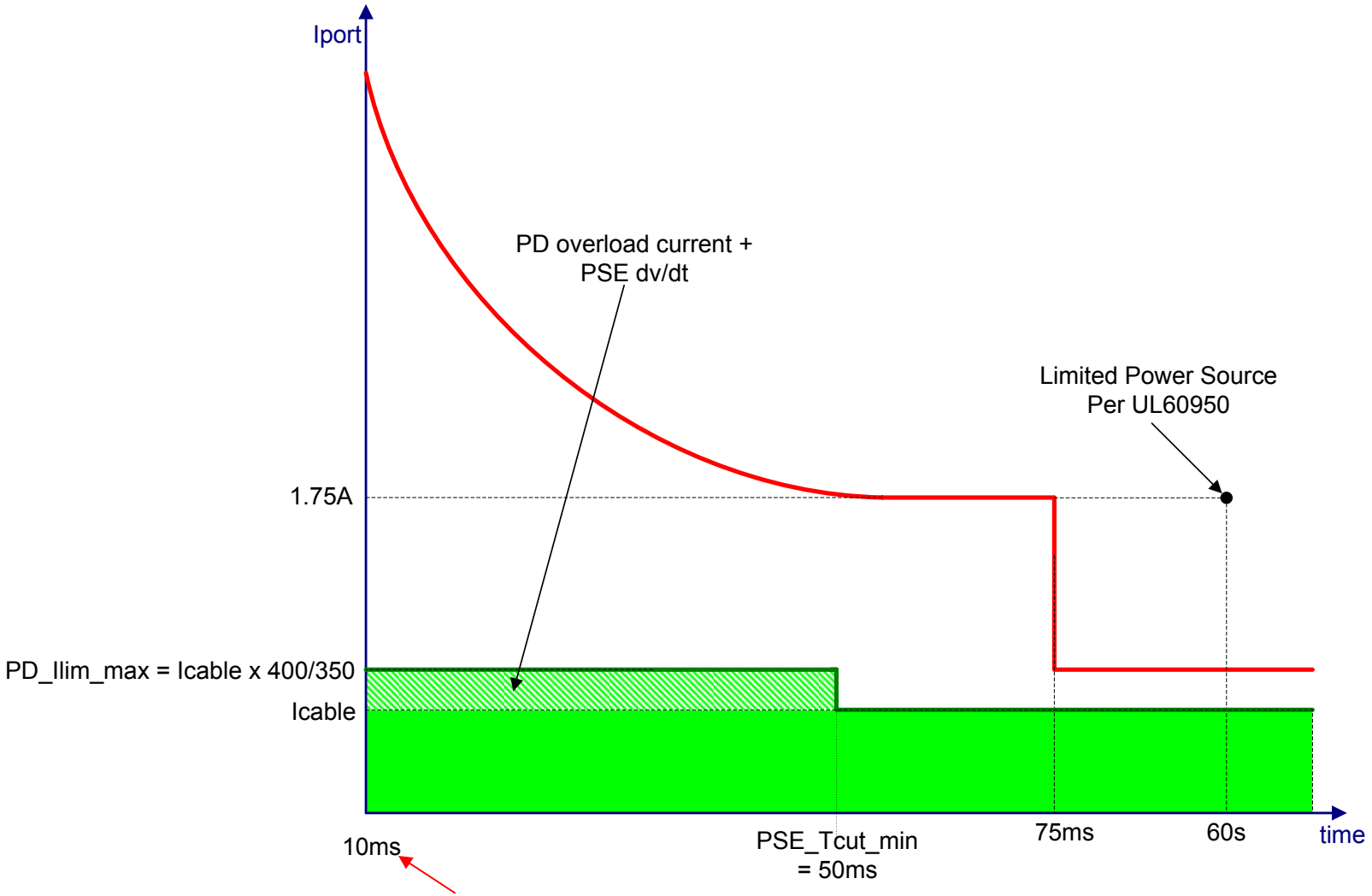
- **PD transformers and PD rectifier diodes have not been taken into account.**
- **The PD input capacitor can be any value.**

Time required to charge PD input capacitor



- **The PD in this example is a constant power PD that continuously draws the maximum power without going into overload (Eg. 720mA at 50V).**
- **There is no current limiting at the PD. The PD input capacitor is 180uF.**
- **The MDI voltage changes from 50V to 55.6V in 2.4ms. Assume that the PSE limits the current at 820mA (15% above Icable).**
- **The PD draws the surge current for a duration of 7ms. After this time the charging current is below 820mA.**
- **Note that 180uF is an extreme value and most PDs will have an input capacitance significantly lower than this value.**

PD Mask 2 (Dynamic MDI voltage)



Note

Refer to slide 13 for PD behavior prior to 10ms.

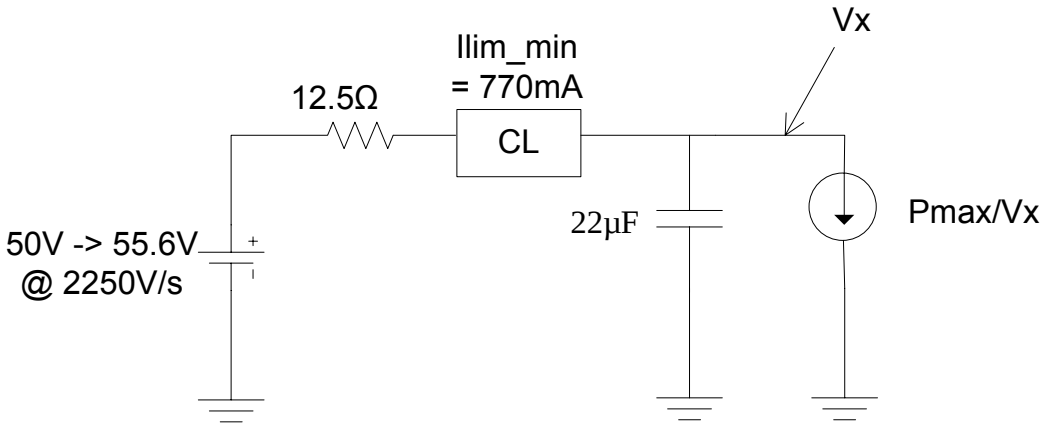
PD Mask 2 …….Continued

- The PSE is responsible for limiting the current for up to 10ms. The PSE may turn off the PD if the current is above PD_Ilim_Max after 10ms.
- The PSE can limit the current at any value between PD_Ilim_Max and SOA curve.
- PSE dv/dt is a fault condition that is expected to be infrequent. Hence saturation of magnetics during this event can be neglected.
- PD Mask 2 is valid for overload conditions after startup.

Current Limiting at the PD

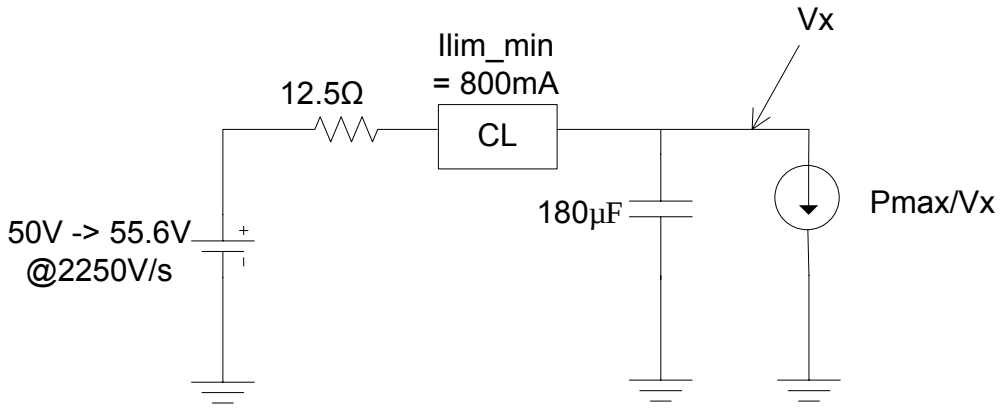
- The following PD designs may require current limiting to restrict themselves within PD Mask 2.
  - Input Capacitance > 180uF
  - Require overload current (current greater than Icable)
- These PDs are niche applications and should not result in any cost increment to the PSE.
- All known PDs already have current limiting.
- External sense resistance or better process technology can be used to obtain tighter tolerance for the current limiting value at the PD.

Sample PD with overload current and 22uF PD input Cap



- **The PD in this example is a constant power PD that draws an overload current. PD input capacitor is 22uF**
- **Assume that the Ilim range for the PD is 770mA-820mA.**
- **Time taken to charge the 22uF input capacitor = 2ms.**
- **If PSE_Tcut_Min = 50ms then PD_Toverload = 48ms**
- **Lower PD input capacitance permits a longer PD_Toverload**

Sample PD with overload current and 180uF PD input Cap

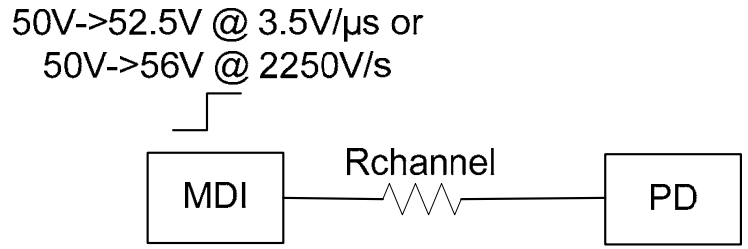


- **The PD in this example is a constant power PD that draws an overload current.**
- **Assume that the Ilim range for the PD is 800mA-820mA (Tighter tolerance).**
- **Time taken to charge the 180uF input capacitor = 9ms.**
- **If PSE_Tcut_Min = 50ms then PD_Toverload = 41ms**
- **A tighter tolerance on PD current limit permits a longer PD_Toverload**

PD Constraints

- **Current limiting is not always mandated at the PD. MDI behavior is defined.**
- **PD designer ensures that PD is compliant under static MDI voltage for the advertised power level.**
- **PD designer ensures that PD is compliant under dynamic MDI voltage. There are two test cases:**
  - **MDI voltage rises from 50V to 52.5V at 3.5V/us**
  - **MDI voltage rises from 50V to 56V at 2250V/s**

PD Compliance Model



Test Case 1

The PD MDI is connected to a voltage source that drives the voltage from 50V to 52.5V at a 3.5V/µs slew rate. Rchannel = 1.5Ω and the MDI voltage source supports a current greater than 2.5A. The current spike should not exceed 2.5A and should settle below PD_Ilim_Max within 4ms.

Test Case 2

The PD MDI is connected to a voltage source that drives the voltage from 50V to 56V at a 2250V/s slew rate. Rchannel = 12.5Ω and the MDI voltage source limits the current at MDI_Ilim. The PD should operate within PD Mask 2 under worst case current draw.

$$PD\_Ilim\_Max < MDI\_Ilim \leq (PD\_Ilim\_Max + 5mA)$$

Advantages

- Flexible PSE architecture
- Flexible PD architecture with realizable tolerance on PD_Ilim value when current limiting is used at the PD
- Compliance can be tested at the MDI
- This proposal requires the PD to meet specific current limits but does not require a PD to provide a current limiter

Motion

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Move that IEEE P802.3at adopt pages 3, 7, 8, 12 and 13 in vetteth_2_0907.pdf as a baseline for the next draft.

M: Fred Schindler S: Matthew Landry

All present; Y: 25 N: 0 A: 2

802.3; Not Voted