Vport ad hoc
D1.0 Vport related comment resolution

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3 ad hocs with an average attendance of 16 people since the last IEEE meeting.

Agenda

- **Principles based comment resolution**
- **Comment Clusters**
- **Recommendations for the Vport-comment bucket.**

Principles to use

- **Develop some principles to use to guide the ad hoc during comment resolution.**
  - **Use concise text**
  - **Focus on what operation you want done**
  - **Cover only compliance (i.e., avoid discussing noncompliance devices)**
  - **Do not repeat requirements**
  - **Change as little as possible when improving text**
  - **Try to refrain from repeat the same issue once it has been resolved.**
  - **Ensure that legacy devices are compliant.**

Consider simplify requirements into logic statements to help support the above principles.

Comment Clusters

- 2 **PSE current limit curve:** 81, 132
- 3 **Vport turn off and transient:** 246, 247, 135, 80
- 4 **Definitions:** 118, 34, 32, 260
- 16 **Matching PSE and PD currents:** 137, 114, 227, 79, 56, 249, 36, 105, 143, 33, 59, 165, 94, 90, 9, 95

Comments in red are related but are not part of this bucket.

Cluster: PSE current limit curve

- **3 PSE current limit curve: 81, 9, 132**

Comment 81

Cl **33** *SC* **2.8** *P* **40** *L* **35** # 81

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Iport_max is shown with the value Icable as a MINIMUM required maximum port current. However, Icable is defined as 720 mA in 33.1.4, and 720 mA is the very top of the allowed current range in Figure 33-9a (formerly SOA curve). So it doesn't seem logical that Icable can be a MINIMUM value for anything including Iport_max for Type 2 PSE's.

SuggestedRemedy

Icable needs to be clearly defined as EITHER the maximum continous current (Iport) that can ever exist on a single pair OR if it is to be equated with 803.3af value of Iport_max (MIN) (=350 mA), then it cannot be considered the maximum continous current allowed on a pair as implied by Figure 33-9a.

Min.

4	Maximum output current in normal powering mode at PSE min output voltage	I_{Port_max}	Adc	0.35		1
				I_{Cable}		2

This is suppose to be: 400/350Pport/Vport see fig. 33-12b

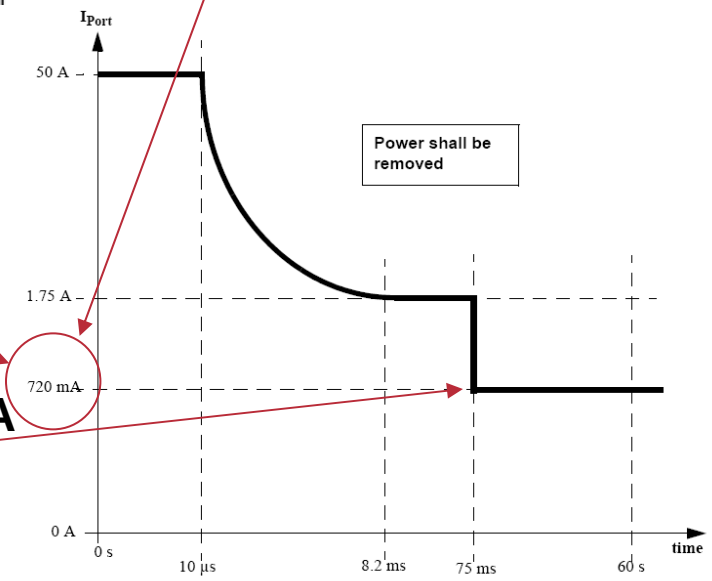


Figure 33–9a—PSE PI operating current template

This says Iport_max > Icable, Icable may = 720 mA
This says Iport <= 820 mA, for t > 75 ms

Both of these statements are true.

Comment 81 Resolution

- **Recommend**
  Correcting figure 33-9a, and generically using Icable for type 1 and 2 PSEs in table 33-5.

Comment 132

Cl **33** *SC* **2.8.2a** *P* **42** *L* **12** # 132

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The PD is restricted to a current slew rate of 15 mA/us maximum. A single PSE port can provide a 35 mA/us demand rate but multiple ports transitioning at this rate may be unrealistic.

SuggestedRemedy

Change PSE requirements in this section of "35 mA/us max." to "at least 15 mA/us."

Proposed Response *Response Status* **O**

33.2.8.2 Load regulation for Type 1 PSEs

The specification for load regulation in Table 33–5 shall be met ~~from~~ with a 0.44 W to ~~15.4 W~~ (I_{Port_max} min × V_{Port} min) load step at a rate of change of 35 mA/µs max. The voltage transients as a result of the load changes shall be limited to 3.5 V/µs max.

Proposed Resolution:

33.2.8.2 Load regulation for Type 1 PSEs — at least 15 mA/us

The specification for load regulation in Table 33–5 shall be met ~~from~~ with a 0.44 W to ~~15.4 W~~ (I_{Port_max} min × V_{Port} min) load step at a rate of change of ~~35 mA/µs max~~. The voltage transients as a result of the load changes shall be limited to 3.5 V/µs max.

of up to 35 mA/us

Cluster: Vport turn off and transient

- **3 Vport turn off and transient: 246, 247, 135, 80**

Comment 246

Cl **33** *SC* **2.8.1** *P* **41** *L* **52** # 246

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The statement:

"A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the VPort specification"

is very broad and doesn't reflect the intent. Add text to clarify.

SuggestedRemedy

IS:
A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the VPort specification.

SHOULD BE: (CAPS INDICATE ADDITION)
A PSE in the POWER_ON state may remove power from the PI IF THE PI voltage no longer meets the VPort specification DUE TO EXCESSIVE PORT LOADING FROM A NON-COMPLIANT PD OR PORT FAULT CONDITION.

This describes what to do for a noncompliant device.

A PSE meeting all the requirements of this standard except Vport is not attached to a PD and may remove the port power. This may be resolved by 135. This same statement was covered during the Richfield Vport ad hoc comment resolution.

This is related to comments 247, 135, and 80.

Simplified view of the problem

Requirement A: Provide Vport for all valid PD loads.

- **Nuance i: Iport <= Pport/Vport, (average PD demand)**
- **Nuance ii: Iport <= Ipeak, for TLIM, 5% duty (peak PD demand)**
- **Nuance iii: Remove power before exceeding SOA**

Passing the PICS ensures equipment is compliant.

Allowance B: You may remove power if Vport is out of spec.

Allowance B, lets you implement A-iii based on your design requirements.

Power Valid = I & II

Power removed = III

Comment 246

Cl **33** *SC* **2.8.1** *P* **41** *L* **52** # 246

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The statement:

"A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the VPort specification"

III

is very broad and doesn't reflect the intent. Add text to clarify.

SuggestedRemedy

IS:
A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the VPort specification.

SHOULD BE: (CAPS INDICATE ADDITION)
A PSE in the POWER_ON state may remove power from the PI IF THE PI voltage no longer meets the VPort specification DUE TO EXCESSIVE PORT LOADING FROM A NON-COMPLIANT PD OR PORT FAULT CONDITION.

Power removed = III & !(I + II)

Note that III is only true if (I + II) is not. Therefore, adding !(I + II) is redundant.

This is related to comments 247, 135, and 80.

Comment 247 see 135

Cl **33** *SC* **2.8.2B** *P* **42** *L* **17** # 247

Stanford, Clay Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Paragraph could be written more clearly to better express intent.

SuggestedRemedy

IS:
A Type 2 PSE shall maintain an output voltage no less than VTran_lo below VPort min for transient conditions lasting more than 30us and less than 250us.

Transients less than 30us in duration may cause the voltage at the PI to fall more than VTran_lo . The minimum PD input capacitance ensures the PD will operate for any input voltage transient lasting less than 30us. Transients lasting more than 250us shall meet the static VPort specification.

The existing text is more concise. This may be resolved by 135.

SHOULD BE:

Brief decaying voltage transients less than 30us in duration should not effect PD operation due to storage capacity present in the PD and as such are not limited.

For decaying voltage transients lasting 30 to 250us, a Type 2 PSE shall maintain an output voltage no less that VTran_low bleow Vport_min.

Transients lasting more than 250us shall meet the static VPort specification.

This explains why 30us is ok and adds a new term "decaying voltage transient."

This repeats what was said in the existing text using "decaying voltage transient."

This repeats what should be done when a transient is not present.

Simplified view of the problem

Requirement A: Provide Vport for all valid PD loads.

- **Nuance i: Iport <= Pport/Vport, (average PD demand)**
- **Nuance ii: Iport <= Ipeak, for TLIM, 5% duty (peak PD demand)**
- **Nuance iii: Remove power before exceeding SOA**

Requirement X: A transient is specified for durations from 30 to 250us.

Passing the PICS ensures equipment is compliant.

Allowance X, lets you provide a system that interoperates with expected system transients.

Power Valid = I & II & X

Comment 247 see 135

Cl **33** *SC* **2.8.2B** *P* **42** *L* **17** # 247

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Paragraph could be written more clearly to better express intent.

SuggestedRemedy

IS:
A Type 2 PSE shall maintain an output voltage no less than VTran_lo below VPort min for transient conditions lasting more than 30us and less than 250us.

Transients less than 30us in duration may cause the voltage at the PI to fall more than VTran_lo . The minimum PD input capacitance ensures the PD will operate for any input voltage transient lasting less than 30us. Transients lasting more than 250us shall meet the static VPort specification.

SHOULD BE:

Brief decaying voltage transients less than 30us in duration should not effect PD operation due to storage capacity present in the PD and as such are not limited.

X For decaying voltage transients lasting 30 to 250us, a Type 2 PSE shall maintain an output voltage no less that VTran_low bleow Vport_min.

Transients lasting more than 250us shall meet the static VPort specification.

This explains why 30us is ok and adds a new term "decaying voltage transient."

This repeats what was said in the existing text using "decaying voltage transient."

This repeats what should be done when a transient is not present.

Here X' = X & (I & II)

with this,

Power Valid = I & II & X' = I & II & (X & (I & II)) = I & II & X

Comment 135

Cl **33** *SC* **2.8.2a** *P* **42** *L* **17** # 135

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *editorial*

The sentence structure does not convey the intent for PSE transient behavior and what action to take when a short circuit condition exists.

SuggestedRemedy

Modify the existing sentence to: "A Type 2 PSE shall maintain an output voltage of no less than VTran_lo below Vport min for transient conditions lasting more than 30 uS and less than 250 us, and meet the requirements of section 33.2.8.8.

Changes

A Type 2 PSE shall maintain an output voltage no less than V_{Tran_lo} ~~%~~ below V_{Port} min for transient conditions lasting more than 30 µs and less than 250 µs.

Transients less than 30 µs in duration may cause the voltage at the PI to fall more than V_{Tran_lo} ~~%~~. The minimum PD input capacitance ensures the PD will operate for any input voltage transient lasting less than 30 µs ~~exceed this rating~~. Transients lasting more than 250 µs shall meet the static V_{Port} specification.

33.2.8.8 Output current—at short circuit condition

Power shall be removed ~~immediately~~ from the PI of a ~~Type 2~~ PSE ~~if~~ before the PI current exceeds the ~~Safe Operating Area (SOA)~~ upperbound template in Figure 33–9a.

This ties a voltage transient allowance to a requirement that power needs to be removed during a short. This tie needs to be present because the voltage transient may be due to a load change.

This did not show up in this bucket but is related to 247.

Recommended solution to 246, 247, 135

- **Keep text on page 41 as is and modifying page 42 as shown in comment 135.**
- **This concisely clarifies transient requirements are and that power is removed when excessive currents are being drawn.**

Comment 80

Cl **33** *SC* **2.8.4** *P* **42** *L* **38** # 80

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *Vport adhoc*

It is no longer clear that 33.2.8.4 requires Vport to fall into the valid Vport range during a transient load condition (Ipeak). Without this clarification, 3.2.8.4 could come into conflict with 33.2.8.1 which allows power to be removed when Vport drops below Vport_Min. Additionally, there is nothing in 33.2.8.2 (Vport Regulation) that assures a valid Vport level given Ipeak as defined in 33.2.8.4. Additionally, "transient current waveforms" or "peak current waveforms" may be a better term than "AC current waveforms" in line 38 since "AC" in the spec is generally associated with MPS technique rather than overload currents.

33.2.8 Power supply output defines Vport and Ipeak in 33.2.8.4

SuggestedRemedy

One solution: Title 3.2.8.4

PSE maximum continuous and peak output current in normal powering mode at or above minimum output voltage

Separately modify line 38 to use "...peak current waveform..."

This section is valid for all Vport voltages.

Proposed Response *Response Status* **O**

33.2.8.4 ~~Maximum Type 1~~ PSE max output current in normal powering mode at ~~PSE~~ min output voltage

For V_{Port} > ~~44 V~~ V_{Port_min}, the minimum value for I_{Port_max} in Table 33–5 shall be ~~15.4 W~~ (P_{Port} / V_{Port}).
The current I_{Port_max} ensures ~~15.4 W~~ P_{Port} min output power.

The PSE shall support the following AC current waveform parameters:
I_{peak} = (400 / 350) × (P_{Port} / V_{Port}) minimum for 50 ms minimum and 5 % duty cycle minimum.

Recommend Resolution to 80

- **Accept in principle**
- **Change the title of 33.2.8.4 to PSE maximum output current during normal powering mode**
- **Continue to "AC current" or use "time varying current."**

Add text to section 33.2.8.4: Normal Powering mode is the mode where the PSE is required to keep Vport>=Vport_min for Iport<=Ipeak for at least 50 msec.

33.2.8.4 ~~Maximum Type 1~~ PSE max output current in normal powering mode at ~~PSE~~ min output ~~voltage~~

For V_{Port} > ~~44 V~~ V_{Port_min}, the minimum value for I_{Port_max} in Table 33–5 shall be ~~15.4 W~~ (P_{Port_min} / V_{Port}). The current I_{Port_max} ensures ~~15.4 W~~ P_{Port_min} output power.

The PSE shall support the following AC current waveform parameters:
I_{peak} = (400 / 350) × (P_{Port_min} / V_{Port}) minimum for 50 ms minimum and 5 % duty cycle minimum.

Cluster: Definitions

- **4 Definitions: 118, 34, 32, 260**

Comment 118

Cl **33** *SC* **3.5.2** *P* **60** *L* **41** # 118

Vetteth, Anoop Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

This section does not referecnce the power negotiated by the PD over Physical Layer Classification or DLL Classification

SuggestedRemedy

Start the section with a paragraph that references the classified power
Suggestion:
Pport_max is the maximum permissible power negotiated over physical layer classification (per table 33-10) or data link layer classification (as defined in section 33.6a.2.2). Data link layer classification takes precedence over physical layer classification

33.3.5.2 Input average power

The specification for P_{Port} in Table 33–12 shall apply for the input power averaged over 1 second. For a Type 1 PD P_{Port} shall be measured when the PD is fed by 44 V to 57 V with 20 Ω in series. For a Type 2 PD P_{Port} shall be measured when the PD is fed by ~~44 V~~ 50 V to 57 V with 12.5 Ω in series. P_{Port} is defined as:

$P_{Port} = V_{Port} \times I_{Port}$

definitions

Comment 118 Recommended Resolution

- **Accept in principle.**
- **33.3.5.2 provides a definition for Pport measurement.**
  A reference to classification section 33.6 should be made at the end of this section.
  "The maximum value of Pport is obtained as described in section 33.6 (33.2.7 select the best location)."
- **The introduction to section 33.6 needs to cover how to arrive at Pport using L1, L2, and default means.**
- **Who is responsible for crafting this introduction?**
  Classification ad hoc.

Comment 34

Cl **33** *SC* **3.5.2** *P* **60** *L* **47** # 34

LANDRY, MATTHEW SILICON LABS

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The equation and instructions for measuring PPort seem unnecessary. The power limit applies regardless of the PSE voltage and cable impedance.

The sudden appearance of a resistive approximation of the cable plant really adds nothing for the reader. Stating that the power limit applies over the specified input voltage range is simply redundant. Telling the reader that power equals voltage times current is a bit patronizing.

SuggestedRemedy

Replace 33.3.5.2 with the following:

33.3.5.2 Input average power

The specification for PPort in Table 33-12 (item 2) shall apply for the input power averaged using any sliding window with a 1s width.

33.3.5.2 Input average power

The specification for P_{Port} in Table 33–12 shall apply for the input power averaged over 1 second. For a Type 1 PD P_{Port} shall be measured when the PD is fed by 44 V to 57 V with 20 Ω in series. For a Type 2 PD P_{Port} shall be measured when the PD is fed by ~~44 V~~ 50 V to 57 V with 12.5 Ω in series. P_{Port} is defined as:

$P_{Port} = V_{Port} \times I_{Port}$

2	Input average power	P_{Port}	W		12.95	1	See 33.3.5.2
					29.5	2	

Proposed solution to 34

Propose to accept.

33.3.5.2 Input average power

The specification for PPort in Table 33–12 shall apply for the input power averaged over 1 second. (No change)

33.3.5.2.1 System Stability Test Conditions

PPort shall be measured when the PD is fed by Vport_min to Vport_max with Rchannel_max in series.

PPort is defined as:

PPort = VPort × IPort

Where

Pport is the average input power

Vport is the static input voltage

Iport is the input current, either DC or RMS.

Rchannel_max is defined in Table TBD. (Table TBD should contain Channel Model data such: Class C 40 Ohms, Class D 25 Ohms, DC resistance unbalance etc.)

Comment 32

Cl **33** *SC* **3.5** *P* **59** *L* **22** # 32

LANDRY, MATTHEW SILICON LABS

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Table 33-12 item 2 describes max static power. This can be expressed in terms of current and Vport.

SuggestedRemedy

Replace Type 1 max PPort with 0.35*VPort min. Replace Type 2 max with ICable*VPort min.

These equations presume that VPort mins are updated to 37V and 41V, respectively.

2	Input average power	P_{Port}	W		12.95	1	See 33.3.5.2
					29.5	2	

Same as comment 260.

Comment 260

Cl **33** *SC* **3.5** *P* **59** *L* **22** # 260

Stanford, Clay Linear Technology

Comment Type **E** *Comment Status* **A** *Vport adhoc*

We decided to not reference the actual power levels but use parameters.

Change 29.5W to Icable * Vport_min

Do we do the same for 12.95W????

SuggestedRemedy

Same as comment 32.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

for item 2 max is Icable*Vport min, applies to type 1 and 2.
see 32

2	Input average power	P_{Port}	W		12.95	1	See 33.3.5.2
					29.5	2	

Comment 32 & 260 proposed resolution

- **Accept in principle.**
- **The PD power maximum is generically Icable (Vport_min).**
- **A table is being created to describe the channel that will contain definitions similar to:**
  Class C, Icable <= 350 mA
  Class D, Icable <= 720 mA

Maximum

Icable (Vport_min)

Max

2	Input average power	P_{Port}	W		12.95	1	See 33.3.5.2
					29.5	2	

Also see 137.

Cluster: Matching PSE and PD currents

- **15 Matching PSE and PD currents:**
- **Static Vport: 105, 31, 259, 95**
- **SOA Curve: 90, 139, 59, 94, 165**
- **Police: 79, 56, 249, 36, 9**
- **PSE current requirements: 143, 137, 114, 227**

Comment 105

Cl **33** *SC* **3.5.1** *P* **60** *L* **31** # 105

Darshan, Yair — Microsemi Corporation

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Draft D1.0:
Table 33-12 item 1 (Vport) may lead to confusion in the future regarding to how it was derived.
The facts are:
a) Vport minimum for type 1 was derived at peak input power (0.4A) and not at steady state current (0.35A).
(44v-20 ohms * 0.4A=36V.)
(44v-20 ohms * 0.35A=37V.)
The same concept is relevant to Type 2 PSE.
We need to clarify it in the text of 33.3.5.1

SuggestedRemedy

Change line 31 from:

"The specification for VPort in Table 33-12 is for the input voltage range after startup, and it includes loss in the cabling plant."

to:
"The specification for VPort in Table 33-12 is for the input voltage range after startup, and it includes loss in the cabling plant at PD maximum peak load current, as defined by table 33-12 item 4.
PD input voltage at maximum average current is given in Table 33-12 item 5."

see 31, 259 which suggest changing item in table to 37V.

Table 33-12

1	Input voltage	V_{Port}	Vdc	36	57	1	See 33.3.5.1
				40	57	2	

Table 33-12

5	Input current (DC or RMS)						
	At V_{Port} = 37 Vdc	I_{Port}	A		0.35	1	See 33.3.5.4
	At V_{Port} = 57 Vdc				0.23		
	At V_{Port} = 41 Vdc	I_{Port}	A		I_{Cable}	2	
	At V_{Port} = 57 Vdc				0.52		

Table 33-12

4	Peak operating current, Class 0, 3	I_{Port}	A		0.4	1	See 33.
	Peak operating current, Class 1				0.12	1	
	Peak operating current, Class 2				0.21	1	
	Peak operating current, Class 4				(400/350) × I_{Cable}	2	

Related to comments 31, 259.
OBE 31

Proposed Resolution to 105

Accept in principle.
This text references related information.

⇒OBE by comment 31
Which improves the transient spec.
Type 2 loads: normal; PD surge; PSE

Cl 33 *SC* 3.5 *P* 59 *L* 16 # 259
Stanford, Clay Linear Technology

Comment Type T *Comment Status* X

PD input voltage should be 37V, not 36V. We clarified this by adding the transient section 1a.

Transient section 1a needs to define Type 1 and Type 2 PSEs.

SuggestedRemedy

Table 33-12, item 1
Vport min IS 36V for a type 1.

Table 33-12, item 1
Vport min SHOULD BE 37V for a type 1.

Is "DC" static? Is 50 mS at a value DC?

1	Input voltage	V_{Port}	Vdc	36	57	1	See 33.3.5.1
				40	57	2	

Cl 33 *SC* 3.5 *P* 59 *L* 16 # 31
LANDRY, MATTHEW SILICON LABS

Comment Type T *Comment Status* X

Item 1 should be describing static VPort, while 1a can describe transient VPort.

SuggestedRemedy

(1) Change item 1: 37V min, 57V max for Type 1. 41V min, 57V max for Type 2.

(2) Change item 1a to apply to Type 1 and Type 2. Note to "see 33.3.5.1"

(3) Adjust note in 33.3.5.1 to say: "The specification for Vport in Table 33-12 (item 1) and VTran_lo (item 1a) is for the input voltage range after startup, and takes into account loss in the cabling plant."

Comment 95

Cl **33** *SC* **Table 33-12** *P* **59** *L* **17** # 95

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Draft D1.0:

Related to 105, 31, 259

Table 33-12 items 1:
It is 39.71V and not 40V (50-12.5 OHMS x 0.72A*0.4A/0.35A=39.71V).

SuggestedRemedy

Table 33-12 item 1 for type 2 PD:
Change PD minimum operating voltage to 39.71V.

How many significant digits does the IEEE use?

two: 40 V; three 39.7 V; …

see 31, recommended 41V…

1	Input voltage	V_{Port}	Vdc	36	57	1	See 33.3.5.1
				40	57	2	

Cl **33** *SC* **3.5** *P* **59** *L* **16** # 31

LANDRY, MATTHEW — SILICON LABS

Comment Type **T** *Comment Status* **X**

Item 1 should be describing static VPort, while 1a can describe transient VPort.

SuggestedRemedy

(1) Change item 1: 37V min, 57V max for Type 1. 41V min, 57V max for Type 2.

(2) Change item 1a to apply to Type 1 and Type 2. Note to "see 33.3.5.1"

(3) Adjust note in 33.3.5.1 to say: "The specification for Vport in Table 33-12 (item 1) and VTran_lo (item 1a) is for the input voltage range after startup, and takes into account loss in the cabling plant."

Accept this: Significant digits: depends but adjust to increase system margin. 39.7 V

Comment 33

Cl **33** *SC* **3.5.4** *P* **61** *L* **36** # 33

LANDRY, MATTHEW SILICON LABS

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The equations use absolute numbers for the port power. They should be variables, which has the added benefit of needing only one equation.

Use variables for calculating Iport.

SuggestedRemedy

Replace equation with:
IPort_max = PPort_max / VPort
where
IPort_max is the max DC and RMS input current
PPort_max is the maximum power as defined in Table 33-12 item 2
VPort is the static input voltage

Remove reference to Type 1 PDs, and remove second equation entirely.

Accept in principle.

The maximum I_{Port_dc} and I_{Port_rms} values for all operating V_{Port} range shall be defined for Type 1 PDs by the following equation: ~~I_{Port_max} [mA] = 12950/V_{Port}~~

~~$I_{Port\_max} = \frac{12.95}{V_{Port}}$~~

where

I_{Port_max}	is the maximum DC and RMS input current
V_{Port}	is the static input voltage

The maximum I_{Port_dc} and I_{Port_rms} values for all operating V_{Port} range shall be defined for Type 2 PDs by the following equation:

$I_{Port\_max} = \frac{29.5}{V_{Port}}$

where

I_{Port_max}	is the maximum DC and RMS input current
V_{Port}	is the static input voltage

Comment 90

Cl **33** *SC* **figure 33-9a** *P* **44** *L* **39** # 90

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Draft 1.0:

The title of figure 33-9a is "PI operating current template"
It is only defines the maximum current.
In addition it contains error: The current after 75msec is Icable*0.4/0.35 and not 720mA.

SuggestedRemedy

Option A: (Recomended)

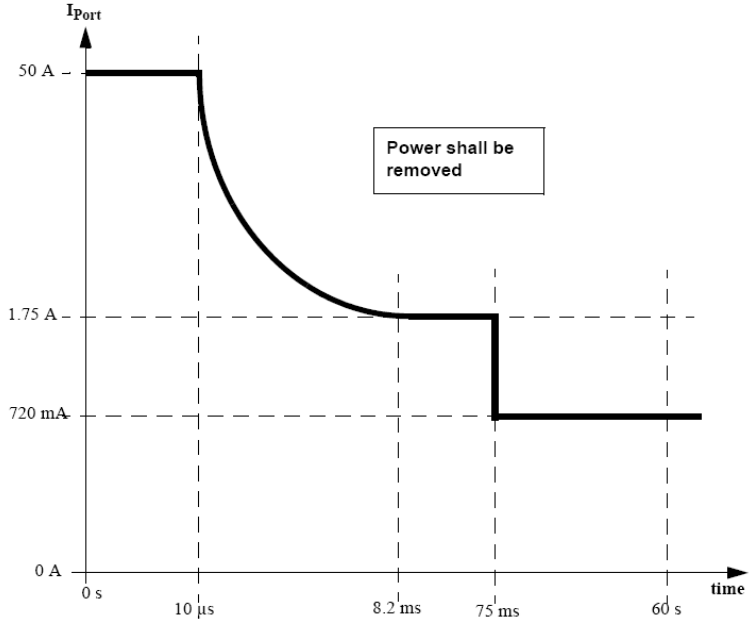
Delete figure 33-9a and use only figures 33-12b and figures 33-12c due to the fact that they contains PSE and PD data and hence figure 33-9a is redundant.

Option B:

Fix error in figure 33-9a and change title to read:
"Figure 33-9a - PSE PI maximum operating current vs. Time"

Proposed Response *Response Status* **O**

third time commentor pointed out Icable*.4/.35…



Accept in principle.
OBE by 81 solution.
We need one set of figures that the PSE and PD sections reference.
We need to decide how to arrive at PSE current requirements before this can be accomplished.

Comment 139

Cl **33** *SC* **2.8.8** *P* **44** *L* **27** # 139

Schindler, Fred Cisco Systems

Comment Type **TR** *Comment Status* **A**

Replace 720 mA on Figure 33-9a with 400/350xIcable.

SuggestedRemedy

Replace 720 mA on Figure 33-9a with 400/350xIcable.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

OBE see 57

Accept in principle.
OBE by 81 solution. Same as 90.

We need one set of figures that the PSE and PD sections reference.

We need to decide how to arrive at PSE current requirements before this can be accomplished.

Comment 59

Cl **33** *SC* **3.5.4a** *P* **62** *L* # 59

Vetteth, Anoop Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Figure 3-12b and 3-12c
This is PD section and hence the SOA curve for the PSE is irrelevant.

PD_Toverload was defined in the presentation. The maximum value of PD_Toverload is PSE_Tcutmin. Hence PD_Toverload is not relevant anymore.

SuggestedRemedy

Remove the SOA curve for the PSE from both the figures.

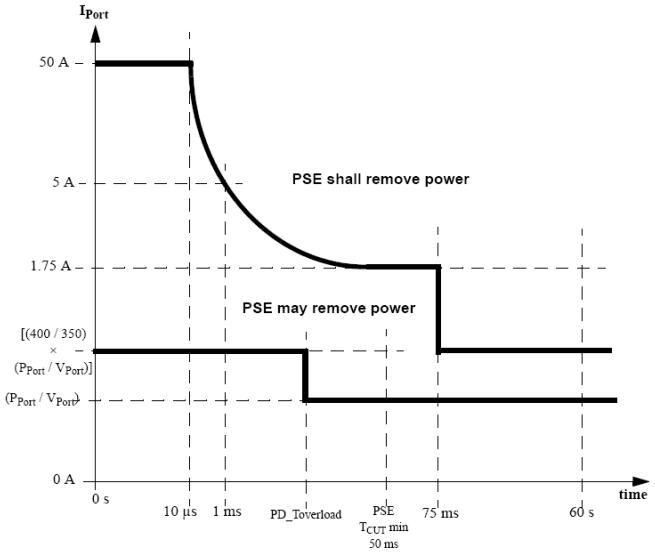
Remove PD_Toverload and make the overload max duration to PSE_Tcutmin

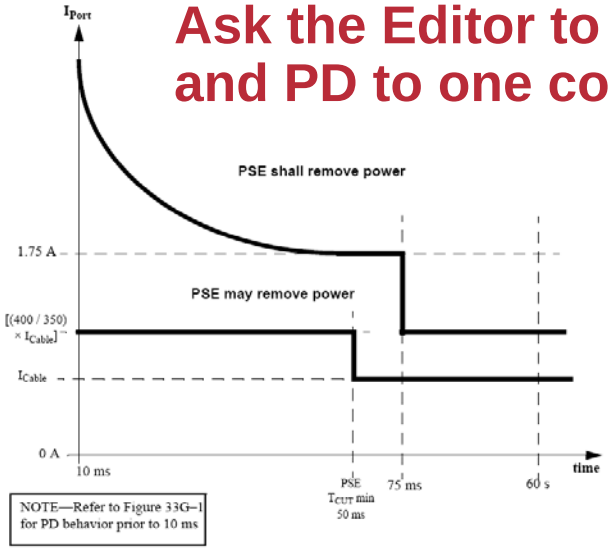
Explain the mask in text using inequalities.

Accept in principle.

Related to 94.

Ask the Editor to point the PSE and PD to one combined curve.





Comment 94

Cl **33** *SC* **figure 33-12b** *P* **62** *L* **31** # 94

Darshan, Yair — Microsemi Corporation

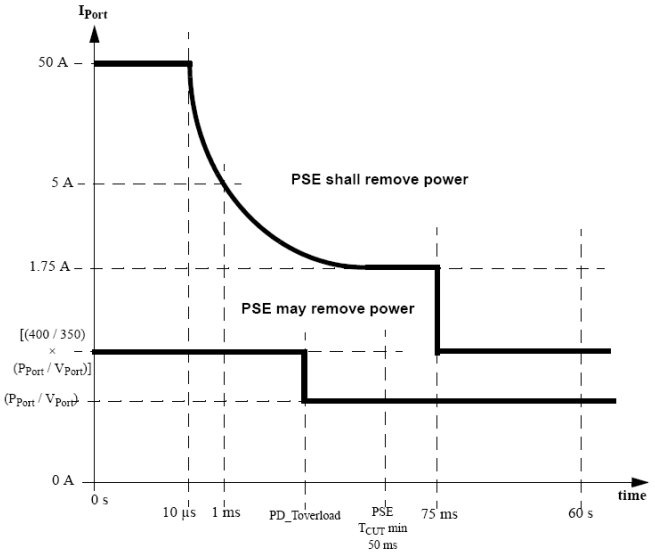
Comment Type **TR** *Comment Status* **D** *Vport adhoc*

It can be understood from the drawing the PSE may remove power at I=0.9999999999*(0.4/0.35)*(Pport/Vport) and t=49.99999999msec which is incorect.
PSE must not remove power at this region due to the fact that PD allowed to take peak current up to this point.
It is ILIM_MIN.

SuggestedRemedy

1. Move the solid hirizontal line from PD_Tovld to Tcut_min.
2. Delete PD_Toverload due to the fact that it doesnt add additional information.
3. Add "PSE shall not remove power" below the PD max. operating current curve.

4. See figure 33-12c and add the "PSE shall not remove power" below the PD max. operating current curve.
The rest is OK.



Accept in principle.

OBE by 59 and change Pport to Pport_max, Vport becomes Vport_static.

Comment 165

Cl **33** *SC* **3.5.4a** *P* **62** *L* **48** # 165

Jones, Chad Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

"During transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for up to 10 ms." This is a PSE design requirement (though it does not carry a shall, it is information that a PSE designer should know) and it is located in the PD section. I can't find the corresponding information in 33.2.

SuggestedRemedy

Find an appropriate place in 33.2 to add this information, perhaps 33.2.8.2b.

Accept in principle.

We need one set of figures that the PSE and PD sections reference.

Comment 79

Cl **33** *SC* **2.8.4** *P* **42** *L* **39** # 79

Johnson, Peter — Sifos Technologies

Comment Type **T** *Comment Status* **D** *Vport adhoc*

The formula as written is confusing and should be corrected to avoid breaking 802.3af specification where any PD is allowed to draw 400 mA for 50 msec.

SuggestedRemedy

Ipeak = (400 / 350) x (Port / Vport_Min) for 50 msec minimum and 5% duty cycle minimum.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Defer to Vport adhoc
The remedy recomends changing Vport to Vport_min in the formula.

You get a peak current at a minimum voltage.
A PD can draw a maximum power at its lowest voltage input.
This may disagree with the goals of # 56.

OBE by 114

Comment 56

Cl **33** *SC* **2.8.6** *P* **43** *L* **30** # 56

Vetteth, Anoop Cisco

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

the denominator of the equation should be Vport and not Vportmin. The minimum value of Icut should be equal to the value of Iport_max as defined in 33.2.8.4

SuggestedRemedy

Change the denominator of the equation to Vport

Proposed Response *Response Status* **O**

A PSE needs to support the maximum PD demand.
The power provided is dependent on the PSE port voltage.

This may disagree with the goals of # 79.

OBE by 114

Comment 249

Cl **33** *SC* **2.8.6** *P* **43** *L* **31** # 249

Stanford, Clay — Linear Technology

Comment Type **T** *Comment Status* **D** *Vport adhoc*

Icut is being re-defined to allow current to be limited to PD power rating.

In equation, I think the intent is for the PSE to use the actual port voltage to calculate the allowed current.

Therefore, Vport_min should be Vport-operation, or Vport-actual.

SuggestedRemedy

A PSE needs to support the maximum PD demand.
The power provided is dependent on the PSE port voltage.

Same as # 56.

OBE 114

Comment 36

Cl **33** *SC* **3.5** *P* **59** *L* **38** # 36

LANDRY, MATTHEW SILICON LABS

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Item 5 is really doing nothing more than telling the reader that IPort should scale with VPort.

They reader should already know this, as PPort max is a max power. Clearly if VPort moves, IPort has to move.

That being said, how is item 5 at all helpful?

Power = Iport x Vport, so table entry 5 is not required.

related to # 56.

OBE 114

SuggestedRemedy

(1) Strike item 5.

or

(2) Remove the multiple lines, and replace item 5 with:
Item: 5
Parameter: Input current (DC or RMS)
Symbol: IPort
Unit: A
Min:
Max: PPort max / VPort
PD Type: 1,2
Addl Info: See 33.3.5.4

5	Input current (DC or RMS)						
	At V_{Port} = 37 Vdc	I_{Port}	A		0.35	1	See 33.3.5.4
	At V_{Port} = 57 Vdc				0.23		
	At V_{Port} = 41 Vdc	I_{Port}	A		I_{Cable}	2	
	At V_{Port} = 57 Vdc				0.52		

Comment 9

Cl **33** *SC* **2.8** *P* **41** *L* **7** # 9

LANDRY, MATTHEW SILICON LABS

Comment Type **T** *Comment Status* **D** *Vport adhoc*

ICUT is optional. ICUT min should be the maximum current the PD can draw at a given port voltage (PClass/VPort). It is.

To maintain the use of the TCUT timer, the maximum ICUT should be less than or equal to the current limit. This is almost true for Type 1. We have a TBD for Type 2.

We need to specify an ICUT max that meets the criteria above.

SuggestedRemedy

Change ICUT max to ILIM.

This will open up the ICUT space a little wider for Type 1 PSEs (e.g. if ILIM is 425mA, then ICUT could be 424mA), but will also properly let the SOA curve guide ICUT for all future PSEs.

Note that it does not break compliance of current PSEs, and still supports both current limited and energy limited PSEs.

This is from the PSE section.

8	Overload current detection range	I_{CUT}	A	P_{Class}/V_{Port}	0.4	1	Optional limit; See 33.2.8.6
				P_{Class}/V_{Port}	TBD	2	

Accept.

Comment 143

Cl **33** *SC* **3.5.4** *P* **61** *L* **17** # 143

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The value of Iport_max created by the formula-using PD Pport_max-does not match the value provided in table 33-12. For example, class 0 PD power is 12.95 W maximum and 12.95W/36V = 360 mA, not the 400 mA shown in table 33-12, item 4.

SuggestedRemedy

The PD formula provides the correct answers when the PSE Pport_max values are scaled by 400/350 for the system classified power. A presentation will be provided at the Atlanta Plenary to cover the details.

33.3.5.4 Peak operating current

At any static voltage at the PI and PD operating condition the peak current shall not exceed P_{Port} max/V_{Port} for more than 50ms max and 5% duty cycle max. Peak current shall not exceed I_{Port} max.

Withdraw

Comment 137

Cl **33** *SC* **2.8.4** *P* **42** *L* **35** # 137

Schindler, Fred — Cisco Systems

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

The value for Ipeak is incorrect.

SuggestedRemedy

The correct value for Ipeak = (Vpse - SQRT(Vpse^2 - 4RchPpd_port_peak))/(2Rch). More details can be found in a presentation that will be provided during the Atlanta Plenary meeting.

$$I_{peak} = \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4R_{ch}P_{PD\_port\_peak}}}{2R_{ch}}\right)$$

33.2.8.4 ~~Maximum Type 1~~ PSE max output current in normal powering mode at ~~PSE~~ min output voltage

For V_{Port} > ~~44 V~~ V_{Port_min}, the minimum value for I_{Port_max} in Table 33–5 shall be ~~15.4 W~~ (P_{Port} / V_{Port}). The current I_{Port_max} ensures ~~15.4 W~~ P_{Port} min output power.

The PSE shall support the following AC current waveform parameters:
I_{peak} = (400 / 350) × (P_{Port} / V_{Port}) minimum for 50 ms minimum and 5 % duty cycle minimum.

Accept in principle.

The new PD table 33-12, item 4, replace peak operating current with peak operating power as per next slide.

Solution for 137

In Table 33-12 item 4, change current to power, and Iport to Ppeak.

OLD	NEW
400	14.4
120	5.0
210	8.36

(400/350) × I_{Cable}

$$\frac{400}{350}\frac{P_{port\_max}}{V_{port\_static\_min}}V_{port\_min}$$

MAX

4	Peak operating ~~current~~, Class 0, 3 power	~~I_{Port}~~ Ppeak	~~A~~ W		~~0.4~~ 14.4	1	See 33.3.5.4
	Peak operating ~~current~~, Class 1 power				~~0.12~~ 5.0	1	
	Peak operating ~~current~~, Class 2 power				~~0.21~~ 8.36	1	
	Peak operating ~~current~~, Class 4 power				~~(400/350)~~ × I_{Cable}	2	

Comment 114

Cl **33** *SC* **2.8.4** *P* **42** *L* **38** # 114

Darshan, Yair — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

1. The editor was not authorized to make the changes in this clause due to the fact that the remedy suggested by the ad-hoc was not concluded and adopted.

2. In addition, the new text makes legacy PSE non compliant due to the fact that the peak power for type PSE is not function of (Pport/Vport)*(0.4/0.35) for class 1 and 2. It is correct only for class 0,3.

3. The peak current is already defined in Table 33-12 item 12 (Ed note: Item 4) and we don't need to define it again for the PSE due to the simple physical fact the PSE output current is equal to the PD input current..

SuggestedRemedy

Option 1: (Not recommended)
Restore the old text.

Option 2: (Recommended)

Replace the text in line 38 from:
"The PSE shall support the following AC current waveform parameters:
Ipeak = (400 / 350) [a] (PPort / VPort) minimum for 50 ms minimum and 5 % duty cycle minimum."

To:
"The PSE shall support the following the maximum peak current as defined by Table 33-12 item 4 for 50 ms minimum and 5 % duty cycle minimum."

Note to the group:
1. The peak current already defined in table 33-12 item 4. No need to repeat it again.
2. The peak current numbers should be defined in one place i.e. in the PD side due to the fact that it is defined by the load and the PSE has only to support it.
3. The peak current with option b remedy is function of (0.4/0.35)*Port/Vport only for Type 2 PD due to the fact that we don't have to take in account previous legacy definitions.
For type 1 class 1 and 2 PDs, the constant power model contains some margin from reasons that was explained in my presentation (that was not presented yet) which is located at the web site of the October 2007 meeting).
3. For class 0,3 the peak current is a constant and not a function of Vport.
(The average current was described as a function of Pport/Vport.)
Taking all this data in account, leads to the suggested remedy of option b.

Accept in principle
OBE 137

Comment 227

Cl **33** *SC* **2.8.4** *P* **42** *L* **38** # 227

Law, David 3Com

Comment Type **TR** *Comment Status* **D** *Vport adhoc*

Please provide definitions for the variables used in this equation.

SuggestedRemedy

Suggest that this text be changed to read:

The PSE shall support an AC current of Ipeak minimum for 50 ms minimum and 5 % duty cycle minimum.

Ipeak = (400 / 350) × (PPort / VPort)

Accept in principle
OBE 137

Where:

IPeak is the peak output current.
PPort is the minimum continuous output power (see Table 33-5, item 14).
VPort is the minimum static output voltage (see Table 33-5, item 1).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.
NOTE: Yair has comment that could remove this section.