Transformer and Channel ad hoc

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1 ad hoc with an average attendance of 15 people since the last report.

Agenda

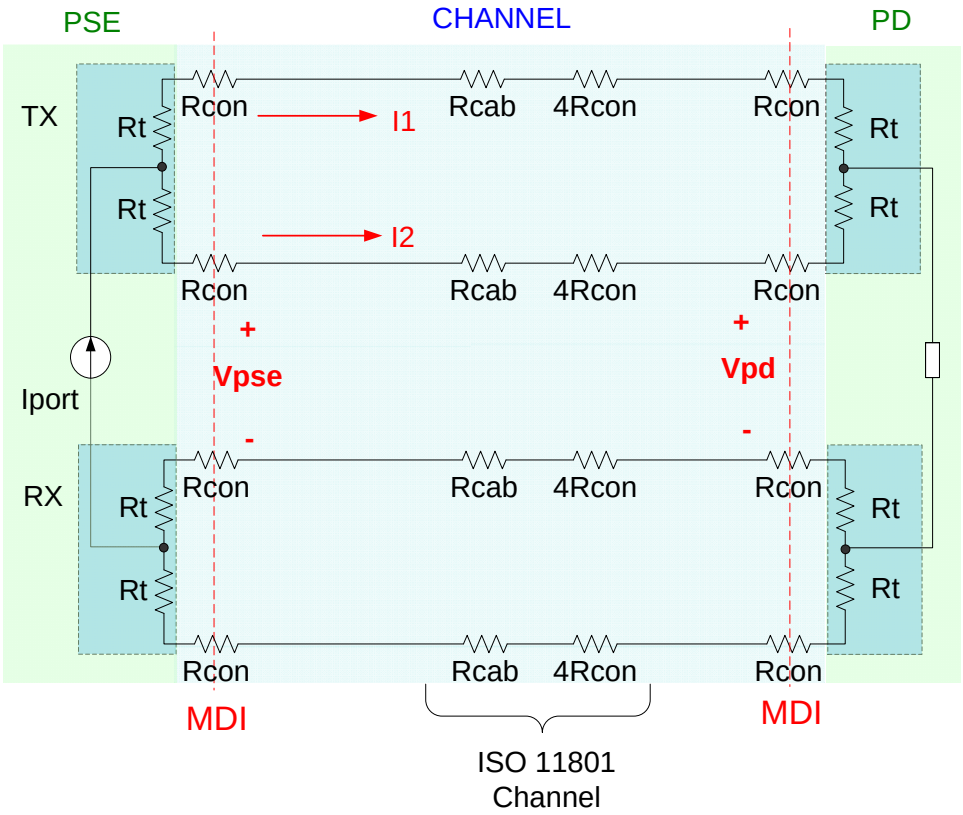
- **Approach taken (abridged version)**
- **Update on progress**
- **Q & A**
- **Next step.**

This is a work in progress: Trends are useful, model specifics are in development.

Approach Taken

- **Agree on a system model for current unbalance calculations.**
- **Use IEEE 802.3 requirements and legacy system data to refine the model used.**
- **Use the refined approach to model IEEE 802.3at current unbalance.**

The Channel Models: Detailed IEEE 802.3



$$I_1 = I_{cable} \frac{\sum R_{\max} // \sum R_{\min}}{\sum R_{\max}}$$

$$I_2 = I_{cable} \frac{\sum R_{\max} // \sum R_{\min}}{\sum R_{\min}}$$

$$I_{UNBAL} = I_{cable} \times \sum R_{\max} // \sum R_{\min} \left(\frac{1}{\sum R_{\min}} - \frac{1}{\sum R_{\max}}\right)$$

The worst-case current unbalance is modeled by combining the ISO channel resistance unbalance with an MDI connections and transformer resistance.

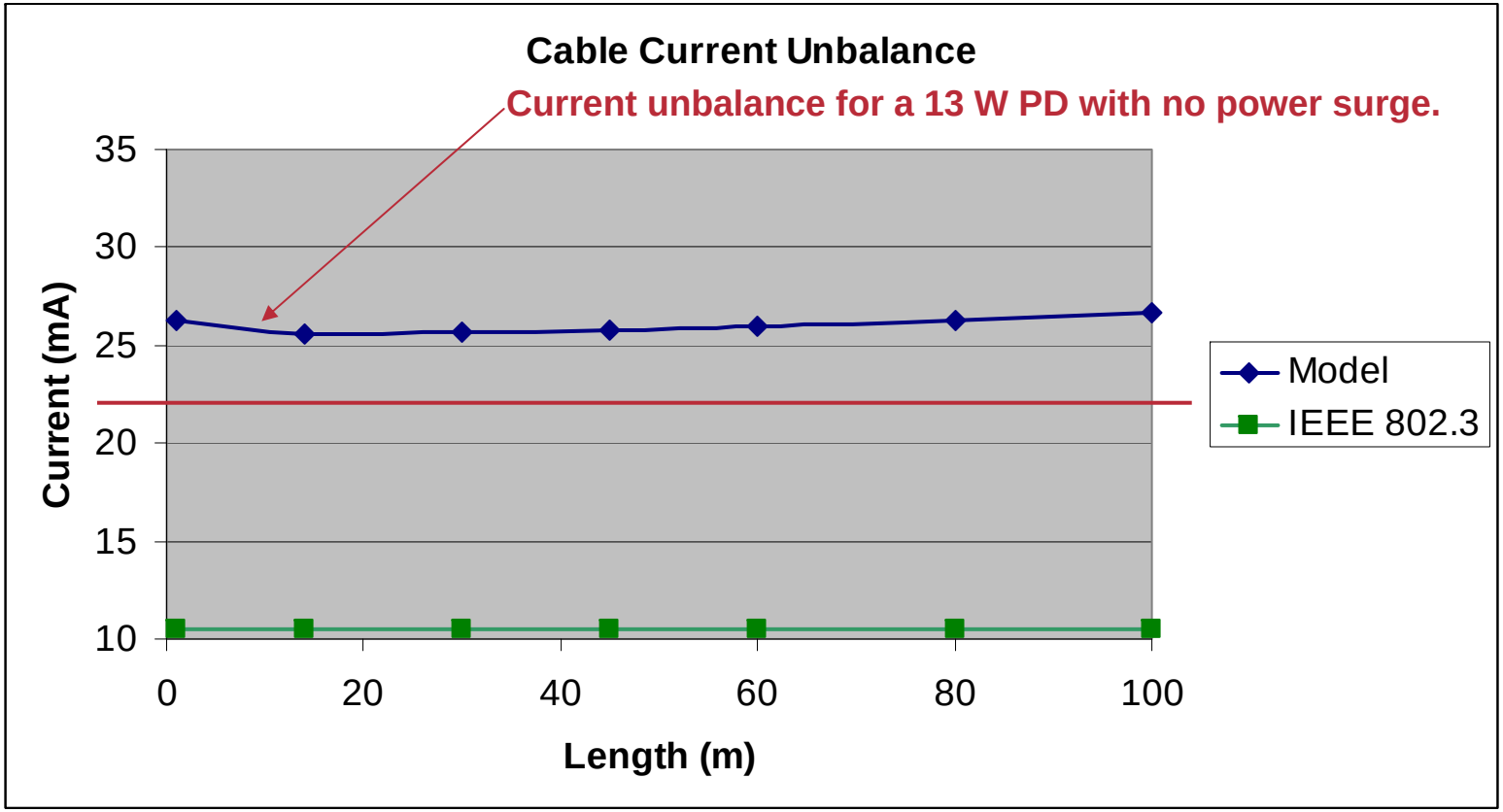
a // b => Replace with the resistance of “a” in parallel with “b”.

Adjusted model for legacy PoE

System Failure

Vendor Average

Interoperability



Adjustments:
- Use root-of-the-sum-of-squares for connectors and transformer.

Ad Hoc Discussions

- **What open circuit inductance reduction has a significant impact on realizing PoE plus magnetics? OCL_min = 350 uH now. At what OCL would manufacturing be easier?**
  Legacy (15 mA): 15% to 30% PoE plus(25 mA): 30% to 50%
- **How significant to realizing PoE magnetics is adding a PD surge allowance of Ppd_ave x 400/350?**
  Legacy: significant PoE plus: not significant
  The OCL is design target is for Ibias_max_ave.
  Icut will consume OCL design margin.

A (400/350 – 1) change in current reduces inductance by approximately the same amount.
m = -16%/14% = -1.1

What does this portion of the curve look like?

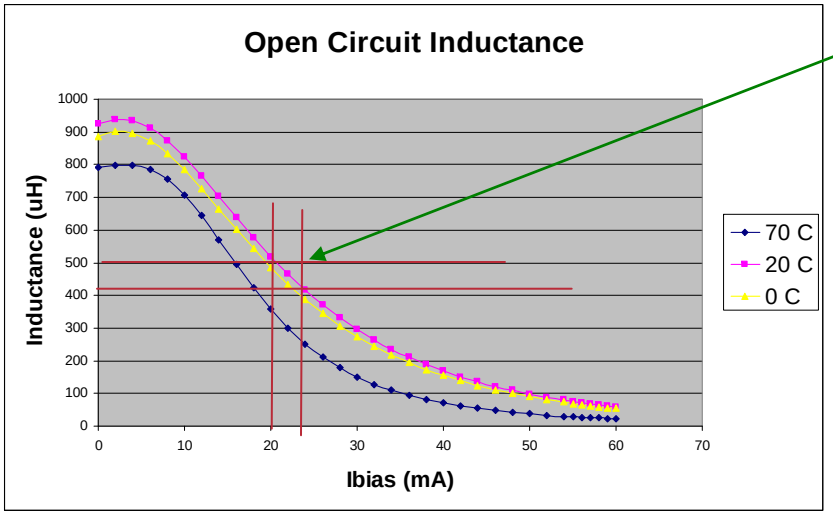
Curve courtesy of Wurth Electronics Midcom, Dean Huumala

Ad Hoc Discussions Continued

- **Are you aware of legacy PD customers that use the PD surge allowance? If so provide details.**

  No participant was aware of a compliant PD that uses surge power.

  The Vport ad hoc did not receive data for a PD that uses surge power.



A (400/350 – 1) change in current reduces inductance by more than the previous example.
m = -20%/14% = -1.4

Curve courtesy of Microsemi, Yair Darshan

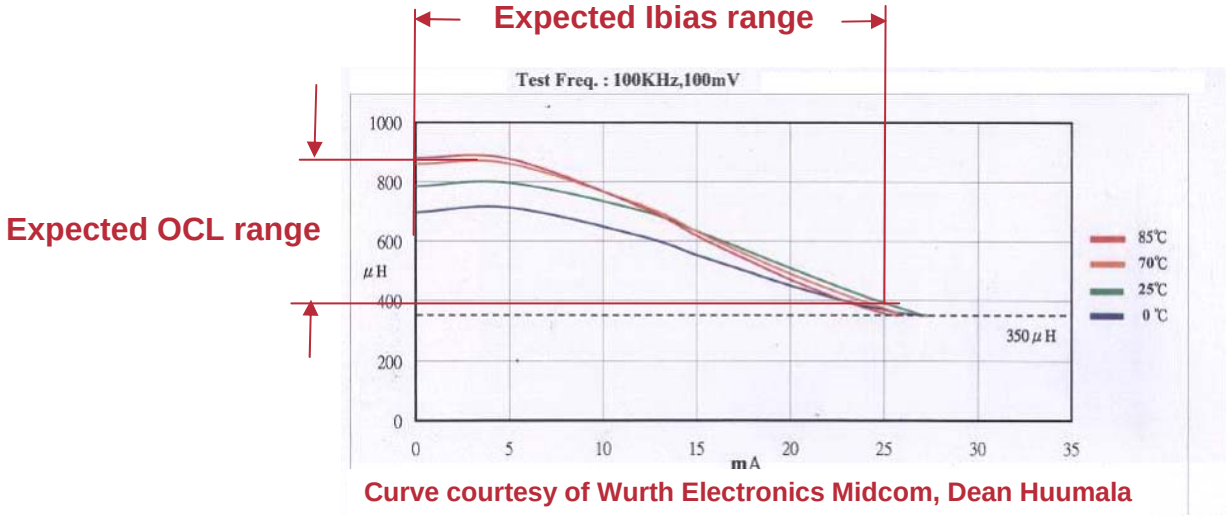
Ad Hoc Discussions Continued

- **What affect will varying TX and RX inductance have on data communication?**
- **Is there an AC and DC component to the affect bias current will have on system data integrity?**

Legacy PoE system rarely change their power demand. Newer systems are expected to move between a power levels.

Will PHY circuits be able to respond to changing system inductance?

DC => Average demand, assume yes.
AC => Ripple and changes to demand, need PHY vendor data.



Curve courtesy of Wurth Electronics Midcom, Dean Huumala

PHY Baseline Wander Correction

- **Baseline wander correction provides low frequency gain at the receiver to improve data recovery.**
- **The correction is not done at the transmitter because larger voltages are not easily accommodated.**
- **Baseline wander correction has been done on most PHYs since 100BASE-TX was ratified in 1995.**
- **Some PHY vendors improved baseline wander to accommodate PoE testers and midspan PSEs. These support a cascade of transformers. A single transformer can have its inductance lower by more than a factor of 2 and interoperate at 100 MBPS.**

PHY baseline wander correction provides a significant benefit to transformer OCL.

Using a Statistical Model

- **The model will be used to calculate the likelihood of a condition. For example, Ibias, or OCL.**
- **For legacy PoE parameters historical data is used.**
- **For PoE plus parameters IEEE specifications requirements will be used.**

Legacy worst-case scenario components

- **PD maximum power** — **25%**
- **PD surge power** — **5%**
- **Minimum PSE voltage** — **0.01%**
- **Highest Channel resistance (length and quality)** — **0.001%**
  - **This increases Iport**
- **Lowest Inductance (I_{bias_max}, T_{A_min})** — **0.02%**
  - **This reduces data signal strength**
- **100BASE-TX, Killer Packet** — **This is being refined.** — **7E-42**
  - **This needs occur repeatedly to prevent communication. The scrambler has 11 bits.**
- **PHY without baseline wander correction** — **1E-7**

The probability of data loss on copper based Ethernet at this point of time due to PoE unbalance current: 1 in 10^61 multiplied by the number of ports in use. => ~0

Failure remains unlikely whether baseline wander correction is used or not.

Question

- **Is there a real benefit to testing how much the OCL can be lowered when baseline wander correction is used?**

  This may eliminate baseline wander as an option and would help build confidence in using this approach.

- **If baseline wander correction ensured interoperation would you be willing to mandate its use for PoE plus if the operating point OCL was less than 350 uH?**

Options that could be used

1. **Accept IEEE 802.3at D3.0 values.**

   Y: 13 N: 7

2. **Determine an OCL value for economically feasible magnetics using the same or smaller form factor as legacy solutions. Then have PHY vendors confirm whether recent baseline wander correct methods will ensure interoperation at all required data rates.**

   Y: 18 N: 2

3. **Use statistics to determine the likelihood that the transformer OCL is below 350 uH and if that value is below ??? consider the system interoperable at the parameter levels selected.**

   Y: 16 N: 2

4. **Alternative A Midspan PSEs continue to be out of scope.**

   Y: 2 N: 13

Which option does the Task Force want to support?
Who will help?

The age of the universe is generally considered to be 14B years.

Next Step

- **Use the approve approaches to calculate IEEE requirements.**
- **Get PHY vendor input on time-varying inductance concerns.**
- **Get more transformer vendor OCL vs current and temperature data.**
- **Get more help to support these efforts.**