Replace Clause 33:

33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

33.1 Overview

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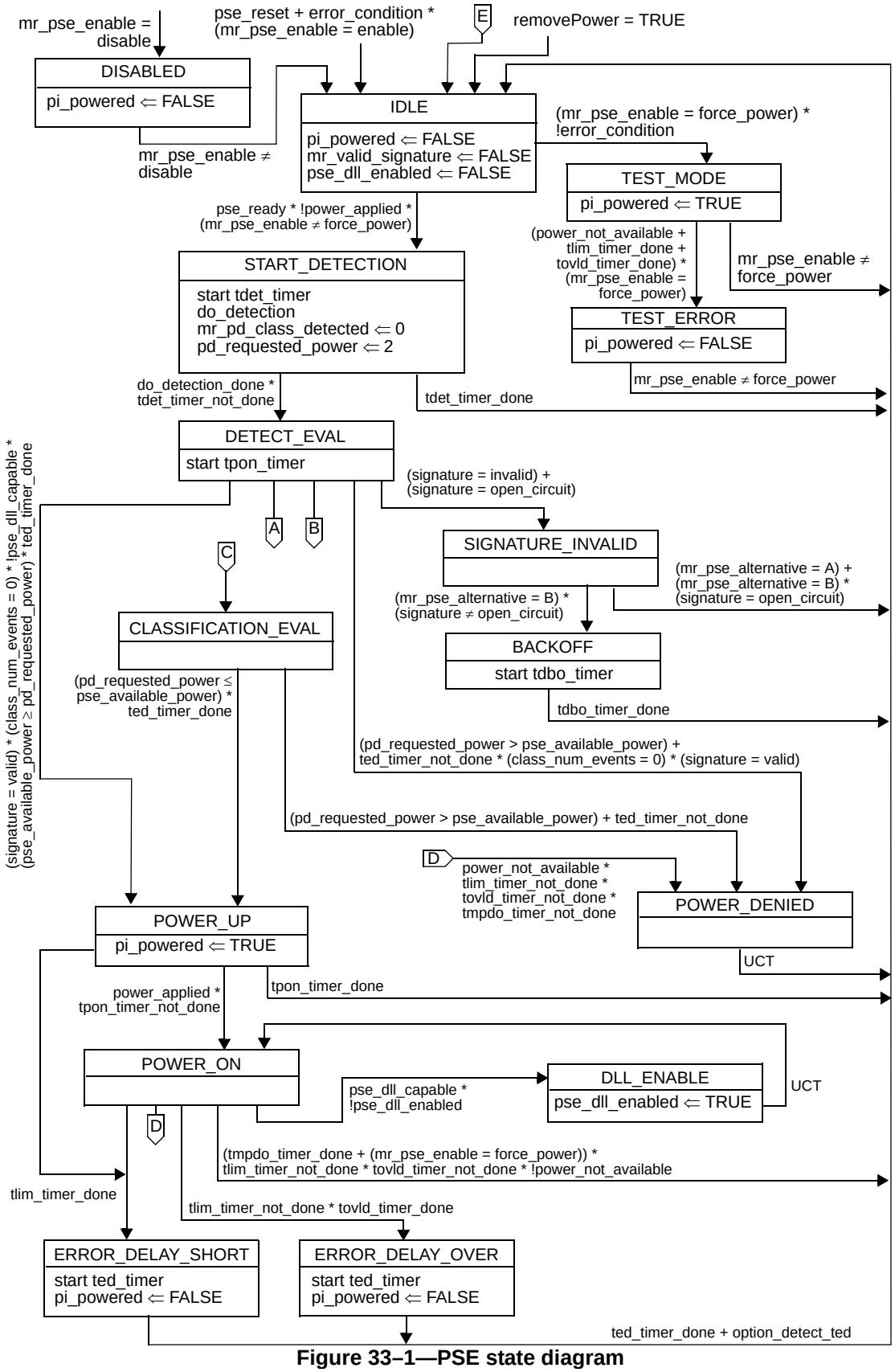

Figure 33–1—PSE state diagram

33.3 Powered devices

33.4 Additional electrical specifications

33.5 Environmental

33.6 Management function requirements

33.7 Data Link Layer classification

[EDITOR'S NOTE—Update the below noted 802.1AB reference to reflect the proper revision during preparation for publication.]

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Annex G of IEEE Std 802.1AB™-200X protocol (LLDP). Type 2 PDs that require more than 12.95 W must support Data Link Layer classification (see 33.3.5). Data Link Layer classification is optional for all other devices.

33.7.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB™-200X; shall support the DTE Power via MDI classification Type, Length, Value (TLV) defined in 33.7.2; and shall support the control state diagrams defined in 33.7.6.

A device implementing Data Link Layer classification shall send power management Protocol Data Units (PDUs) and process PDUs received from the remote device at least once every 30 seconds. Each power management PDU shall contain the DTE Power via MDI classification TLV.

33.7.2 DTE Power via MDI classification TLV

The DTE Power via MDI classification TLV is used to perform Data Link Layer classification. Figure 33–2 shows the format of this TLV.

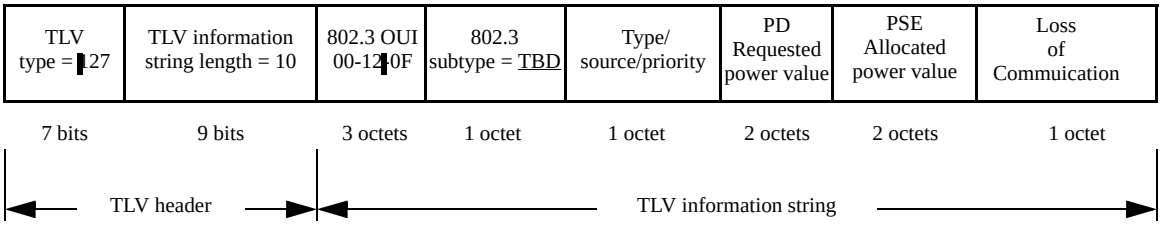

Figure 33–2—DTE Power via MDI classification TLV format

The information supplied by the Power Via MDI TLV defined in IEEE Std 802.1AB™ Annex G.3 is superseded by the DTE Power via MDI classification TLV. Based on this, in order to conserve LLDPDU space, when the DTE Power via MDI classification TLV is being transmitted, the Power via MDI TLV shall not be transmitted.

33.7.2.1 Requested power type/source/priority

The power type/source/priority field shall contain a bit-map of the power type, source and priority defined in Table 33–1.

Table 33–1—Power type/source/priority field

Bit	Function	Value/meaning
7:6	power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	power source	Where power type = PD 5 4 1 1 = PSE and local 1 0 = Local 0 1 = PSE 0 0 = Unknown Where power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3:2	Reserved	Reserved
1:0	power priority	1 0 1 1 = low 1 0 = high 0 1 = critical 0 0 = unknown (default)

33.7.2.1.1 Power type

This field shall be set to 01 for a PD (see 33.3) and 00 for a PSE (see 33.2).

33.7.2.1.2 Power source

When the power type is PD, this field shall be set to 01 when the PD is being powered only through the PI; to 10 when the PD is being powered only from a local supply; to 11 when the PD is being powered from both; and to 00 when this information is not available.

When the power type is PSE, this field shall be set to 01 when the PSE is sourcing its power through the PI from its primary supply; to 10 when the PSE is sourcing its power through the PI from a backup source; and to 00 when this information is not available.

33.7.2.1.3 Power priority

When the power type is PD, this field shall be set to the power priority configured for the device. If a PD is unable to determine its power priority or it has not been configured, then this field shall be set to 00.

When the power type is PSE, this field shall be set to 00.

33.7.2.2 Requested PD power value

The requested power value field shall contain the PD's requested power value defined in Table 33–2.

Table 33–2—Power value field

Bit	Function	Value/meaning
15:0	PD power value	Power = 0.1 × (decimal value of bits) Watts. Valid values for these bits are decimal 0 through 295.

The PD power value is encoded according to the following formula:

$$\{Power = (0.1 \times X)\}_{\text{Watts}} \quad (0–1)$$

where

Power is the effective requested PD power value
X is the decimal value of the power value field, bits 15:0

This power is always the power at the input of the PD's PI, and so does not include channel losses. ~~In the case of a PSE, this power is the power at the output of the PSE's PI~~. The PSE is therefore responsible for estimating and including channel loss when calculating the PSE allocated port power value.

~~If accepted by the PSE, the requested PD power value for a PD is the new maximum input average power (see 33.3.7.2) the PD will ever draw under this power allocation. If accepted by the PD, the PD requested power value for a PSE is the new maximum input average power it wants the PD to ever draw under this power allocation.~~

~~33.7.2.3 Actual power type/source/priority~~

~~The actual power type/source/priority field shall contain a bit-map of the actual power type, source, and priority defined in Table 33–1.~~

~~33.7.2.4 Actual PD power value~~

~~The PD actual power value field shall contain the current actual PD power value defined in Table 33–2.~~

~~The actual PD power value for a PD is the maximum input average power (see 33.3.7.2) the PD will ever draw under the current power allocation. The actual PD power value for a PSE is the maximum input average power the PD may ever draw under the current power allocation.~~

33.7.2.5 Loss of Communication

The Loss of Communcation field shall contain a value to indicate that the device believes it has lost communication with the far end. The encoding of this field is defined in Table 33–3.

Table 33–3—Loss of Communication field

Bit	Function	Value/meaning
7:1	reserved	reserved
0		1 = loss of communications 0 = communication OK (default)

33.7.3 DTE Power via MDI classification TLV to ~~local~~ PSE object class cross references

The cross references between the DTE power via MDI classification TLV and the DTE Power via MDI classification local object class (30.9.1) attributes are listed in Table 33–4.

Table 33–4—DTE power via MDI classification TLV to PSE object class cross references

TLV name	TLV variable	Attribute
DTE power via MDI classification	power type	aDLLPowerType
	power Source	aDLLPowerSource
	power priority	RESERVED
	PD Requested power value	aMirroredDLLPDRequestedPowerValue
	PSE Allocated power value	aDLLPSEAllocatedPowerValue
	Loss of Communication	aLostCommunication

33.7.4 DTE Power via MDI classification TLV to remote object class cross references

The cross references between the DTE power via MDI classification TLV and the DTE Power via MDI classification PD object class (30.9.2) attributes are listed in Table 33–5.

Table 33–5—DTE power via MDI classification TLV to PD object cross references

TLV name	TLV variable	Clause 30 attribute
DTE power via MDI classification	power type	aDLLPowerType
	power Source	aDLLPowerSource
	power priority	aDLLPDPowerPriority
	PD Requested power value	aDLLPDRequestedPowerValue
	PSE Allocated power value	aMirroredDLLPSEAllocatedPowerValue
	Loss of Communication	aLostCommunication

33.7.5 Data Link Layer classification timing requirements

An LLDPDU containing a DTE Power via MDI classification TLV shall be sent within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled, or in a PSE as indicated by the variable pse_dll_enabled. See 33.2.4.4, 33.3.3.3, 33.7.6.2.

An LLDPDU containing a DTE Power via MDI classification TLV with the Acknowledge field set to either “acknowledge” or “non-acknowledge” shall be sent within 5 minutes of an LLDPDU containing a DTE Power via MDI classification TLV being received with the Requested power value field not equal to the Actual power value field.

An LLDPDU containing a DTE Power via MDI classification TLV with the Acknowledge field set to “not part of acknowledge cycle” shall be sent within 5 minutes of an LLDPDU containing a DTE Power via MDI classification TLV~~ with the Acknowledge field set to either “acknowledge” or “non-acknowledge.”~~

33.7.6 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively. PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–3. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–4.

33.7.6.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.7.6.2 Variables

The PSE power control state diagram (Figure 33–3) and PD power control state diagram (Figure 33–4) use the following variables:

~~locAcknowledge~~

~~Indicates the response of the local system to the remote system's last change in requested power value. This variable is mapped to the aLLDPPoEPLocAcknowledge attribute (30.12.1.1.10).~~

~~Values: LOSS: The local system has detected a loss of communication. This value maps to the enumeration "loss of communications."~~

~~NACK: The local system has not accepted the requested change to the allocated power. This value maps to the enumeration "non-acknowledge."~~

~~ACK: The local system has accepted the requested change to the allocated power. This value maps to the enumeration "acknowledge."~~

~~NULL: There is no requested change to the allocated power. This value maps to the enumeration "not part of acknowledge cycle."~~

~~locActualPowerValue~~

~~Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.7.2) the PD will ever draw under the current power allocation. The actual PD power value for a PSE is the maximum input average power the PD may ever draw under the current power allocation. The PD power value is encoded according to Equation (0–1), where *X* is the decimal value of locActualPowerValue. This variable is mapped to the aLLDPPoEPLocActualPDPowerValue attribute (30.12.1.1.9).~~

Values: 0 through 295.

local_system_change

An implementation specific control variable that indicates that the local system wants to change the locRequestedPowerValue.

Values: FALSE: The local system does not wants to change the locRequestedPowerValue.
TRUE: The local system wants to change the locRequestedPowerValue.

~~locRequestedPowerValue~~

~~Integer that indicates the requested PD power value of the local system. The requested PD power value for a PD is the new maximum input average power (see 33.3.7.2) the PD will ever draw under this power allocation if it is accepted. The PD requested power value for a PSE is the new maximum input average power it wants the PD to ever draw under this power allocation if it is accepted. The PD power value is encoded according to Equation (0–1), where *X* is the decimal value of locRequestedPowerValue. This variable is mapped to the aLLDPPoEPLocRequestedPDPowerValue attribute (30.12.1.1.5).~~

~~Values: 0 through 295~~

PDRequestedPowerValue

Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.7.2) the PD requests. The PD power value is encoded according to Equation (0–1), where *X* is the decimal value of PDRequestedPowerValue. This variable is mapped from the aDLLPDRequestedPowerValue attribute (30.9.2.1.7).

Values: 0 through 295.

MirroredPDRequestedPowerValue

The copy of PDRequestedPowerValue that the PSE has. The definition is the same as that of PDRequestedPowerValue. This variable is mapped from the aMirroredDLLPDRequestedPowerValue attribute (30.9.1.1.17).

Values: 0 through 295.

PSEAllocatedPowerValue

Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.7.2) the PD will ever draw. The power value for a PSE is the maximum input average power the PD may ever draw. The PD power value is encoded according to Equation (0–1), where *X* is the decimal value of PSEAllocatedPowerValue. This variable is mapped from the aDLLPSEAllocatedPowerValue attribute (30.9.1.1.18).

Values: 0 through 295.

MirroredPSEAllocatedPowerValue

The copy of PSEAllocatedPowerValue that the PD has. The definition is the same as that of PSEAllocatedPowerValue. This variable is mapped from the aMirroredDLLPSEAllocatedPowerValue attribute (30.9.2.1.8).

Values: 0 through 295.

PSE_INITIAL_VALUE: This value is derived from the mr_pd_class_detected variable output by the PSE state diagram (Figure 33–1) as follows:

class_num_events	mr_pd_class_detected	PSE_INITIAL_VALUE
1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	0	130
2	1	39
2	2	65
2	3	130
2	4	255

PD_INITIAL_VALUE: This value is derived from the mr_pd_class_detected variable of the PD state diagram (Figure 33–4) as follows:

pse_power_type	pd_max_power	PD_INITIAL_VALUE
1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	0	130
2	1	39
2	2	65
2	3	130
2	4	255

PSE_NEW_VALUE; This is the new value of power that the PSE allocates to the PD.

PD_NEW_VALUE; This is the new value of power that the PD wants to request of the PSE.

loss_of_comms

Indicates if a loss of management frame communication defined in 33.8 has occurred.

Values: FALSE: A loss of communications defined in 33.8 has not occurred.
TRUE: A loss of communications defined in 33.8 has occurred.

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–4) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values: FALSE: PD Data Link Layer classification is not enabled.
TRUE: PD Data Link Layer classification is enabled.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–1) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values: FALSE: PSE Data Link Layer classification is not enabled.
TRUE: PSE Data Link Layer classification is enabled.

pse_power_cycles

Indicates whether the PSE performs power cycling after a loss of management frame communication (see 33.8).

Values: FALSE: PSE does not power cycle after loss of communications defined in 33.8.
TRUE: PSE does power cycle after loss of communications defined in 33.8.

~~remAcknowledge~~

~~Indicates the response from the remote system to the local systems last change in requested power value. This variable is mapped from the aLLDPPoEPRemAcknowledge attribute (30.12.2.1.10).~~

~~Values:~~ ~~LOSS:~~ ~~The remote system has detected a loss of communication. This value maps from the enumeration "loss of communications."~~
~~NACK:~~ ~~The remote system has not accepted the requested change to the allocated power. This value maps from the enumeration "non-acknowledge."~~
~~ACK:~~ ~~The remote system has accepted the requested change to the allocated power. This value maps from the enumeration "acknowledge."~~
~~NULL:~~ ~~There is no requested change to the allocated power. This value maps from the enumeration "not part of acknowledge cycle."~~

removePower

Indicates if the PSE is removing power from the PD ~~by setting the PSE state diagram variable pse_reset to TRUE~~ due to a detected a loss of communications with the PD.

Values: FALSE: Power should not be removed from PD.
TRUE: Power to be removed by PSE~~, pse_reset set to TRUE.~~

A summary cross references between the DTE Power via MDI classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in Table 33–27.

Table 33–6—Attribute to state diagram variable cross-reference

Object	Attribute	Mapping	State diagram variable
oPSE managed object class	aMirroredDLLPDRequestedPowerValue	⇐	MirroredPDRequested-PowerValue
	aDLLPSEAllocatedPowerValue	⇒	PSEAllocatedPower-Value
	aMirroredLostCommunication	⇒	loss_of_comms
oPD managed object class	aDLLPDRequestedPowerValue	⇒	PDRequestedPower-Value
	aMirroredDLLPSEAllocatedPowerValue	⇒	MirroredPSEAllocat-edPowerValue
	aLostCommunication	⇐	loss_of_comms

33.7.6.3 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. ~~A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.~~

~~pd_denial_timer~~
~~A timer used to limit when a PD can make a new request to change the allocated power after a request is denied. The timer is done when it reaches 1 second.~~

~~pse_denial_timer~~
~~A timer used to limit when a PSE can make a new request to change the allocated power after a request is denied. The timer is done when it reaches 1 second.~~

power_change_timer
A timer that is started once a PSE reallocates the power for the PD. It may be used by the PSE system.

33.7.6.4 Functions

examine_request
This function evaluates the request from the remote system to change the allocated power. This function returns the following variables:
change_accept:
Values: TRUE: The requested change to the allocated power is accepted
FALSE: The requested change to the allocated power is not accepted

33.7.6.5 State diagrams

The general state change procedure for PSEs is shown in Figure 33–3.

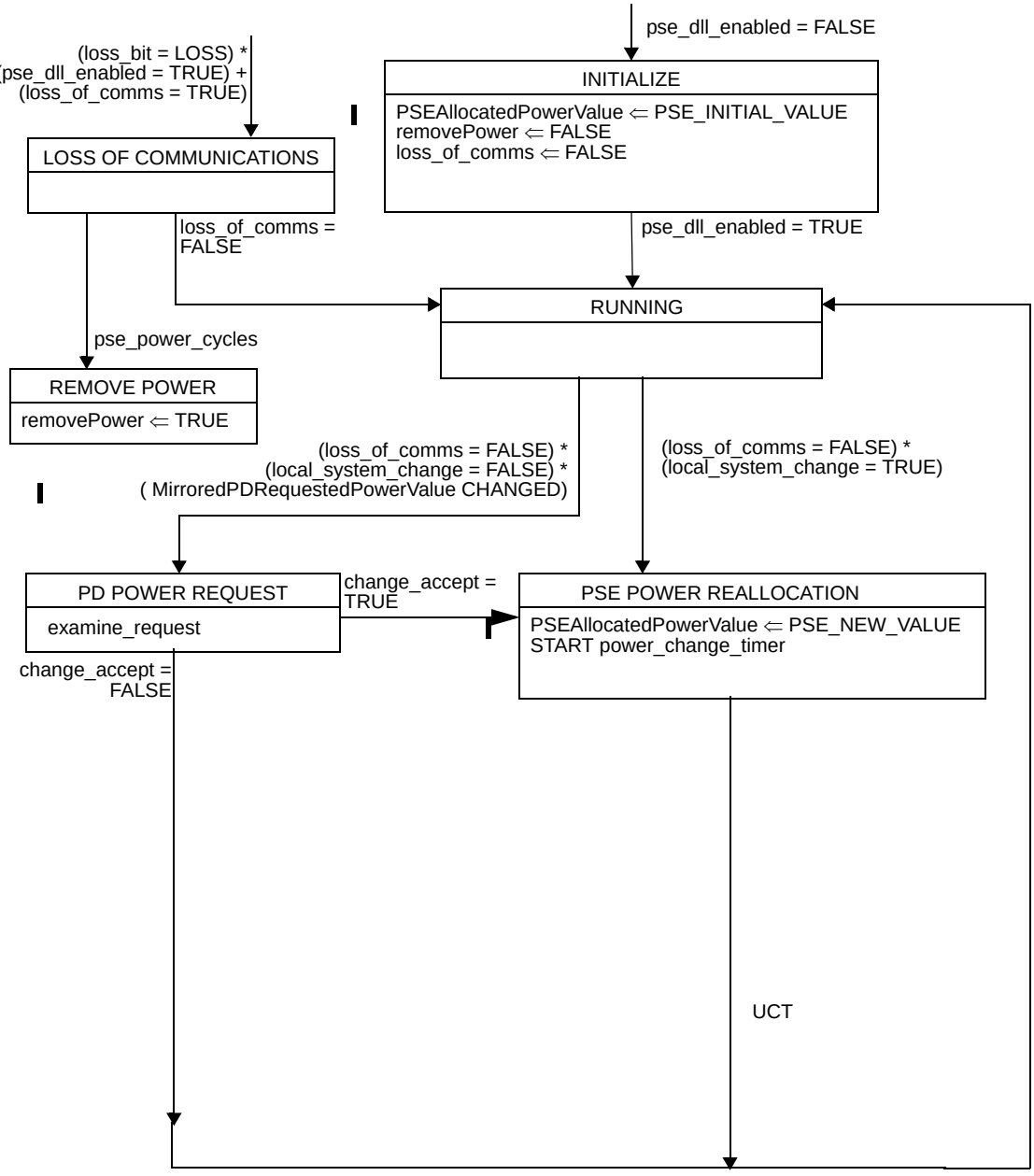

Figure 33–3—PSE power control state diagram

The general state change procedure for PDs is shown in Figure 33–4.

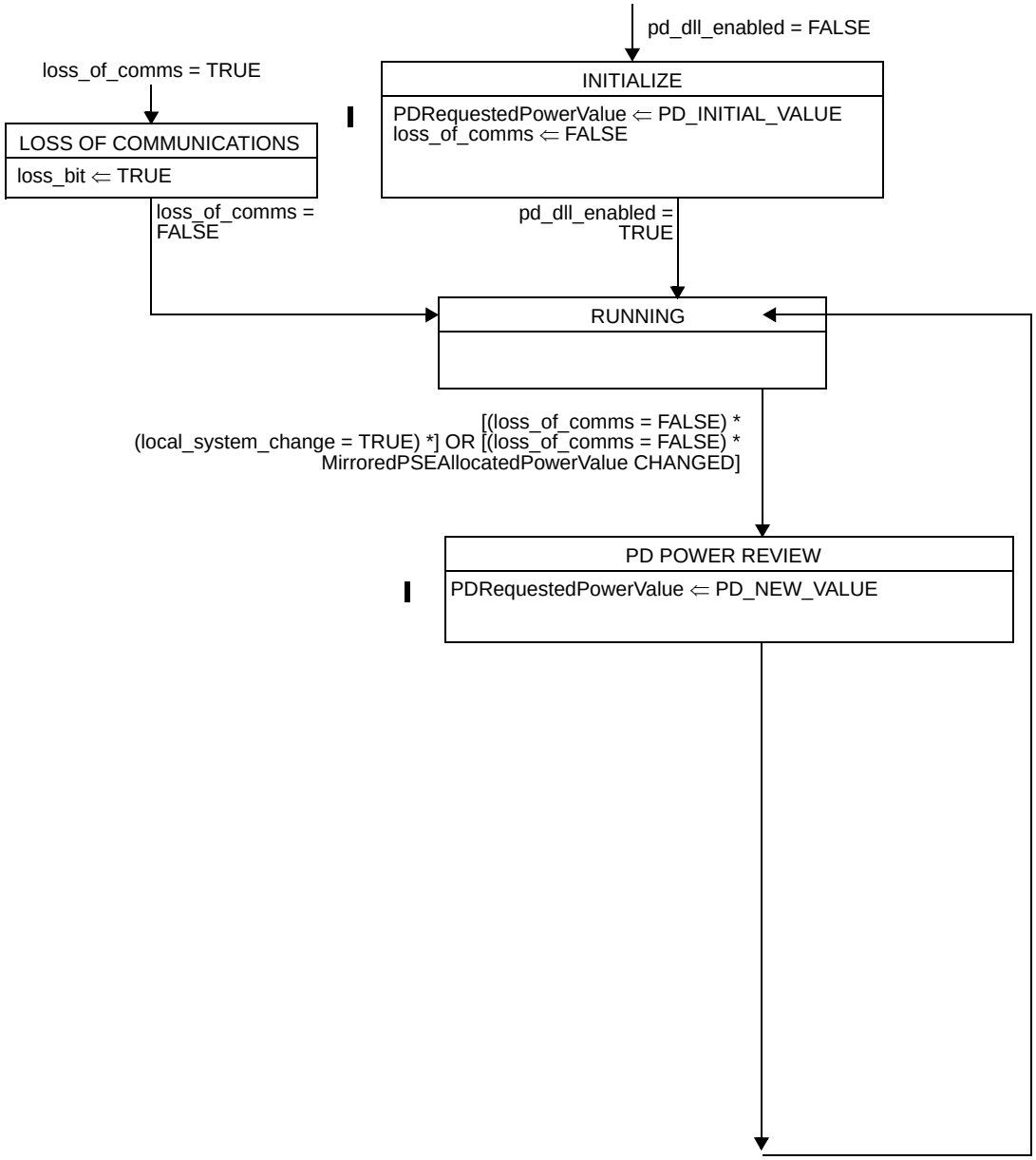

Figure 33–4—PD power control state diagram

33.7.7 State change procedure across a link

The PSE and PD utilize the LLDP mechanism to advertise their various attributes to the other entity.

The PD may request a new power value through the aDLLPDRequestedPowerValue (30.9.2.1.7) attribute in the DTE Power via MDI classification PD object class. The request appears to the PSE as a change to the aMirroredDLLPDRequestedPowerValue (30.9.1.1.17) attribute in the DTE Power via MDI classification PSE object class.

The PSE responds to a PD's request or arbitrarily reallocates the PD's power classification through the aDLLPSEAllocatedPowerValue (30.9.1.1.18) attribute in the DTE Power via MDI classification PSE object

class. This appears to the PD as a change to the aMirroredDLLPSEAllocatedPowerValue (30.9.2.1.8) attribute in the DTE Power via MDI classification PD object class.

The state machines describe the behaviour above.

33.7.7.1 PSE State change procedure across a link

During normal operation the PSE machine is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters the PSE POWER REALLOCATION state in the machine, which causes the PSEAllocatedPowerValue to be updated to the new level the PSE would like to assign indicated by the PSE_NEW VALUE. The machine then returns to the RUNNING state.

If the PSE machine sees a change to the previously stored MirroredPDRequestedPowerValue, it recognizes a request by the PD to change its power allocation. The PSE examines the request by entering into the PD POWER REQUEST state. The PSE may decide to ignore the request, in which case it returns to the RUNNING state or it may decide to change the PD allocation by entering the PSE POWER REALLOCATION state and behaves as described above.

When the PSE enters the PSE POWER REALLOCATION state it also re-starts a timer that may be used by the higher layer control function. For example, it may wait to see if the PD changes its request based on the reallocation. The use of the timer is outside the scope of this standard.

At any time, if the conditions of a loss of communication are met, the PSE enters the LOSS OF COMMUNICATIONS state.

33.7.7.2 PD State change procedure across a link

During normal operation the PD machine is in the RUNNING state. If the PD machine sees a change to the previously stored MirroredPSEAllocatedPowerValue, it recognizes a command by the PD to change its power allocation. Consequently, the PD enters the PSE POWER REALLOCATION state in the machine, which causes the PDRequestedPowerValue to also be updated to the new MirroredPSEAllocatedPowerValue. The machine then returns to the RUNNING state.

If the PD machine wants to initiate a request in its allocation, the local_system_change is asserted and the PD enters the PD POWER REQUEST state in the machine, which causes the PDRequestedAPowerValue to be updated to the new level the PD would like indicated by the PD_NEW VALUE. The machine then returns to the RUNNING state.

At any time, if the conditions of a loss of communication are met, the PD enters the LOSS OF COMMUNICATIONS state.

~~If the local device is in the running state and the remote device changes to the request state, the local device observes the remote device's requested power through the aLLDPPoEPRemRequestedPDPowerValue (30.12.2.1.5) attribute in the DTE Power via MDI classification remote object class. The local device changes to an acknowledge state or a non-acknowledge state depending on acceptance of the remote device's requested change.~~

~~If the local device changes to the acknowledge state, it then changes the aLLDPPoEPLocActualPDPowerValue (30.12.1.1.9) attribute in the DTE Power via MDI classification local object class to match the remote device's requested power. The local device then sends a PDU reflecting its new settings.~~

~~If the local device is in the running state and it wishes to change to a new power mode, it may only do so if the remote device's most recent PDU reported that the remote device is in the running state. To change to a~~

~~new power mode, the local device sets its local requestedPower object and changes to the requesting state. The local device then sends a PDU reflecting its requested power mode.~~

~~If the remote device changes to the acknowledge state in response to the mode change request from the local device, the local device updates its local actual power objects and changes to the running state. The local device then sends a PDU reflecting its new settings.~~

~~If the remote device changes to the non-acknowledge state in response to the mode change request from the local device, the local device does not change its operating power mode and changes back to the running state. The local device then sends a PDU reflecting its return to the running state.~~

~~In the event of a PDU collision (e.g., the local device is in a requesting state and the remote device changes to a requesting state), the local device does not change its operating power mode. The local device instead changes back to the running state and sends a PDU reflecting its return to the running state. If the local device is a PSE it may restart the request to change after pse_denial_timer, if the local device is a PD it may restart the request to change after pd_denial_timer (see 33.7.6.3).~~

~~State definitions require that each request must be acknowledged or denied before returning to running state. The requestor does not deassert the request until it receives an acknowledge or non-acknowledge. The partner responds to a request as soon as it is seen. The requestor may persist or vacillate after a non-acknowledge. To persist, it reasserts its request after a 1 second delay. It may decide to not persist.~~

33.7.8 Sample exchange

33.8 Loss of management frame communication

There are three scenarios which may cause a loss in management frame communication:

1) Management frame communication not established after power-on, resulting in systems using the power values established with Physical Layer classification
2) Loss in management frame communication, resulting in systems reverting to last ~~acknowledged~~ Data Link Layer classification power value
3) Loss in management frame communication or communication not established after power-on, resulting in PSE optionally power cycling the PD after 2 × TTL timeout value time period

If Data Link Layer classification fails to come up within 5 minutes after the PSE has turned on power to the PD and the PSE identified the PD as a Type 2 PD via Physical Layer classification, the PSE may remove power.

Upon loss of management frame communication, PSEs and PDs shall remain operational using the last ~~acknowledged~~ classification state.

If a loss of management frame communication persists past the LLDP time to live (TTL) timeout value for the remote system (see IEEE Std 802.1AB-200X, subclause 9.5.4) plus an additional delay of 2 × TTL timeout value for the remote system, a PSE may remove power, a PD shall update aLostCommunication (30.9.1.1.19) attribute in the DTE Power via MDI classification PD object class to the enumeration “loss of communications.”

The PSE may remove power at any time per Figure 33–1.

33.9 Protocol implementation conformance statement (PICS) proforma for Clause 33, DTE Power via MDI[1]

33.9.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 33, DTE Power via MDI, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.9.2 Identification

33.9.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
1—Required for all implementations 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

33.9.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2005, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2005.)	
Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

33.9.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDCL	PD Classification	33.3.4	PD supports classification	O	Yes [ ] No [ ]

33.9.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*CL	Implementation supports classification	33.2.8	Optional	O	Yes [ ] No [ ]
*END	Endpoint PSE	33.2.1	PSE implemented as an endpoint device	O/1	Yes [ ] No [ ]
*ENDA	Alternative A Endpoint PSE	33.2.1	PSE implements Alternative A	END:O.2	Yes [ ] No [ ]
*ENDB	Alternative B Endpoint PSE	33.2.1	PSE implements Alternative B	END:O.2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.6	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a mid-span device	O/1	Yes [ ] No [ ]
*PA	Power Allocation	33.2.10	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability—PSE supports the option to control which PSE Pinout is used	33.6.1.1.4	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.11.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.11.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

33.9.3 PICS proforma tables for DTE Power via MDI

33.9.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility considerations.	33.1.2	PDs and PSEs compatible at their PIs.	M	Yes [ ]

33.9.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	Alternative B	33.2.1	Only implementation allowed for Midspan	MID:M	Yes [ ] N/A [ ]
PSE3	Alternative A and Alternative B	33.2.3	Not operate on same link segment simultaneously	END:M	Yes [ ] N/A [ ]
PSE4	PSE behavior	33.2.4	In accordance with state diagrams shown in Figure 33–1 and Figure 33–3	M	Yes [ ]
PSE5	Detection, classification, and turn on timing	33.2.4.1	In accordance with Table 33–9	M	Yes [ ]
PSE6	Turn on power	33.2.3.1	After valid detection in less than T_{pon}	M	Yes [ ]
PSE7	Not apply power within T_{pon}	33.2.4.1	Must initiate and successfully complete a new detection cycle before applying power	M	Yes [ ]
PSE8	Alternative B backoff cycle	33.2.4.1	Must wait no less than T_{dbo} as specified in Table 33–9 before attempting another detection	M	Yes [ ]
PSE9	Backoff voltage	33.2.4.1	Not greater than 2.8 Vdc	M	Yes [ ]
PSE10	Applying power	33.3	Not until a PD requesting power has been successfully detected	M	Yes [ ]
PSE11	Power pairs	33.3	Power must be supplied on the same pairs as those used for detection	M	Yes [ ]
PSE12	Detecting PDs	33.2.6	Performed via the PSE PI	M	Yes [ ]
PSE13	Open circuit voltage	33.2.6	Item 1 in Table 33–4	M	Yes [ ]
PSE14	Short circuit current	33.2.6	Item 2 in Table 33–4	M	Yes [ ]
PSE15	Backdriven current	33.2.6	Not be damaged by up to 5 mA over the range of Vport	M	Yes [ ]
PSE16	Output capacitance	33.2.6	Item 18 in Table 33–9	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE17	Exhibit Thevenin equivalence to one of the detection circuits in all detection states	33.2.5	Figure 33–12 or Figure 33–13	M	Yes [ ]
PSE18	V_{detect} with a valid PD signature connected	33.2.5.1	Item 3 in Table 33–4	M	Yes [ ]
PSE19	Two measurements with V_{detect}	33.2.5.1	At least 1 V difference between consecutive measurements	M	Yes [ ]
PSE20	Control slew rate when switching detection voltages	33.2.5.1	Item 6 in Table 33–4	M	Yes [ ]
PSE21	Polarity of $V_{detect.}$	33.2.5.1	Match polarity of V_{Port} defined in 33.2.1	M	Yes [ ]
PSE22	Probe link to detect all PDs which present a valid signature	33.2.6.1	(19 kΩ to 26.5 kΩ DC resistance) and (120 nF capacitance or less) and (Voltage offset of up to 2.0 V DC) and (Current offset of up to 12 μA)	M	Yes [ ]
PSE23	Reject PDs that present an invalid signature	33.2.6.2	(Less than 15 kΩ DC resistance) or (More than 33 kΩ DC resistance) or (More than 10μF capacitive load)	M	Yes [ ]
PSE24	Default classification	33.2.7	Assign to Class 0 if PD cannot be classified as Class 1, 2, 3, or 4	M	Yes [ ]
PSE25	Classification power levels	33.2.7.1	PDs classified as Class 4 will be treated as Class 0	M	Yes [ ]
PSE26	Provide V_{Class}	33.2.7.2	Between 15.5 and 20.5 V, limited to 100 mA or less at the PI	CL:M	Yes [ ] N/A [ ]
PSE27	Classification polarity	33.2.7.2	Same as V_{Port}	CL:M	Yes [ ] N/A [ ]
PSE28	Classification timing	33.2.7.2	Item 20 in Table 33–9	CL:M	Yes [ ] N/A [ ]
PSE29	Measure I_{Class}	33.2.7.2	Classify PD according to Table 33–7	CL:M	Yes [ ] N/A [ ]
PSE30	Classification default	33.2.7.2	Assign PD to Class 0 if I_{class} is greater than or equal to 51 mA	CL:M	Yes [ ] N/A [ ]
PSE31	Power supply output	33.2.8	Provide power to the PI according to Table 33–9, Figure 33–1, and Figure 33–3	M	Yes [ ]
PSE32	Output voltage	33.2.8.1	The specification for V_{Port} includes line and temperature variations	M	Yes [ ]
PSE33	V_{Port} measurement	33.2.8.1	Measured between any conductor of one power pair and any conductor of the other power pair	M	Yes [ ]
PSE34	Load regulation	33.2.8.2	Specified as 0.44 W to 15.4 W load step at a rate of change of 35 mA/μs max	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE35	Voltage transients	33.2.8.2	Limited to 3.5 V/μs max	M	Yes [ ]
PSE36	Power feeding ripple and noise	33.2.8.3	Met for common-mode and/or pair-to-pair noise values for power outputs from 0.44 W to 15.4 W at operating V_{Port}	M	Yes [ ]
PSE37	Maximum current at minimum voltage	33.2.8.4	For V_{Port} > 44V, the minimum value for I_{Port_max} in Table 33–9 shall be 15.4 W/V_{Port}	M	Yes [ ]
PSE38	AC current waveform parameters	33.2.8.4	I_{Peak} = 0.4A minimum for 50ms minimum and 5% duty cycle minimum For V_{Port} > 44 V, I_{Peak} = 17.6 W/ V_{Port}	M	Yes [ ]
PSE39	Specifications for I_{Inrush} current	33.2.8.5	Meet conditions specified in 33.2.9.6 items a) through e)	M	Yes [ ]
PSE40	Overload current detection range	33.2.8.6	If $I_{Port\_MPS} > I_{CUT}$ for $T > T_{ovld}$ the PSE shall remove power. Item 8 in Table 33–9	M	Yes [ ]
PSE41	Overload time limit	33.2.8.7	Item 9 in Table 33–9	M	Yes [ ]
PSE42	Short circuit current	33.2.8.8	Item 10 in Table 33–9	M	Yes [ ]
PSE43	Short circuit time limit	33.2.8.9	Item 11 in Table 33–9	M	Yes [ ]
PSE44	Turn off time	33.2.8.10	Applies to the discharge time from V_{Port} to 2.8Vdc with a test resistor of 320kΩ attached to the PI	M	Yes [ ]
PSE45	Turn off voltage	33.2.8.11	Applies to the PI voltage in the IDLE State	M	Yes [ ]
PSE46	Current unbalance	33.2.8.12	Item 15 in Table 33–9.	M	Yes [ ]
PSE47	Power turn on time	33.2.8.13	Item 16 in Table 33–9.	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE48	Power provision	33.2.9	Do not initiate if PSE is unable to provide maximum power level requested by PD based on PD's classification	PA:M	Yes [ ] N/A [ ]
PSE49	Power allocation	33.2.9	Not be based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]
PSE50	PSE AC MPS component requirements	33.2.10.1.1	Meet requirements specified in item 1 and item 3 in Table 33–10	AC:M	Yes [ ] N/A [ ]
PSE51	PSE AC MPS component present	33.2.10.1.1	Meets requirements specified in item 4a in Table 33–10	AC:M	Yes [ ] N/A [ ]
PSE52	PSE AC MPS component absent	33.2.10.1.1	Meets requirements specified in item 4b in Table 33–10	AC:M	Yes [ ] N/A [ ]
PSE53	Power removal	33.2.10.1.1	When AC MPS has been absent for a time duration greater than T_{PMDO}	AC:M	Yes [ ] N/A [ ]
PSE54	PSE DC MPS component present	33.2.10.1.2	Meet requirements specified in item 6 and item 7b in Table 33–9	DC:M	Yes [ ] N/A [ ]
PSE55	PSE DC MPS component absent	33.2.10.1.2	Meet requirements specified in item 6 in Table 33–9	DC:M	Yes [ ] N/A [ ]
PSE56	Power removal	33.2.10.1.2	When DC MPS has been absent for a time duration greater than T_{PMDO}	DC:M	Yes [ ] N/A [ ]
PSE57	Not remove power	33.2.10.1.2	When the DC current is greater than or equal to I_{Min2} max for at least T_{MPS} every $T_{MPS} + T_{MPDO}$, as defined in Table 33–9	DC:M	Yes [ ] N/A [ ]

33.9.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	33.3.1	On either set of PI conductors	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–11	M	Yes [ ]
PD3	Source power	33.3.1	The PD will not source power on its PI	M	Yes [ ]
PD4	Voltage tolerance	33.3.1	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]
PD5	PD behavior	33.3.2	According to state diagram shown in Figure 33–13	M	Yes [ ]
PD6	Valid detection signature	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the PI	M	Yes [ ]
PD7	Non-valid detection signature	33.3.3	Presented on each set of pairs defined in 33.3.1 if not powered via the PI and will not accept power via the PI	M	Yes [ ]
PD8	Non-valid detection signature	33.3.3	When powered, present an invalid signature on the set of pairs not drawing power	M	Yes [ ]
PD9	Valid detection signature	33.3.3	Characteristics defined in Table 33–12	M	Yes [ ]
PD10	Non-valid detection signature.	33.3.3	Exhibit one or both of the characteristics described in Table 33–13	M	Yes [ ]
PD11	Return Class 0 to 3 classification	33.3.4	Implement classification selection according to maximum power draw specified in Table 33–14	PDCL:M	Yes [ ] N/A [ ]
PD12	Classification signature	33.3.4	As defined in Table 33–15	PDCL:M	Yes [ ] N/A [ ]
PD13	Classification signature	33.3.4	One classification signature during classification	PDCL:M	Yes [ ] N/A [ ]
PD14	PD power supply	33.3.5	Operate within the characteristics in Table 33–17	M	Yes [ ]
PD15	PD turn on voltage	33.3.5.1	PD will turn on at a voltage less than V_{On}.	M	Yes [ ]
PD16	PD stay on voltage	33.3.5.1	Must stay on for all voltages in the range of V_{Port}	M	Yes [ ]
PD17	PD turn off voltage	33.3.5.1	Must turn off at a voltage less than V_{Port} minimum and greater than V_{Off}	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD18	Input average power	33.3.5.2	Applies for input power as specified in Table 33–17 averaged over one second	M	Yes [ ]
PD19	Input inrush current	33.3.5.3	Limited by the PD if C_{port} is greater than or equal to 180 μF so that I_{Inrush} max is satisfied.	M	Yes [ ]
PD20	Peak operating current	33.3.5.4	Not to exceed P_{Port} max/V_{Port} for more than 50ms max and 5% duty cycle max	M	Yes [ ]
PD21	Peak current	33.3.5.4	Not to exceed I_{Port} max	M	Yes [ ]
PD22	RMS, DC, and ripple current	33.3.5.4	Bounded by $Irms = [(Idc)^2 + (Iac)^2]^{1/2}$.	M	Yes [ ]
PD23	Maximum operating DC and RMS current	33.3.5.4	Defined by the following equation: I_{Port_max} [mA] =12950/ V_{Port}	M	Yes [ ]
PD24	PI capacitance during normal powering mode	33.3.5.5	As specified in subclause 33.3.7.6	M	Yes [ ]
PD25	Ripple and noise	33.3.5.6	As specified in Table 33–17 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD26	Ripple and noise specification	33.3.5.6	For all operating voltages in the range defined by Table 33–17 item 1	M	Yes [ ]
PD27	Ripple and noise presence	33.3.5.6	Must operate correctly when connected to a PSE generating ripple and noise levels specified in Table 33–9 item 3	M	Yes [ ]
PD28	Power supply turn on/turn off voltages	33.3.5.7	As specified in Table 33–17 when connected to a PSE through a 20 Ω series resistor.	M	Yes [ ]
PD29	Startup oscillations	33.3.5.7	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD30	Classification stability	33.3.5.8	Classification signature will remain valid within T_{class} and remain valid for the duration of the classification period	M	Yes [ ]
PD31	Backfeed voltage	33.3.5.10	Mode A and Mode B per 33.3.7.10	M	Yes [ ]
PD32	Maintain power signature	33.3.6	(current draw) and (AC impedance) defined in Table 33–18	M	Yes [ ]
PD33	No longer require power	33.3.6	Remove both components of the Maintain power signature	M	Yes [ ]

33.9.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Electrical isolation	33.4.1	Isolation between all accessible external conductors and all MDI leads including those not used by the PD or PSE.	M	Yes [ ]
EL2	Strength tests for electrical isolation	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1	M	Yes [ ]
EL3	Isolation and grounding requirements	33.4.1	Conductive link segments that have different requirements must have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL4	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL5	Environment A requirement	33.4.1.1.1	Switch more negative conductor	M	Yes [ ]
EL6	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	M	Yes [ ]
EL7	Fault tolerance for PSEs and PDs encompassed within the MDI	33.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL8	Fault tolerance for PSEs and PDs not encompassed within an MDI	33.4.2	Meet the requirements of 33.4.2	M	Yes [ ]
EL9	Common-mode fault tolerance	33.4.2	Each wire pair will withstand a 1000V common-mode impulse applied at *E*cm of either polarity without damage	M	Yes [ ]
EL10	The shape of the impulse for item common-mode fault tolerance	33.4.2	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of the half value)	M	Yes [ ]
EL11	Impedance balance for transmit and receive pairs	33.4.3	Exceed: – 29-17 log 10 (f/10)dB from 1.0 to 20MHz for 10Mb/s PHYs – 34-19.2 log 10 (f/50)dB from 1.0 MHz to 100 MHz for 100Mbits/s or greater PHYs	M	Yes [ ]
EL12	Common-mode output voltage	33.4.4	Magnitude while transmitting data and with power applied will not exceed 50 mV peak when operating at 10Mbits/s and 50 mV peak-to-peak when operating at 100 Mbits/s or greater	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL13	Common-mode AC voltage	33.4.4	Magnitude at all other ports will not exceed 50 mV peak-to-peak	M	Yes [ ]
EL14	Frequency range for common-mode AC voltage measurement	33.4.4	At all other ports will be from 1 MHz to 100 MHz	M	Yes [ ]
EL15	Common-mode output voltage test configuration	33.4.4	Must be performed with the PHY transmitting data and an operating PSE or PD and with the PSE load or PD source requirements specified in 33.4.4 items 1) or 2)	M	Yes [ ]
EL16	Noise from an operating PSE or PD to the differential transmit and receive pairs	33.4.6	Will not exceed 10 mV peak-to-peak measured from 1MHz to 100 MHz	M	Yes [ ]
EL17	Differential noise voltage test setup	33.4.6	The PSE and PD shall be terminated as illustrated in Figure 33–22 and tested with the PSE and PD conditions as specified in 33.4.4	M	Yes [ ]
EL18	Return loss requirements	33.4.7	Specified in 14.3.1.3.4 for a 10Mb/s PHY, in ANSI X3.263:1995 for a 100Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY	M	Yes [ ]

33.9.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	PSE electrical isolation	33.4.1	Provided between port device circuits, frame ground and PI leads	M	Yes [ ]
PSEEL2	Short circuit fault tolerance	33.4.2	Any wire pair will withstand any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL3	Magnitude of short circuit current	33.4.2	Not to exceed maximum value of $I_{LIM.}$	M	Yes [ ]
PSEEL4	Limitation of electromagnetic interferenc.	33.4.5	PSE will comply with applicable local and national codes	M	Yes [ ]
PSEEL5	Insertion of Midspan at FD	33.4.8	Comply with the guidelines specified in 33.4.8 items a) and b)	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”	33.4.8	Installation of a Midspan PSE will not increase the length to more than 100 m as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL7	Configurations with Midspan PSE	33.4.8	Must not alter transmission requirements of the "permanent link"	MID:M	Yes [ ] N/A [ ]
PSEEL8	Midspan PSE insertion in the channel	33.4.8	Must provide continuity for signal pairs	MID:M	Yes [ ] N/A [ ]
PSEEL9	Midspan continuity in non-data pairs	33.4.8	Will not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE inserted as a "Connector" or "Telecom outlet"	33.4.8.1	Meet transmission parameters NEXT, insertion loss and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE NEXT	33.4.8.1.1	$NEXT_{conn} \geq 40 - 20\log(f/100)$ dB [(Equation 33–5)] but not greater than 65 dB from from 1 MHz to 100 MHz.	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Insertion Loss	33.4.8.1.2	$Insertion\_loss_{conn} \leq 0.04 SQRT(f)$ dB [Equation (33–6)] but not less than 0.1 dB from from 1 MHz to 100 MHz.	MID:M	Yes [ ] N/A [ ]
PSEEL13	Midspan PSE Return Loss	33.4.8.1.3	1 MHz ≤ f < 20 MHz: 23dB 20 MHz ≤ f ≤ 100 MHz:14 dB (Table 33–19) for transmit and receive pairs	MID:M	Yes [ ] N/A [ ]
PSEEL14	Work area or equipment cable Midspan PSE	33.4.8.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 for insertion loss, NEXT, and return loss for all transmit and receive pairs	MID:M	Yes [ ] N/A [ ]

33.9.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD electrical isolation	33.4.1	Provided between all external conductors, including frame ground, and all PI leads	M	Yes [ ]
PDEL2	PD common-mode test requirement	33.4.4	The PIs that require power shall be terminated as illustrated in Figure 33–22	M	Yes [ ]

33.9.3.7 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.5.1	Conform to IEC publication 60950-1:2001	M	Yes [ ]
ES2	Safety	33.5.1	Comply with all applicable local and national codes	M	Yes [ ]
ES3	Telephony voltages	33.5.6	Application thereof described in 33.5.6 not result in any safety hazard	M	Yes [ ]
ES4	Limitation of electromagnetic interference	33.5.7	Comply with applicable local and national codes	M	Yes [ ]

33.9.3.8 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	33.5.1	Limited Power Source in accordance with IEC 60950-1:2001	M	Yes [ ]
PSEES2	Resistance unbalance	33.5.5	As specified in IEC 11801 Edition 2 Clause 6.4.8 (reference: 3 percent)	M	Yes [ ]

33.9.3.9 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability	33.6	Access via MII, GMII, or equivalent	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers	33.6.1	Register address 11 for control functions and register address 12 for status functions	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH)	33.6.1	Remain high until read via the management interface	MAN:M	Yes [ ] N/A [ ]
MF4	Register bits read	33.6.1	Bit assumes a value based on the current state of the condition it monitors	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:4)	33.6.1.1.1	Not affected by writes and return a value of zero when read	MAN:M	Yes [ ] N/A [ ]
MF6	Pair Control Ability not supported	33.6.1.1.2	Ignore writes to bits 11.3:2	MAN* !PCA:M	Yes [ ] N/A [ ]
MF7	Writes to 11.3:2 when Pair Control Ability not supported	33.6.1.1.2	Return the value that reports the supported PSE Pinout Alternative	MAN* !PCA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF8	Bits 11.3:2 set to '01'	33.6.1.1.2	Forces the PSE to use Alternative A	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF9	Bits 11.3:2 set to '10'	33.6.1.1.2	Forces the PSE to use Alternative B	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF10	Pair control ability bit, (12.0)	33.6.1.1.2	A value of ‘1’ sets the mr_pse_alternative variable	MAN∗ PCA:M	Yes [ ] N/A [ ]
MF11	PSE function disabled	33.6.1.1.3	Setting PSE Enable bits 11.1:0 to a logic ‘00’, also the MDI shall function as it would if it had no PSE function	MAN:M	Yes [ ] N/A [ ]
MF12	PSE function enabled	33.6.1.1.3	Setting PSE Enable bits 11.1:0 to a logic ‘01’	MAN:M	Yes [ ] N/A [ ]
MF13	PSE enable bits (11.1:0)	33.6.1.1.3	Writing to these register bits shall set mr_pse_enable to the corresponding value: ‘00’ = disable, ‘01’ = enable and ‘10’ = force power	MAN:M	Yes [ ] N/A [ ]
MF14	Reserved bits (12.15:13)	33.6.1.2.1	Not affected by writes and shall return a value of zero when read	MAN:M	Yes [ ] N/A [ ]
MF15	Power denied bit (12.12)	33.6.1.2.2	A value of ‘1’ indicates power has been denied	MAN:M	Yes [ ] N/A [ ]
MF16	Power denied bit implementation	33.6.1.2.2	Will be implemented with a latching high behavior as defined in 33.6.1	MAN:M	Yes [ ] N/A [ ]
MF17	Valid signature bit (12.11)	33.6.1.2.3	Logic ‘1’ indicates a valid signature has been detected	MAN:M	Yes [ ] N/A [ ]
MF18	Valid signature bit implementation	33.6.1.2.3	Will be implemented with a latching high behavior as defined in 33.6.1	MAN:M	Yes [ ] N/A [ ]
MF19	Invalid signature bit (12.10)	33.6.1.2.4	Logic ‘1’ indicates an invalid signature has been detected	MAN:M	Yes [ ] N/A [ ]
MF20	Invalid signature bit implementation	33.6.1.2.4	Will be implemented with a latching high behavior as defined in 33.6.1	MAN:M	Yes [ ] N/A [ ]
MF21	Short circuit bit (12.9)	33.6.1.2.5	Logic ‘1’ indicates a short circuit condition has been detected	MAN:M	Yes [ ] N/A [ ]
MF22	Short circuit bit implementation	33.6.1.2.5	Will be implemented with a latching high behavior as defined in 33.6.1	MAN:M	Yes [ ] N/A [ ]
MF23	Overload bit (12.8)	33.6.1.2.6	Set to ‘1’ when PSE state diagram enters the state ‘ERROR_DELAY_OVER’	MAN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF24	Overload bit implementation	33.6.1.2.6	Will be implemented with a latching high behavior as defined in 33.6.1	MAN:M	Yes [ ] N/A [ ]
MF25	MPS absent bit (12.7)	33.6.1.2.7	Read as logic 1 indicates either or both elements of the MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.11	MAN:M	Yes [ ] N/A [ ]
MF26	MPS Absent bit implementation	33.6.1.2.7	Will be implemented with a latching high behavior as defined in 33.6.1	MAN:M	Yes [ ] N/A [ ]