PSE Current Measurement

IEEE 802.3at Task Force

Anoop Vetteth

Problem

From Ripple and Noise Presentation:

Ripple and Noise	Vpp V	Ipp (Type 1) mA	Ipp (Type 2) mA
500Hz to 150kHz	0.2	17	24

- Consider a PSE ADC that has a sampling rate of 50kHz
- Consider a PD current waveform has maximum permissible ripple at ~ 50kHz or 100kHz i.e. 24mA Ipp (Type 2)
- Finite probability of sampling all the peaks of the ripple current
- Power draw reported by PSE is 0.6W more than actual power draw
- The PSE could potentially shut off a compliant PD

Solution

- Use an anti aliasing filter at the input to the PSE ADC to band-limit the waveform being sampled

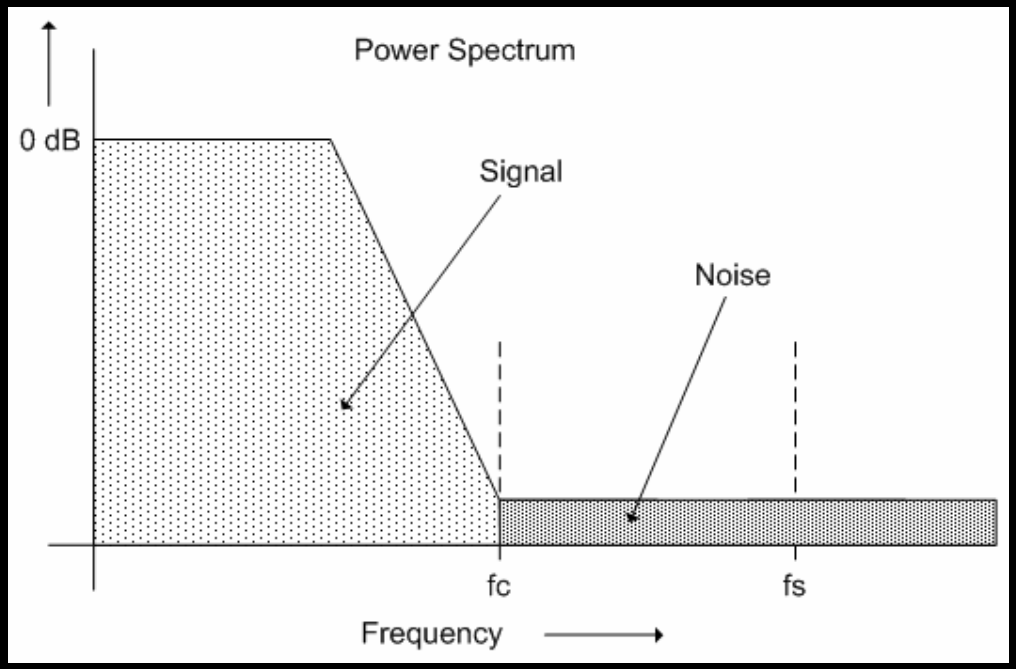
  OR

- Limit the bandwidth of the ripple current waveform that is permissible at the PD PI

Recommendation – Limit PD Bandwidth

- All PDs analyzed by the Vport ad-hoc had minimal or no ripple. Mandating type-2 PDs to limit the bandwidth of the ripple should have minimal impact
- Power policing is critical for type-2 PSE systems with over-subscribed power
- Ripple frequency content depends on the power supply architecture of the PD
- No cost impact to the PSE

Proposal



- fc is the cut-off frequency beyond which all ripple is treated as noise
- All ripple component at frequencies below fc is treated as signal
- fs is the sampling frequency and is usually 5 times fc

Proposal …… continued

- Overprovision 0.25W (?) at the PSE to account for aliasing while sourcing 30W
- SNR = 120 SNR(dB) ≈ 20dB
- fc = 2kHz (?)
- Most PSEs today can sample at > 4kHz
- Provides deterministic approach to power provisioning and policing