IEEE P802.3at Task Force
Power Via MDI Enhancements

PD Power Bandwidth- Worst Case Analysis
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Background

- There is a need to digitally sample the PD power in order to implement Power Management
  - **Note**: It is not the only way to implement power management
- In order to reduce PD power measurement errors we need to know the useful PD power bandwidth i.e. what is the frequency spectrum of the PD load changes as reflected to the PSE.
- Once the PD power bandwidth is known, the PSE sampling frequency and measurement error can be determined.
- The measurement error magnitude determines the sensitivity to false port disconnection when implementing power policing.
  - **Notes:**
  - 1. Power Policing is optional and not mandatory.
  - 2. Sampled data errors can be significantly reduced by simple filter/s
  - 3. Sensitivity to false port disconnection may be prevented by other means

PD Power Bandwidth – Test Setup

- PD Worst Case Power Changes Bandwidth is determined by the following method:
  - Changing PD load from Minimum Load (~0.5W) to maximum load (25.5W)
  - Measuring Vport as function of frequency or
  - Measuring Iport as function of frequency or
  - Measuring Pport as function of frequency
- Due to the fact that Ripple Voltage << Vdc
  - Vdc ~= Constant
  - Measuring Iport vs Frequency
  - Pport (f) ~= Vport x Iport (f)

How to find PD Power Bandwidth

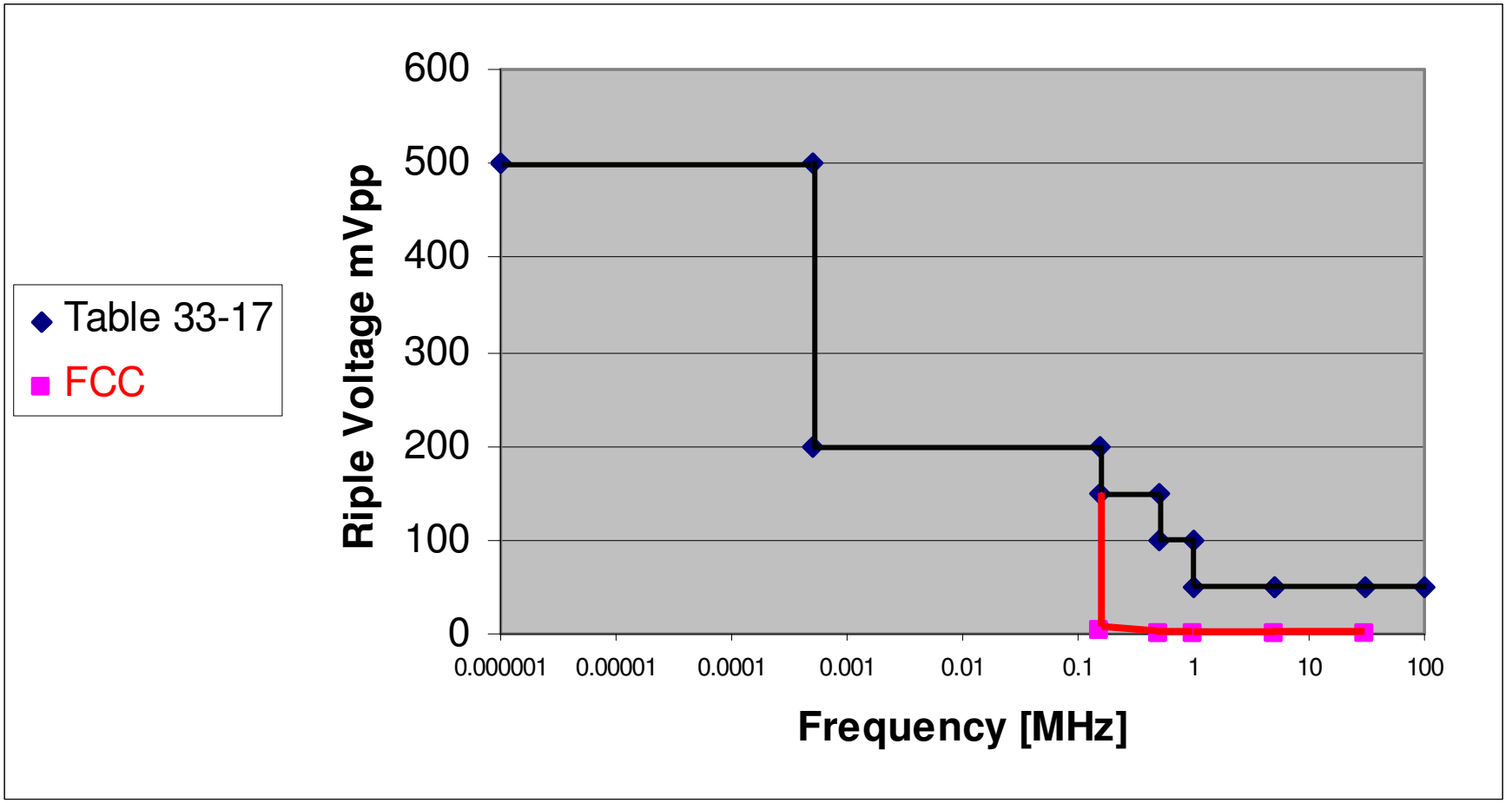
	Option A	Option B
	Measurements of many PDs	Worst Case Analysis Based on PD specification and Power Supply Design considerations
Covering most of current PDs	NO	YES
Covering most of PD load dynamics	NO	YES
Covering most of Future PDs based on PD specifications	NO	YES
Cost Effectiveness of conclusions	Low - Medium	High

Option B looks better i.e. Worst Case Analysis Based on PD specification and Power Supply Design considerations

Bandwidth limiting factors

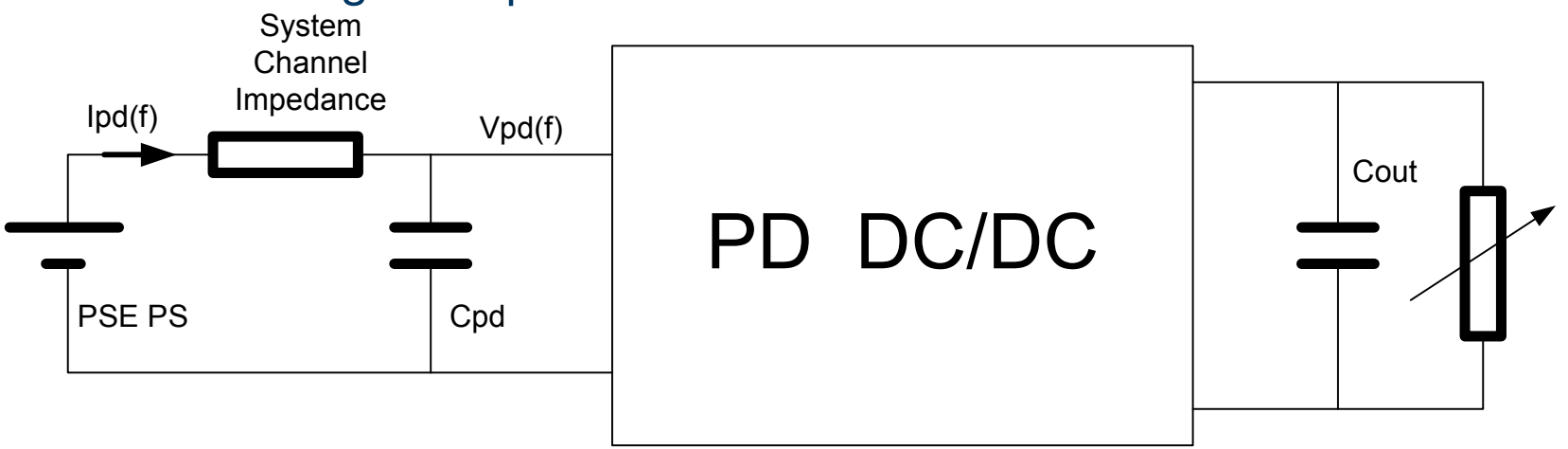
PD specification	W.C	Lowering BW
Table 33-12 item 6, Cport_min = 5uF	5uF	>5uF
Table 33-12 item 4, Class 4 Ppeak.	28.4W	<28.4W
Table 33-12 item 7, Ripple & Noise	0.5Vpp @ f<500Hz 0.2Vpp @ 500 Hz to 150KHz 0.15Vpp @ 150KHz to 500KHz 0.1Vpp @ 500KHz to 1MHz	< W.C
33.4.4 lines 23-24	0.05Vpp @ 1MHz to 100MHz	< W.C
PD Power Supply		
Switching Frequency 100KHz to 1MHz. Higher switching Frequency ➔ Higher Power supply Bandwidth	1MHz	< W.C
DC/DC converters passive elements: Output Capacitors and Inductors	DC/DC output ripple and regulation <5%. Determines DC/DC output capacitor Cout for min-max load variations	>Cout
EMI requirements - Conducted emissions (FCC Quasi-Peak values) (For current values, divide voltage by 50Ω)	0.002 V @ f=150KHz 0.00063 V @ f<500KHz 0.00063 V @ 5000KHz to 5MHz 0.001 V @ 5MHz to 30MHz	< W.C

PD Voltage BW limitations as derived by the PD explicit specifications



PD voltage BW limitations vs PD current bandwidth

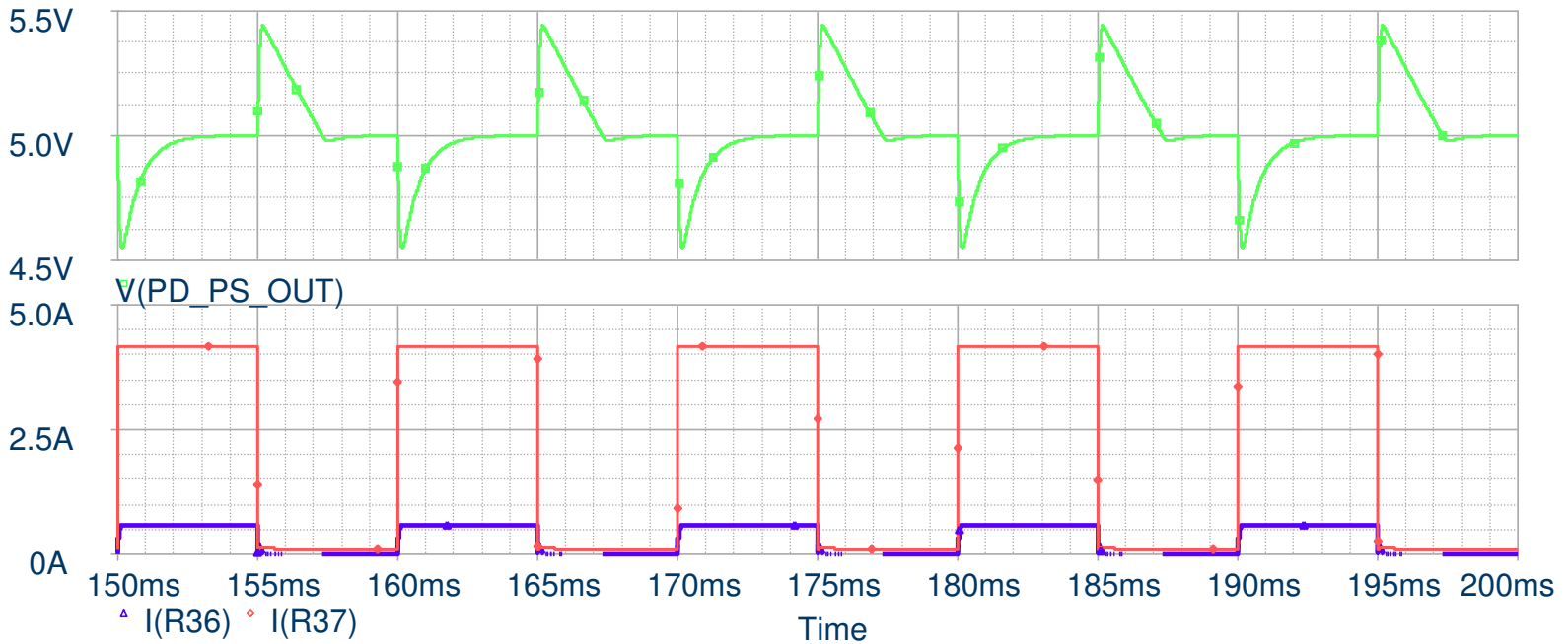
- For a given implementation, PD voltage bandwidth limitation specifications, Vpd(f) is controlled by PD input filter and PD DC/DC output filter.
- PD current bandwidth, Ipd(f) is function of System Channel Impedance and Vpd(f).
  - Ipd(f) = (Vpse – Vpd(f))/Channel_Imp
- Hence meeting PD specification will determine current bandwidth.



Approximated Worst Case Model

- Case 1
- Cpd=5uF minimum.
- DC/DC voltage loop reacts within 1msec
  - DC/DC output ripple and regulation <5%
    - Sets minimum Cout for low frequency ripple
  - Load step from ~0.5W to ~25.5W
    - Vout=5V, Iout_min=0.1A, Iout_max=4.16A, Pout=~10.65W
    - Load pulse duration at DC/DC output =5msec, Period = 10msec tr=tf=100uS (faster values are filtered by EMI requirements)
  - Load parameters tuned for 0.6A max at PD input at Vpd=42.5V
    - As a result: Pin_avg=0.013*42.5+(0.599-0.013)*42.5*5msec/10msec=~13W (<25.5W)

Worst Case Model Results – Time Domain

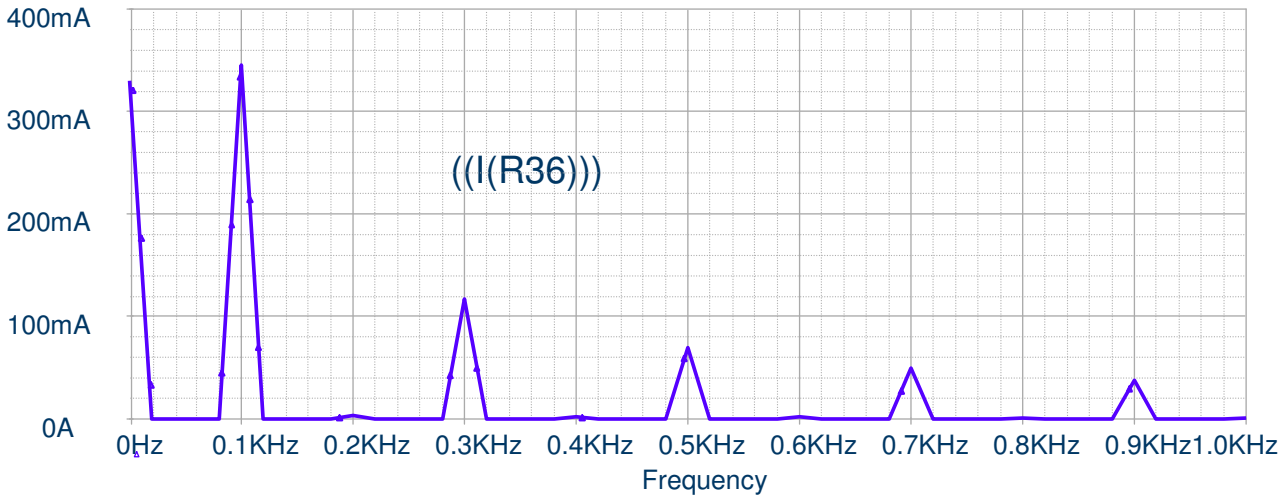


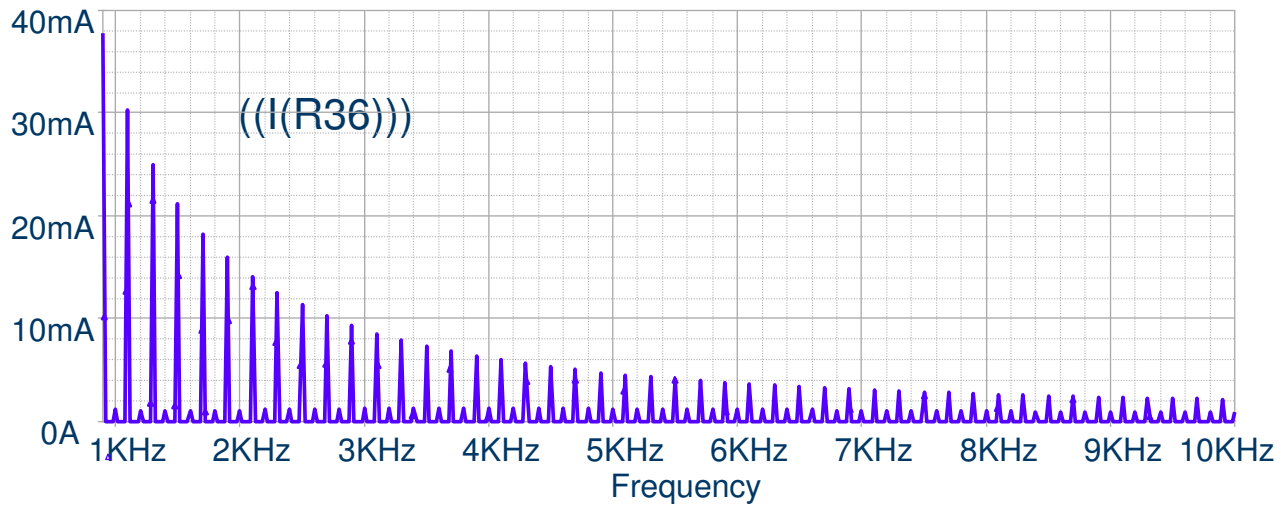
V(PD_PS_OUT) = PD DC/DC output voltage

I(R36)=PD input current

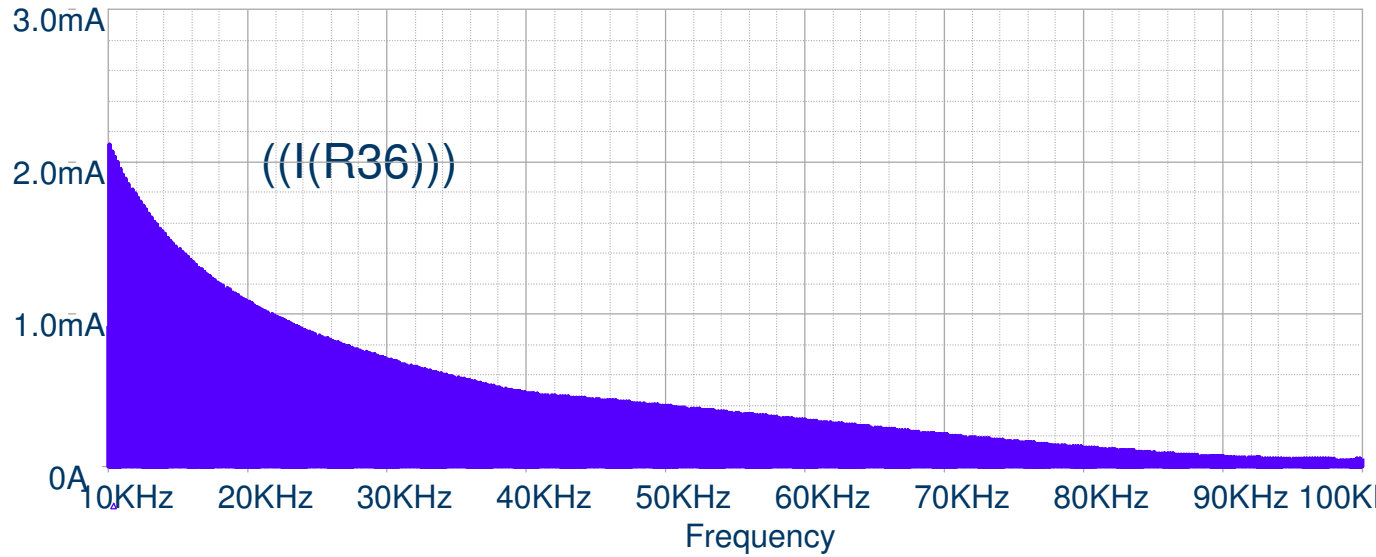
I(R37) = PD output load

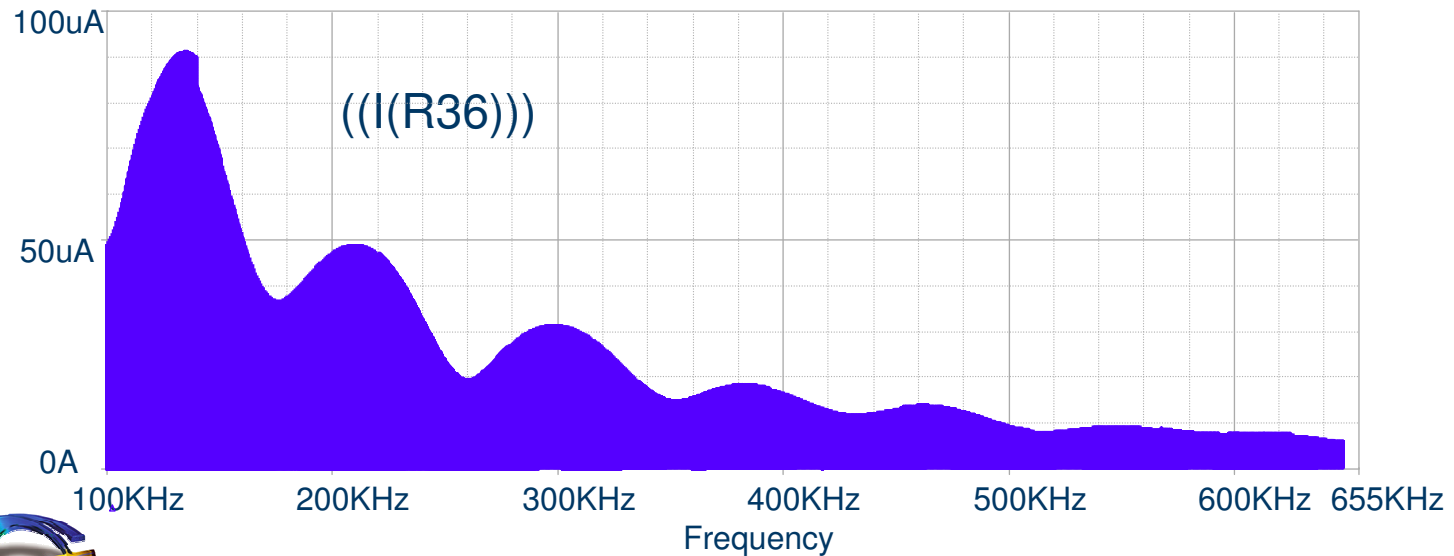
Worst Case Model Results – Frequency Domain





Worst Case Model Results – Frequency Domain





Conclusions

- Most of useful current energy lays well below 10KHz
- BW may further be reduced by alias filter
- Worst case current spectrum is in short cable
- PD vendor need to meet voltage ripple spec at PD input.
- No need for additional requirements for PD or PSE

Discussion

Annex A – FCC requirements for conducted emissions

Frequency range MHz	Class B Limits dB (uV)	
	Quasi-peak	Average
0.15 to 0.50	66 to 56	56 to 46
0.50 to 5	56	46
5 to 30	60	50

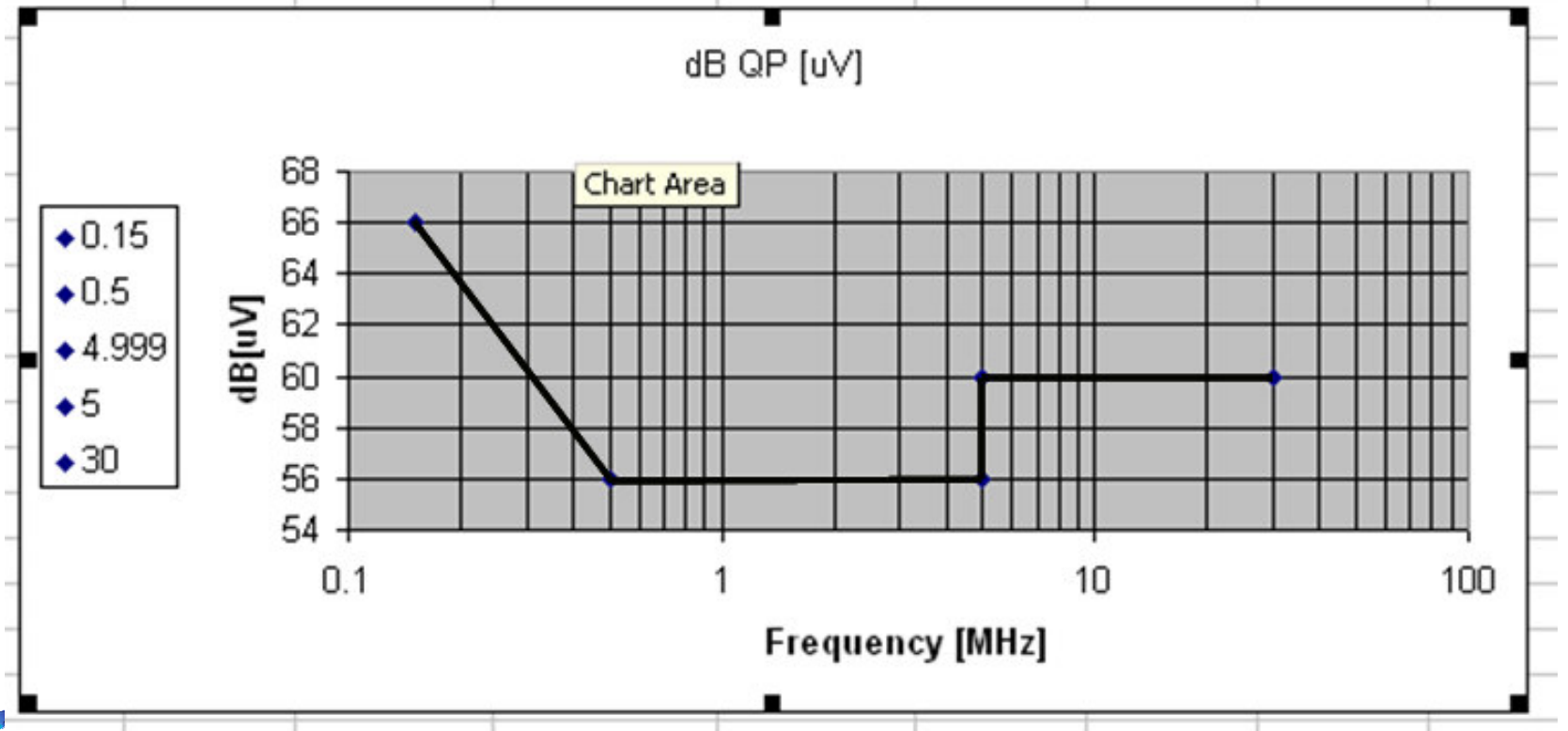
Note

1.The lower limit shall apply at the transition frequencies

2.The limit decreases linearly with the logarithm of the frequency in the range 0.15 MHz to 0.50 MHz.

Annex A1 – FCC requirements for conducted emissions

f[MHz]	dB QP [uV]	V	dB avg [uV]	Vavg
0.15	66	0.00200	56	0.00063
0.5	56	0.00063	46	0.00020
4.999	56	0.00063	46	0.00020
5	60	0.00100	50	0.00032
30	60	0.00100	50	0.00032



Annex B – Pair to Pair Conducted Emissions to maintain Data Integrity. Includes at least 20dB margin.

- Data is a differential signal across the pair
- Power is a Pair to Pair signal
- Pair to Pair (CM) to Differential Mode DM attenuation is >60dB at low frequencies.
- In addition, IEEE802.3-2005 contains 20dB minimum margin
- IEEE802.3 – 2005:

Table 33-12 item 7, Ripple & Noise

0.5Vpp	@ f<500Hz
0.2Vpp	@ 500 Hz to 150KHz
0.15Vpp	@ 150KHz to 500KHz
0.1Vpp	@ 500KHz to 1MHz

33.4.4 lines 23-24

0.05Vpp	@ 1MHz to 100MHz