

10Gb/s EPON FEC

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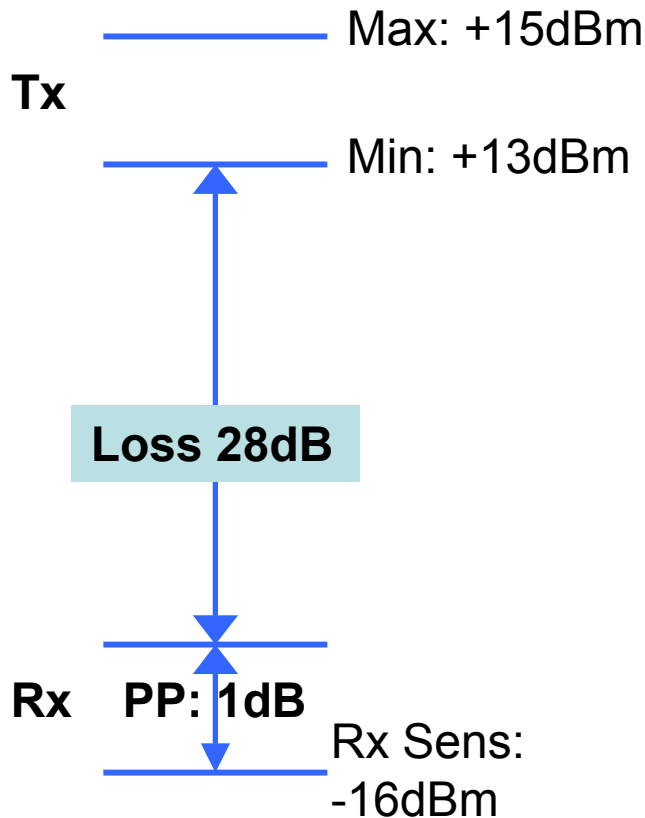
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Introduction

- From July meeting FEC “seems” to be considered as a mandatory part of the budget.
- The purpose of this presentation is to initiate generic discussion of using FEC to help 10G EPON power budgets, no plan to reach any concrete conclusion at this stage.
- This first set of slides address following FEC issue other than framing:
 - FEC rates/overhead
 - Algorithms
 - Code gain
 - Latency issue

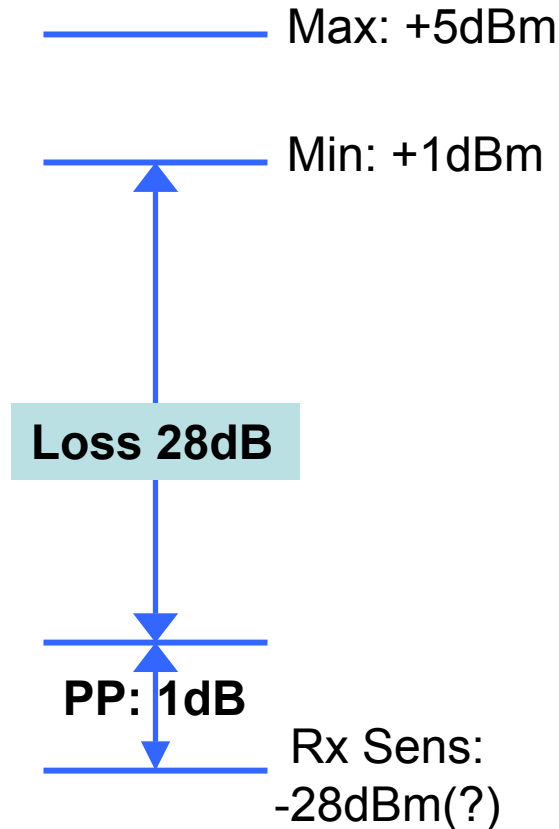
DS 29dB link budget (example)

SOA based Tx



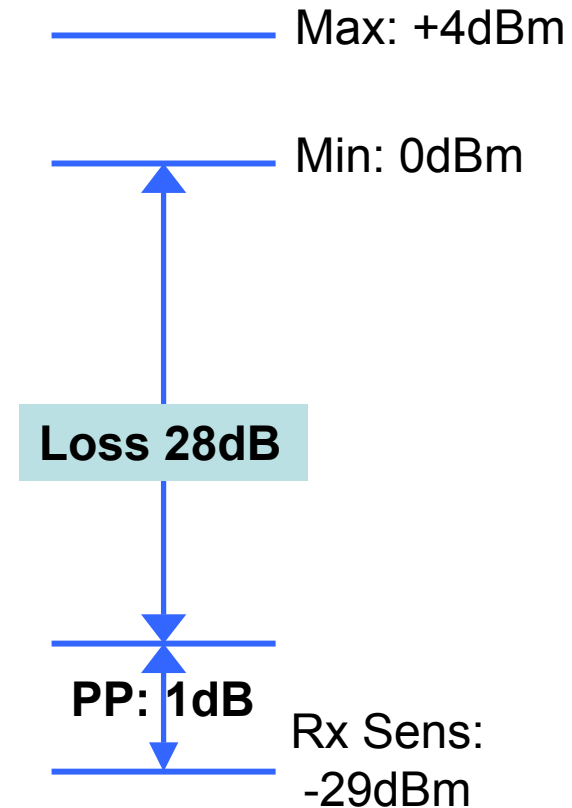
(Assume EA/SOA TX and PIN Rx)

SOA based Rx



(Assume SOA+PIN RX)
(Challenging due to large NF)

FEC-IC based Rx



(Assume APD+FEC Rx)
(Easy/margin with GFEC/EDC)

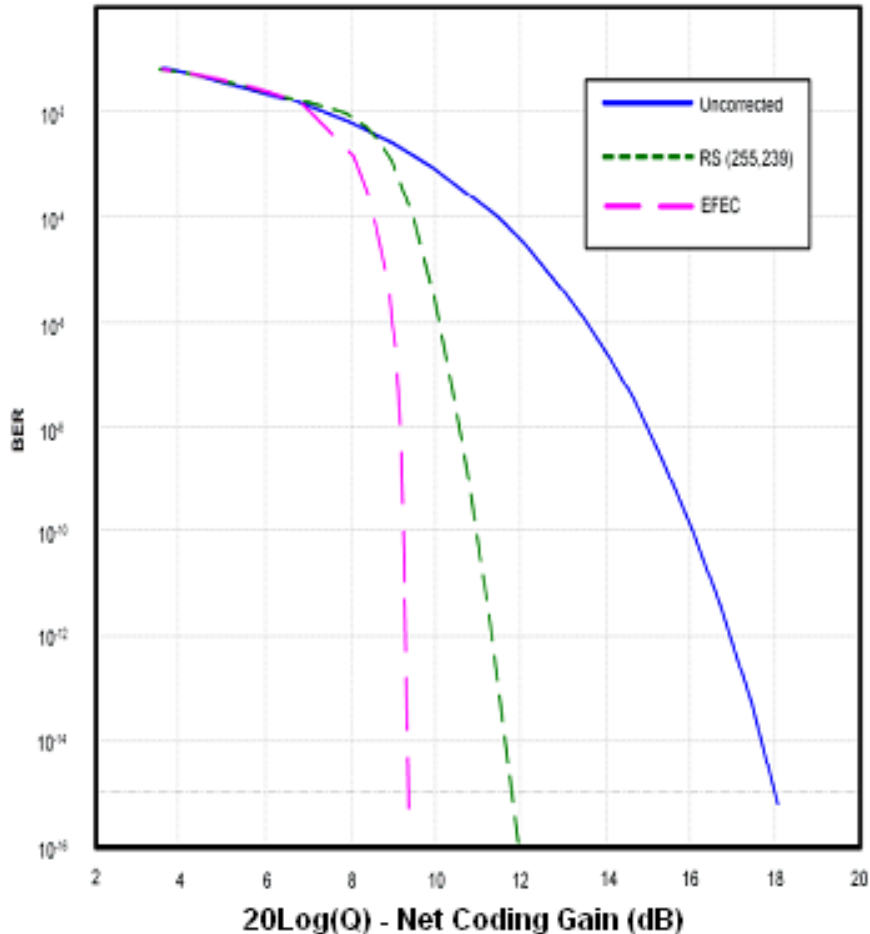
FEC cost saving consideration

Suggest evaluate cost saving parameters:

- The saving in system link cost by the increase in the number of ONUs.
- The saving in power budget from remaining gain.
- Silicon cost for FEC by integration including in transceiver.
- APD cost in case an APD is used.
- Power saving vs. FEC gate counts & gain.

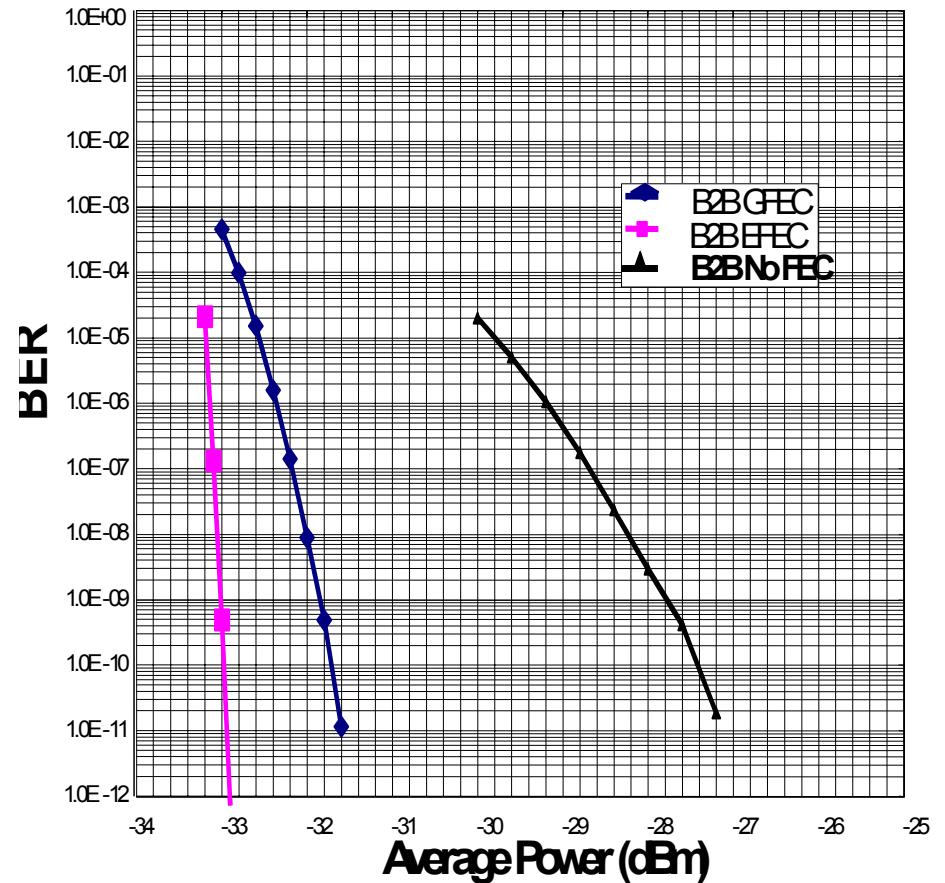
RS(255, 239) code: an example

Simulated results



Measured results

Vitesse FEC Performance Curves



(Note: Off-the-shelf APD is assumed)

RS(255, 239) code: an explanation

- The performance of a given code is uniquely represented by input BER vs. output BER, or net coding gain (after adjusting noise BW penalty).
- Optical gain (in dBm) normally does not match half of the coding gain (in dB).
- Optical gain depends on channel/Rx response
 - RS code: 6dB coding gain typically show over 4dB optical gain.
- RS codes is implemented in generic CMOS process.

Common codes with std rates

- Coding gain obviously implementation dependant (slightly).
- 64B/66B rate FEC: same rate as 10.3125Gb/s; ~2.5dB coding gain, input BER=1E-7.
 - Standard based code specified in OIF-CEI-P, backplane.
- RS(255, 239): 6-7% overhead, 6dB coding gain; input BER=1E-4.
- Enhanced FEC: 6-7% overhead same as RS(255, 239) (vendor proprietary); 8.5dB coding gain; input BER<1E-3.

Other codes in consideration

FEC lowers BER at the expense of overhead

- Alternative RS codes:
 - RS(255, 247): 4% overhead, 5dB
 - RS(255, 223): 12% overhead, 7.5dB
- BCH codes (weaker ones):
 - BCH(8191, 8178): 0.15% overhead, 2dB
 - BCH(8191, 8165): 0.32% overhead, 3dB
 - BCH(8191, 8152): 0.48% overhead, 4dB
- RS+BCH codes
 - RS(255, 239)+BCH(127,120): ~13% overhead, 6.5dB

Latency issues

- Latency obviously depends on framing and implementation.
- RS codes potentially has total latency $\sim 1\mu\text{s}$
 - Note: propagation in 200m fiber: $\sim 1\mu\text{s}$
- In ethernet, preferable small block sizes to minimize buffer size.
- Some existing FEC IC with long blocks may has well over $\sim 10\mu\text{s}$ total latency.

Trade-off of rate vs. performance

The group needs to answer the following:

- What rate is acceptable?
 - Non-std rates may require re-qualify the optics for the performance in the new rate.
 - LAN vs. WAN PHY? Piggyback on mature 10G/SONET.
- How much coding gain is enough?
 - Need to run through various power budget scenarios
- What is the clear trade-off between FEC perf. and its implementation (overhead, complexity, latency)?
 - Good news: most codes doable in CMOS.

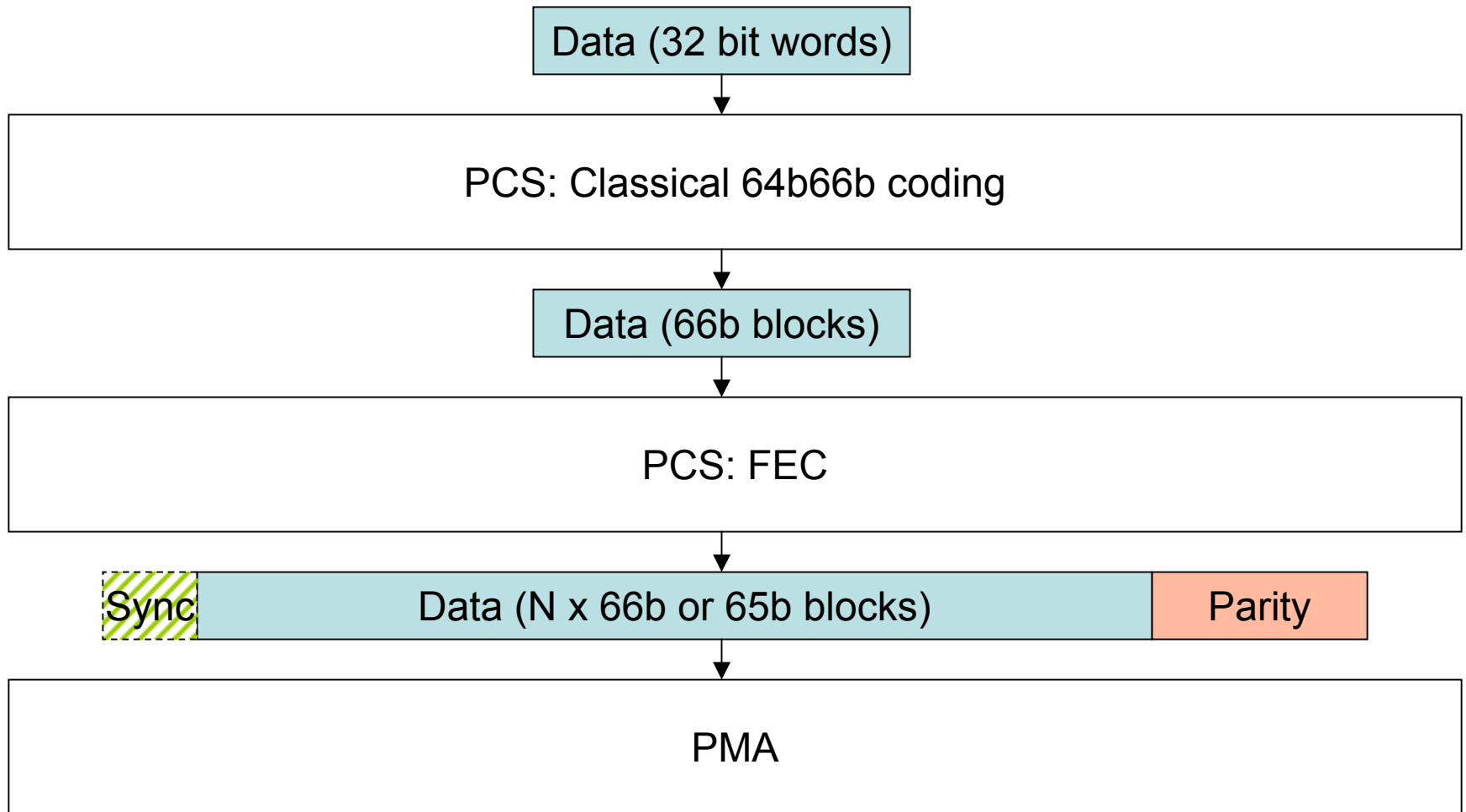
10 Gb/s EPON FEC - Framing

- Presentations in July seemed to demonstrate general consensus on:
 - FEC is most likely needed for 10G
 - FEC should be at the lowest layer
- There are two parts to the FEC puzzle
 - ‘Framing,’ or how to arrange the bits
 - ‘Algorithm,’ or the actual math of FEC
- This set of slides concentrates on framing

FEC framing - Common Ideas

- FEC will be applied at the lowest layer
 - Below the 64b66b sub-layer
 - Right before the PMA
- FEC sub-layer will be responsible for obtaining codeword lock, because without it, FEC is impossible
 - Frame lock must work with extensive errors
 - In the upstream, lock must work very fast
- 64b66b sub-layer will be handed aligned data, so there is no need for its own framing system
 - Or will it?

What FEC would look like



FEC framing structure issues

- There are several differently sized data objects in the 10G EPON technology that we should consider:
 - 64b66b blocks, 6.4 ns long
 - MPCP time quanta, 16 ns long
 - FEC codeword, (yet to be determined)
- There are different data rates to consider
 - 10.0000 Gb/s MAC rate
 - 10.3125 Gb/s 66b rate
 - “super” FEC rates (e.g., 10.7, 11.1 Gb/s)

Choice #1: Protocol Sizing

- How should we set the size of the relevant items (FEC codeword, synchronization pattern, time quanta)?
- One goal is to make everything integrally related so as to avoid fragmentation issues
- Other goals are: performance, flexibility, 1GEPON-compatibility (if upstream TDM is employed)

Choice #2: Line Rate

- Should we keep the optical line rate at 10.3125 Gb/s?
- If Yes, then desired FEC will need more overhead, and MAC control will need to slow down the MAC
- If No, then PMD and PMA operate at higher speed and slightly worse noise

Choice #2a: Rate Right Sizing

- If we are to choose a new line rate, then should we make the new rate a 'round number'
- If Yes, then clock generator circuits are simplified
- If No, certain pre-existing rates might be attractive (e.g., SONET FEC rates)

Example: Good codeword arrangements for 66b in RS(255,x)

- Maximum number of 66b blocks that fit is 28
 - 1848 bits payload
 - 40 bits synchronization
 - 128 bits parity
 - 252 total bytes: 9/8 line rate
- With an even number of quanta, 25 blocks fit
 - 1650 bits payload
 - 22 bits synchronization
 - 128 bits parity
 - 225 total bytes: 9/8 line rate

Choice #3: 66b or 65b

- Should the FEC payload be 66b blocks, or 65b blocks
- If 65b, then more efficient, removes redundancy
- If 66b, then less efficient, but more familiar, and the 2bit header might be useful for auxiliary framing purposes

Example: Good codeword arrangements for 65b in RS(255,x)

- Maximum number of 66b blocks that fit is 29
 - 1885 bits payload
 - 17 bits synchronization
 - 128 bits parity
 - 2030 total bits: 35/32 line rate
- With an even number of quanta, 25 blocks fit
 - 1625 bits payload
 - 22 bits synchronization
 - 128 bits parity
 - 1775 total bits: 71/64 line rate

Choice #4: Downstream FEC Sync

- How should we perform downstream synchronization?
- Serial locking?
- With a periodic sync pattern (present for each FEC codeword) ?

Choice #5: Burst FEC Sync

- How will we synchronize the upstream bursts?
- Use continuous sync: simple, but probably too much overhead
- Use a special burst preamble: more complicated, but more efficient

Final Thoughts

- A good FEC system is designed taking all the choices into account together
 - We shouldn't think that we will knock off these decisions one by one
 - The 'art' of the design is finding the one solution that best fits all the constraints